NCP51820 GaN Driver, PCB Design and Layout

AND9932/D

ABSTRACT

The NCP51820 is a 650−V, high speed, half−bridge driver capable of driving GaN power switches at dV/dt rates up to 200 V/ns. The full performance benefit of switching high voltage at high frequency with fast dV/dt edge rates can only be achieved with a properly designed printed circuit board (PCB) capable of supporting such aggressive power switching transitions. This whitepaper will highlight the most important PCB design considerations that must be taken into account for successfully designing a GaN based, half−bridge, gate drive circuit utilizing the NCP51820.

INTRODUCTION

The NCP51820 is a full−featured, dedicated driver intended to maximize high electron mobility transistor (HEMT) GaNFET switching performance. For similar rated breakdown voltage, GaNFETs are fabricated using a smaller die size compared to silicon. As a result, GaNFETs have significantly reduced gate charge, output capacitance and dynamic on−resistance compared to even the best in class silicon MOSFETs. In addition, GaNFETs do not include p-n junctions so there is no intrinsic, parasitic body−diode across the drain−source and therefore no reverse recovery charge associated with third quadrant operation.

GaNFETs can be especially beneficial in off−line, half−bridge power topologies, bridgeless PFC and single−ended, active clamp topologies. These power stages often employ zero voltage switching (ZVS) but can also operate under hard−switching conditions, from voltages in the range of 400 V. These combined improvements, enable GaNFETs to switch at or near frequencies in the MHz range with drain−source edge rates as high as 100 V/ns. Achieving optimal performance from GaN based power stages is highly dependent upon the designer's understanding of parasitic circuit elements such as package inductance, PCB trace inductance, transformer capacitance and component selection and placement. While these various parasitic elements also exist in silicon MOSFET power systems, they become much more responsive and therefore, problematic when stimulated by the high dV/dt and di/dt that can exist in a GaN power solution.

The NCP51820, MLP leadless power package (Figure 3) combined with the various leadless GaNFET power packages (Figure 1 and Figure 2) available in the industry attest to the amount of design effort placed upon minimizing parasitic inductance. Similarly, specific care must be given to the PCB design and component placement. This whitepaper will focus on some of the most important PCB design considerations necessary to take full advantage of the benefits offered from using the NCP51820 for driving GaN power switches used in high−speed, half−bridge power topologies.

HEMT GaN AND NCP51820 PACKAGE DESCRIPTIONS

Most GaNFET packages include a dedicated source Kelvin return, shown as "SK" in Figure 1, which is intended only to carry gate drive return current back to the NCP51820. The higher current drain−source pins are bonded to multiple pads using multiple bond wires, although the simplified diagram in Figure 1 shows only single bond wire connections for simplicity. The interface between the NCP51820 outputs and the GaNFET gate−source Kelvin needs to be a direct single point connection and is especially critical as described in section GaNFET with Source Kelvin Pin.

However, not all GaNFETs include a dedicated source Kelvin return, such as the example shown in Figure 2. For GaNFETs that do not include a source Kelvin return, special care must be taken when routing the gate drive portion of the PCB design. For the switch−node connection in a half−bridge power stage, the source of the high−side GaNFET connects directly to the drain of the low−side GaNFET creating a high dV/dt node carrying high di/dt load current. Referencing the gate drive return directly from this high−voltage switch−node is not recommended as described in section GaNFET without Source Kelvin Pin.

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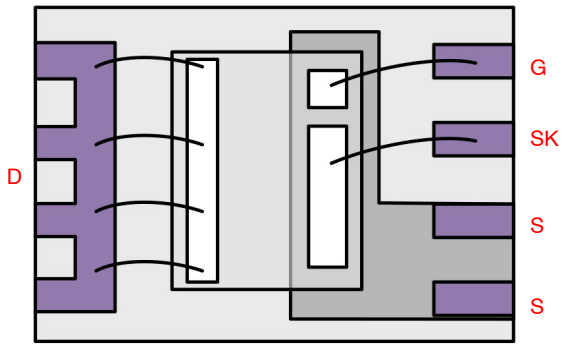

Figure 1. Typical GaN with Source Kelvin Return

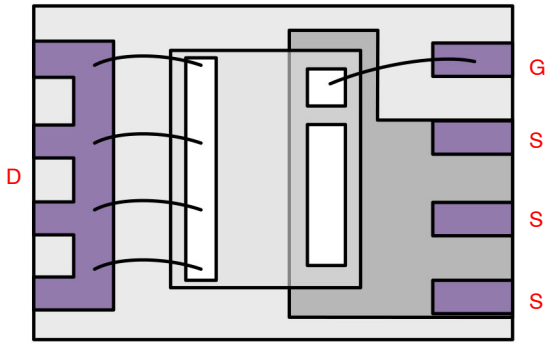

Figure 2. Typical GaN without Source Kelvin Return

The NCP51820 is packaged in a 4x4 mm, leadless package with all logic level inputs and programming functions grouped together on the right side of the IC, separate from the power functions which are strategically grouped on the remaining three sides of the IC. The pins are strategically placed to provide high−voltage isolation where necessary. The advantage of the NCP51820 pin assignments will become apparent throughout the following PCB layout sections.

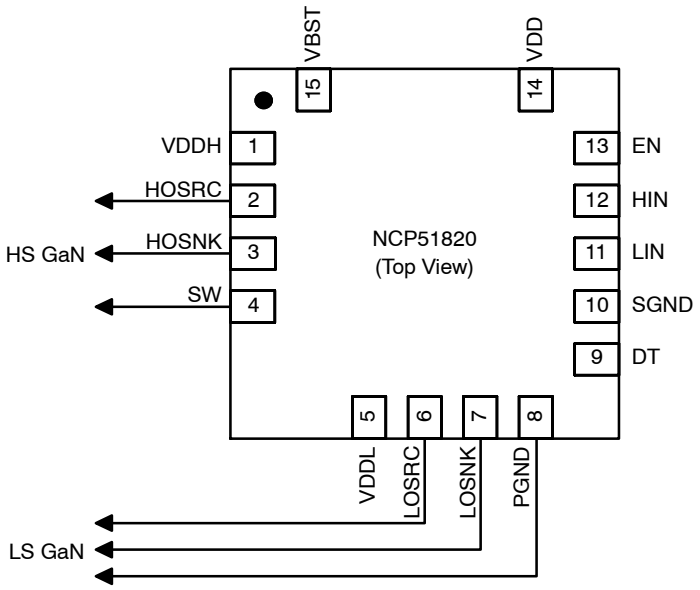

Figure 3. NCP51820 GaN Driver Pin Assignments

PCB DESIGN STRATEGY SUMMARY

When beginning a PCB design using GaNFETs, the best layout procedure is one that is priority−driven as listed below. Each of these “summary” comments will be highlighted in more detail with clarifying diagrams in the following sections.

1. Multi−layer PCB designs with proper use of ground/return planes as described in this document are a must. High frequency, high voltage, high dV/dt and high di/dt all warrant the need for a multi−layer PCB design approach. Inexpensive, single−layer PCB designs do not allow for proper routing or design of ground planes necessary to realize the full benefits of a GaN based power stage.
2. Begin by placing the most noise sensitive components near the NCP51820 first. VDD, VDDH and VDDL bypass capacitors as well as the VBST capacitor, resistor and diode should be placed as close to their respective pins as possible.
3. Place the DT resistor directly between the DT and SGND pins.
4. Place the HO and LO, source and sink gate drive resistors as close to the GaNFETs as possible.
5. Move the NCP51820 and associated components as close as possible to the GaNFET source and sink resistors.
6. If possible, arrange the GaNFETs with the goal of maintaining the HO and LO gate drive lengths as closely matched as possible. To avoid high current and high dV/dt through vias, it is preferred that both GaNFETs be located on the same side of the PCB as the NCP51820.
7. The HO and LO gate drives should be considered as two independent gate drive circuits that are electrically isolated from each other. HO and LO will therefore each require dedicated copper land return planes on layer 2 directly beneath layer 1 gate drive routing.

Proper routing of the power loop, switch−node, gate drive loops and use of planes are critical for a successful GaN PCB design. These will each be addressed and illustrated in the following sections. For the gate drives, proper routing and noise isolation will help reduce additional parasitic loop inductance, noise injection, ringing, gate oscillations and inadvertent turn-on. The goal is to design a high frequency, power PCB that is thoughtful with regard to proper grounding while maintaining controlled current flow through direct pathway connections with minimal loop distances.

COMPONENT PLACEMENT AND ROUTING

The diagram shown in Figure 4 highlights the critical component placement around the NCP51820 and the interface to the HS and LS GaNFETs.

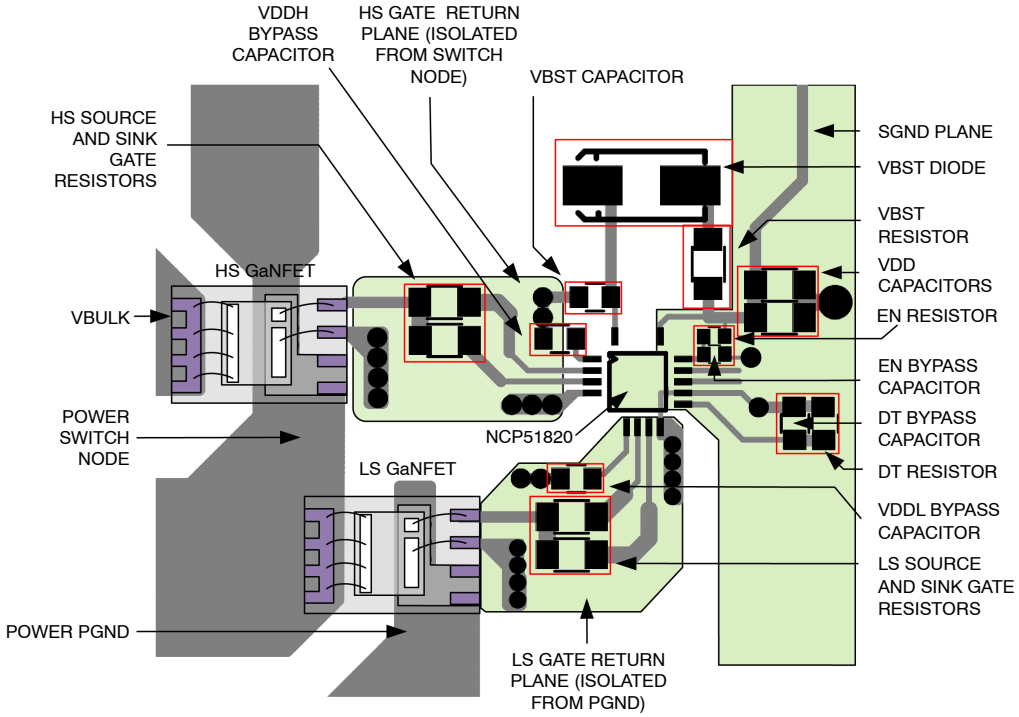

Figure 4. NCP51820 Component Placement

GaNFET with Source Kelvin Pin

Many GaNFET packages include a dedicated source Kelvin pin, reserved for isolating the gate drive return current from the higher current and voltage levels seen at the power switch−node (high−side) or power ground (low−side). For GaNFETs with dedicated source Kelvin pins, the gate−drive routing is fairly straight forward. An example of the recommended PCB routing design illustrating careful separation of the high−side GaNFET gate drive return from the power, switch−node current is shown in Figure 5.

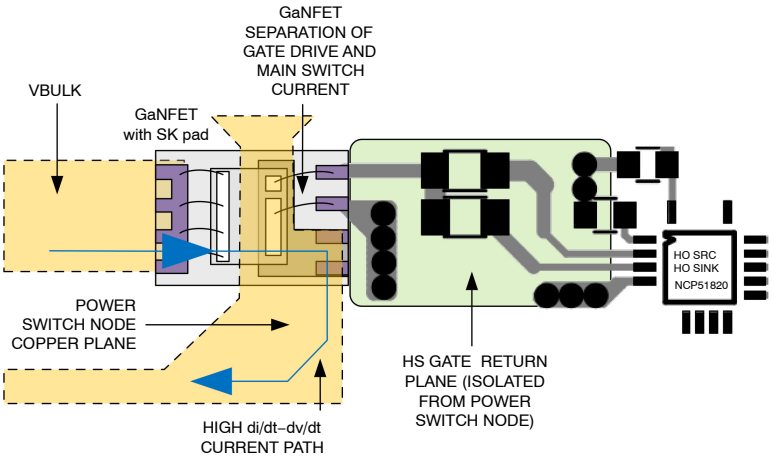

Figure 5. Source Kelvin GaNFET Routing

GaNFET without Source Kelvin Pin

Some GaNFET packages do not include a dedicated source Kelvin pin so additional consideration must be given for isolating the gate drive return current from the higher current and voltage levels seen at the power switch−node (high−side) or power ground (low−side). For GaNFETs without dedicated source Kelvin pins, an additional piece of copper etch should be routed from the GaNFET source, serving the sole purpose of carrying the gate drive return current back to the NCP51820. Although not as effective as having a dedicated Kelvin pin connection, this routing technique can still achieve an acceptable degree of separation between gate drive current and power switch−node. An example of the recommended PCB routing design illustrating careful separation of the high−side GaNFET gate drive return from the power, switch−node current is shown in Figure 6. The design goal for either GaNFET package type is to not introduce the NCP51820 and associated supporting circuitry to the potentially disruptive switching voltage and current flowing through the power stage. Additional details regarding gate drive routing and the use of isolated copper gate drive return planes is discussed in section Gate Drive Routing.

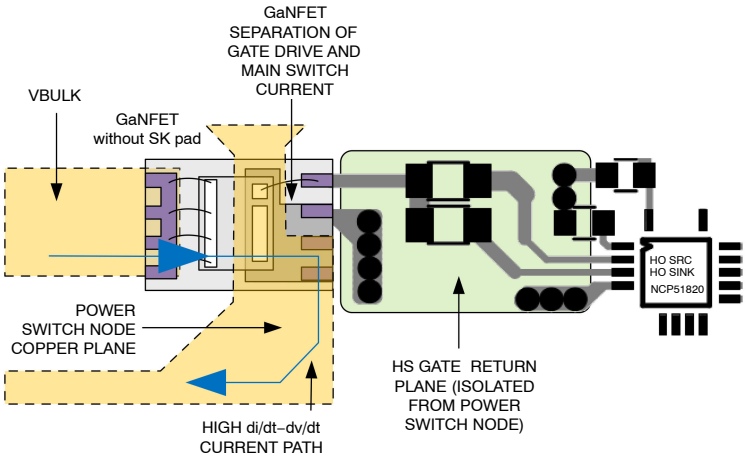

Figure 6. GaNFET Routing with no Source Kelvin Pin

The remainder of this design document will refer to routing examples using GaNFET packages that include source Kelvin connecting pins.

VDD Capacitors

The VDD pin should have two ceramic capacitors placed as close to the VDD pin as possible. A lower value high frequency bypass capacitor (typically 0.1 μF) should be placed closest to the VDD pin along with a second parallel capacitor (1 μF) as shown in Figure 7.

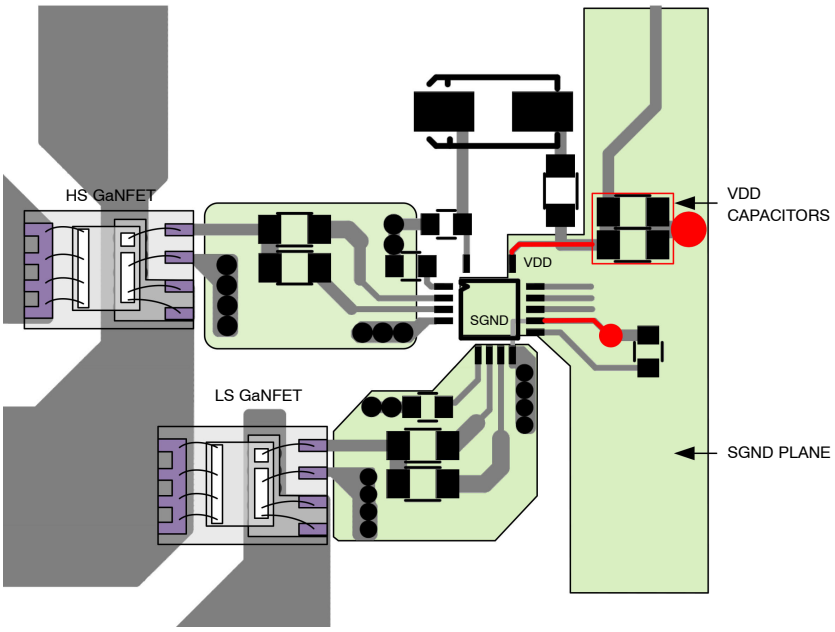

Figure 7. NCP51820 VDD Capacitor Placement and Routing

Keep all traces as short and direct as possible. Vias can be used, as the VDD current is relatively low. An SGND return plane is preferable for its shielding properties as well as keeping all signal−side ground returns at the same potential. The SGND plane is on layer 2, to keep it close to the signal−side components and the NCP51820. All signal−side components are placed over the SGND plane and connect through vias. A direct connection between the VDD pin and VDD capacitors should be made while the use of vias as return connections to the SGND plane is preferred.

The two VDD capacitor ground connections are joined and connected to the SGND plane through a single via as shown in Figure 7. If possible, a solid, unbroken SGND ground plane is best to avoid ground loops. It is recommended to extend the “quiet” SGND plane beneath the NCP51820 to aid in shielding the driver IC from noise. Notice in Figure 7, the SGND plane does not extend beneath the NCP51820 gate drive output pins. This is intentional so as to avoid the possibility of coupling noise from the gate drive di/dt source and sink peak currents into the SGND plane.

VBST Capacitor and Diode, VDDH and VDDL Bypass Capacitors

Place the VBST capacitor as close as possible to the VBST pin. The VBST capacitor return should connect to the driver SW pin, VDDH return and the source Kelvin of the GaNFET. Each of these connections is common through vias tied to the HS gate return plane, as shown in Figure 8. It is important to note that there should be no connection from the power stage switch−node back to the NCP51820. Do not connect the VBST capacitor to the power stage switch−node. The only connection from “switch−node” is through the HS GaNFET source Kelvin pin.

The HS gate return plane should be designed such that there is no overlap or interaction with the power stage switch−node. Similarly, the LS gate return plane should be designed such that there is no overlap or interaction with the LS GaNFET power ground. Do not place the SGND plane below the VBST diode or VBST capacitor, as the high dV/dt present on the cathode of the VBST diode can inject noise into the SGND plane.

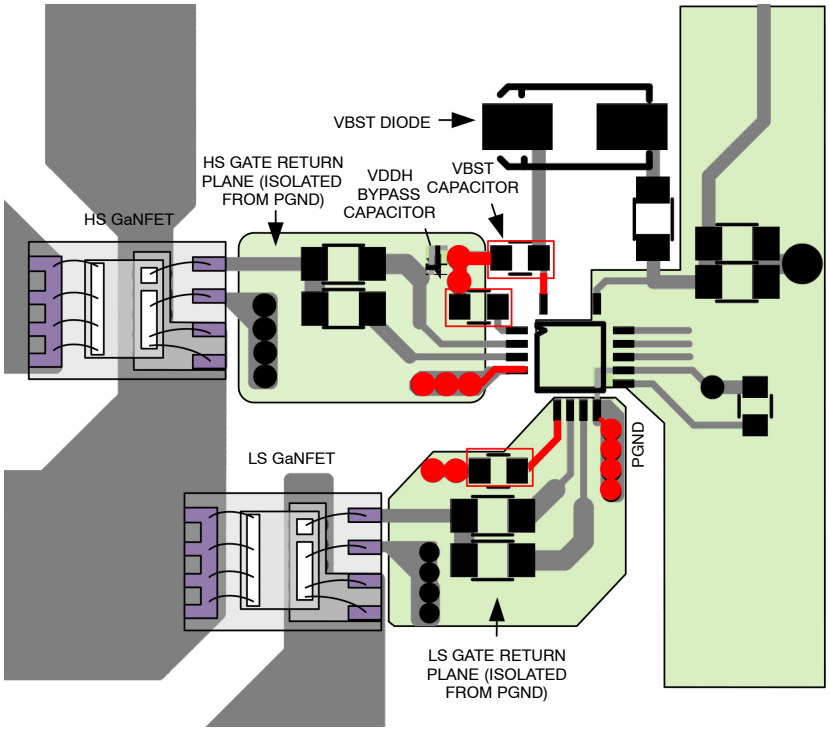

Figure 8. NCP51820 VBST Capacitor and Diode, VDDH and VDDL Capacitors

Place the VDDH capacitor as close as possible to the VDDH pin. The VDDH capacitor return should connect to the HS gate return plane through a via (shares a double via connection with the VBST capacitor) as shown in Figure 8.

Place the VDDL capacitor as close as possible to the VDDL pin. The VDDL capacitor return should connect to the LS gate return plane through vias as shown in Figure 8. The VDDL capacitor return must connect to the PGND pin on the driver. The VDDL capacitor return connects through vias to the LS gate return plane, which is also connected through vias to the driver PGND pin.

For VBST, VDDH and VDDL, multiple vias are needed because of the high peak, gate drive currents and to reduce parasitic via inductance. In this example, four vias are used for each GaNFET gate return connection. This is a reasonable trade−off between obtaining a low−impedance connection between the NCP51820 gate drive returns and the GaNFET returns while maintaining a solid return plane with good shielding integrity. If possible, conductively filled vias are preferred due to their even lower associated inductance.

Gate Drive Routing

When the NCP51820 is sourcing current to the HS GaNFET gate, the gate current is derived from the charge stored in the VDDH regulator bypass capacitor. As illustrated in Figure 9, source current flows through the HO driver source impedance, the gate−source resistor, and into the GaNFET gate. The current then returns from the GaNFET source Kelvin pin and back to the VDDH bypass capacitor.

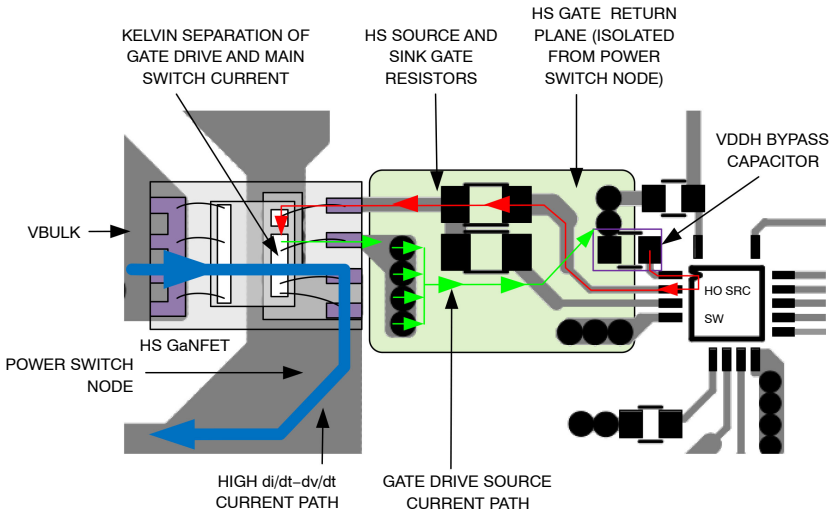

Figure 9. High−Side Gate Drive Source Current

When the NCP51820 is sinking current from the HS GaNFET, the current is derived from the energy stored in the gate−source capacitance. As shown in Figure 10, sink current flows from the HS GaNFET gate, through the gate sink resistor, through the HO SINK driver impedance, through SW pin and back to the GaNFET source Kelvin pin.

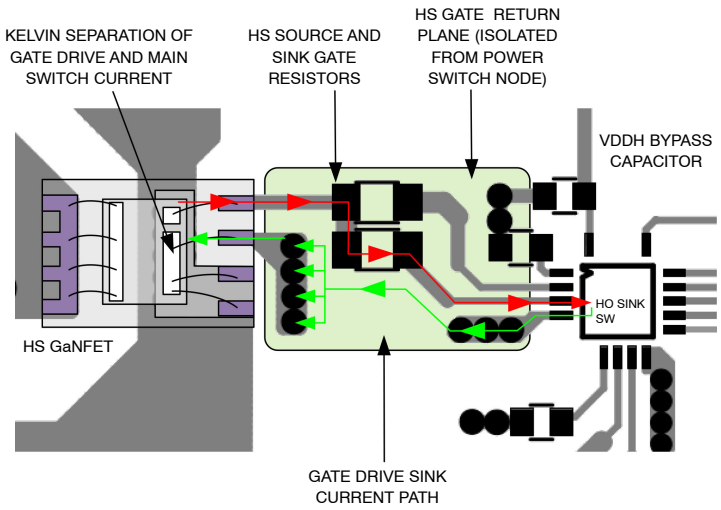

Figure 10. High−Side Gate Drive Sink Current

When the NCP51820 is sourcing current to the LS GaNFET gate, the gate current is derived from the charge stored in the VDDL regulator bypass capacitor. As shown in Figure 11, source current flows through the LO driver source impedance, the gate−source resistor, and into the GaNFET gate. The current then returns from the GaNFET source Kelvin pin and back to the VDDL bypass capacitor.

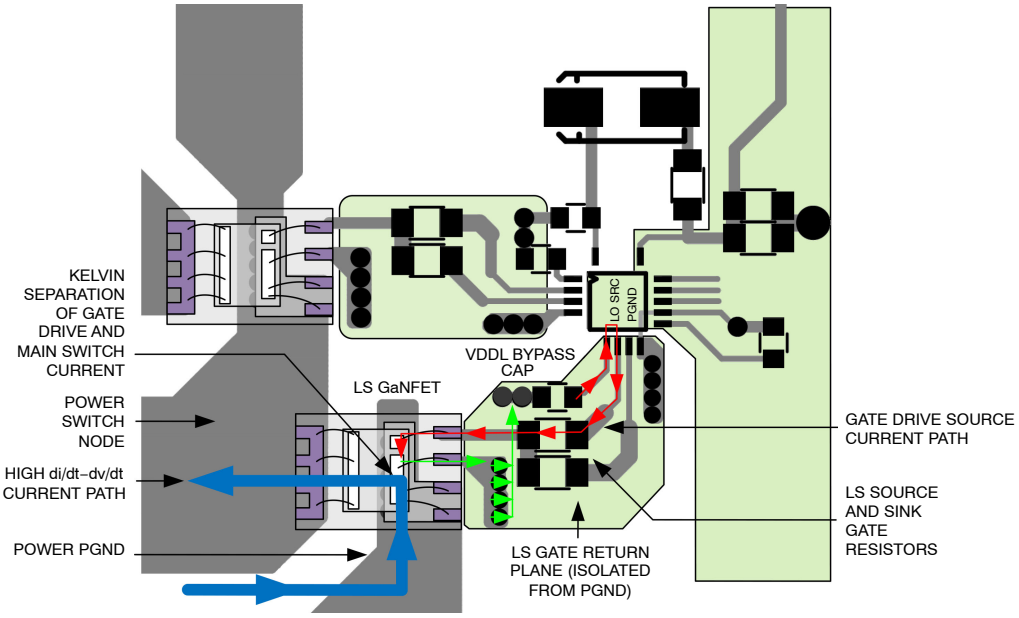

Figure 11. Low−Side Gate Drive Source Current

When the NCP51820 is sinking current from the LS GaNFET, the current is derived from the energy stored in the gate−source capacitance. As shown in Figure 12, sink current flows from the LS GaNFET gate, through the gate sink resistor, through the LO SINK driver impedance, through the PGND pin and back to the GaNFET source Kelvin pin.

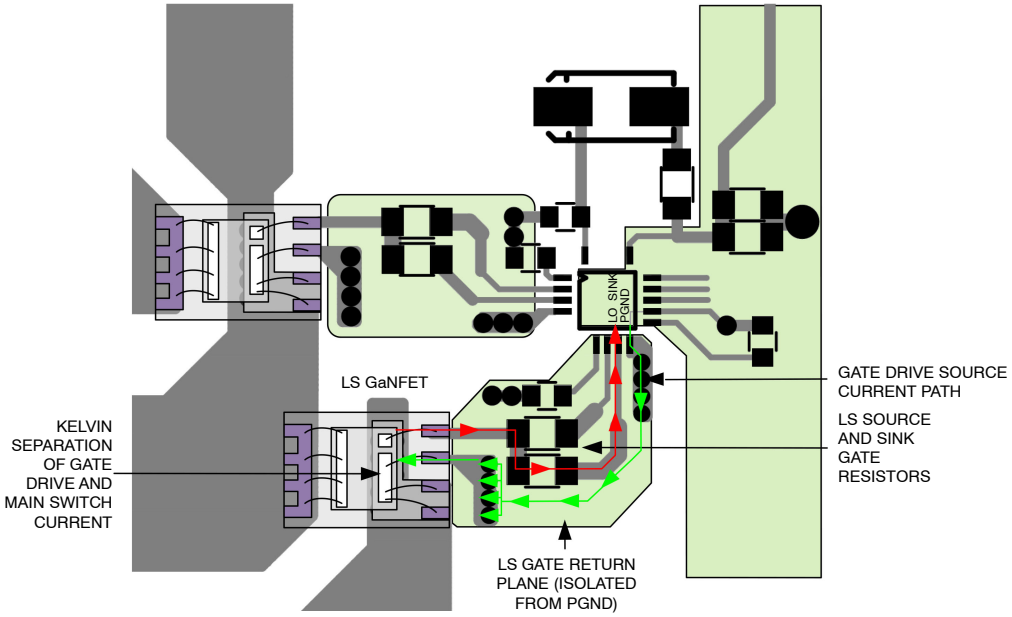

Figure 12. Low−Side Gate Drive Sink Current

GaNFETS can operate at high switching frequency with high dV/dt occurring during drain−source switching (100 V/ns and higher). Because the gate−source turn−on threshold is lower for GaN (<2 V), it is imperative that the gate drive source and sink paths be kept as short and direct as possible to mitigate the adverse effects of parasitic trace inductance. Excess parasitic inductance in the gate loop can cause gate oscillations or high frequency ringing that can exceed the gate−source threshold voltage. Vias in the gate drive and return path should be used only when absolutely necessary. Conductively filled vias are preferred, as they have far less inductance per via. Using a current carrying return plane under the gate resistors and associated routing, helps reduce the loop inductance by providing a return path that is directly under the source and sink path.

The NCP51820 high−side and low−side drives are internally isolated from each other. For the high−side, the SW pin must be isolated from the power switch−node to prevent switching noise from being injected into the gate drive path, and can only connect to the SK pin on the high−side GaNFET. The Kelvin connection between the source Kelvin pin and the source pins is the only electrical connection between the NCP51820 SW pin and the power stage switch−node, as illustrated in Figure 9 and Figure 10.

Similarly, the low−side gate drive should be routed such that the NCP51820 PGND pin is isolated from the power stage PGND, and can only connect to the SK of the low−side GaNFET. The design goal is to avoid power PGND noise from being injected into the low−side, gate drive path. Inside the low−side GaNFET, there is a Kelvin connection between the SK pin the power source pins, which is the actual connection between the NCP51820 PGND and the power PGND, as illustrated in Figure 11 and Figure 12.

Both HS and LS gate traces should be as equal in length as the design allows. This will help assure both GaNFETs have similar gate drive impedance. Staggering the alignment of the high−side and low−side GaNFETs serves the dual purpose of allowing nearly symmetrical, equidistant gate drive routing and permitting a larger, higher current, power switch−node copper land.

Assigning the HS and LS return planes to layer 2 is preferred and places them directly under the gate drive resistors and traces which helps reduce gate drive loop inductance. For the high−side GaNFET, because the VDDH bypass capacitor return and the NCP51820 SW pin are separated by the HO source and HO sink traces, unfilled vias can be used to connect to the source Kelvin pin of the GaNFET, through the HS gate return plane. Multiple vias are recommended to help reduce via inductance. Note that the gate drive current path is isolated from the power switch−node current path to minimize the occurrence of noise from the main current path being injected into the gate drive current path.

For the low−side GaNFET, because the VDDL bypass capacitor return and the NCP51820 PGND pin are separated by the LO source and LO sink traces, unfilled vias can be used to connect to the source Kelvin pin of the GaNFET through the LS gate return plane. Multiple vias are recommended to help reduce parasitic via inductance. Note that the gate drive current path is isolated from the power PGND current path to minimize the occurrence of noise from the main current path being injected into the gate drive current path.

Signal Ground (SGND) and Power Ground (PGND)

SGND is the GND for all internal control logic and digital inputs. Internally, the SGND and PGND pins are isolated from each other. PGND serves as the low−side gate drive and return reference.

For half−bridge power topologies or any applications using a current sense transformer, the NCP51820 SGND and PGND should be connected together on the PCB. In such applications, it is recommended to connect the SGND and PGND pins together with a short, low−impedance trace on the PCB as close to the NCP51820 as possible. Directly beneath the NCP51820 is an ideal way to make the SGND to PGND connection as illustrated in Figure 13.

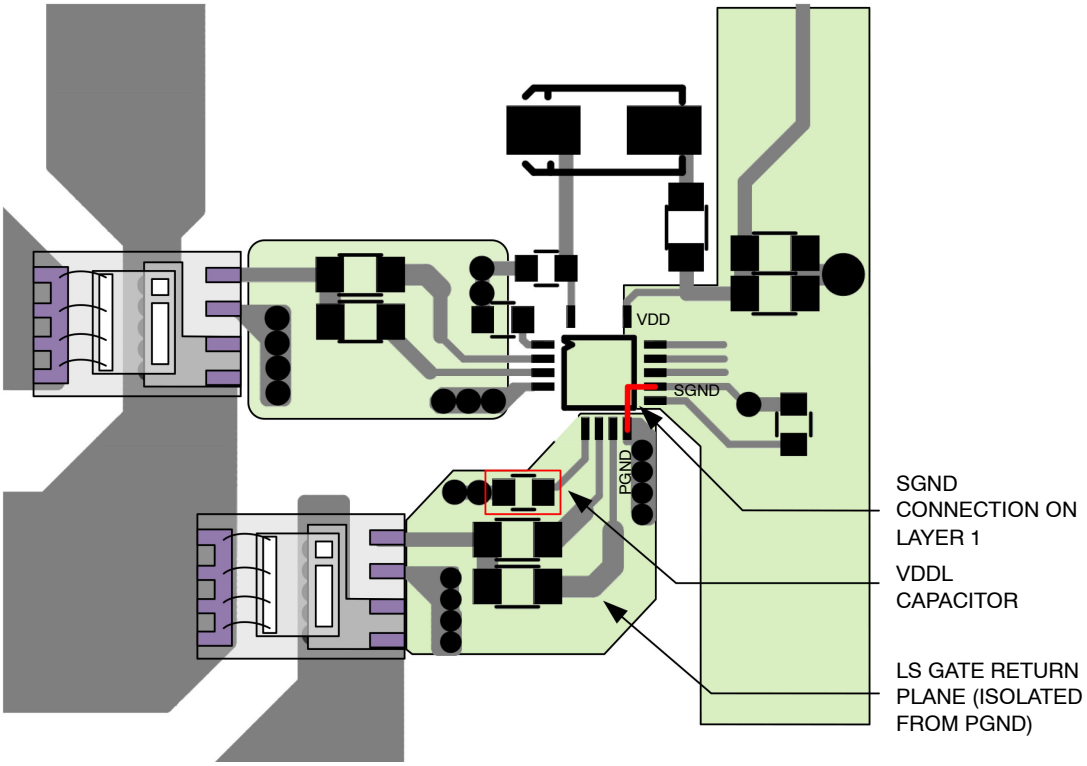

Figure 13. PGND to SGND, 0−Ω Single Point Connection

For low−power applications, such as an active−clamp flyback or forward converter, a current sensing resistor, R_{CS}, located in the low−side GaN FET source leg is commonly used. In such applications, the NCP51820 PGND and SGND pins must not be connected on the PCB because R_{CS} would essentially be shorted through this connection. The NCP51820 low−side drive circuit is able to withstand −3.5 V to +3.5 V of common mode voltage. Since most current sense voltage signals are less than 1−V, the low−side drive stage can easily “float” above the voltage, V_{RCS}, generated by the current sense. As illustrated in Figure 14, the entire low side gate drive is floating above V_{RCS}. This is important because it ensures no loss of gate drive amplitude so the full VDDL voltage appears at the low−side GaN FET gate−source terminals.

When laying out a circuit as described in the above paragraph, the controller HO/LO path connecting to the NCP51820 HIN and LIN must return to the controller GND to complete the circuit. Therefore, the NCP51820 SGND and the controller GND must be connected. This is accomplished by connecting both the NCP51820 SGND and the controller GND to the SGND plane with vias, as illustrated in Figure 14. The SGND plane is for signal and signal−side VDD return only, and will also act as a shield for the signals. As the V_{RCS} return must also connect to the controller GND, this should be done with a single, low−impedance trace, run as close as possible (or under) to the V_{RCS} trace. This will connect the power stage PGND to the SGND at a single point, and will isolate the high dV/dt and di/dt on the power stage PGND from the SGND plane.

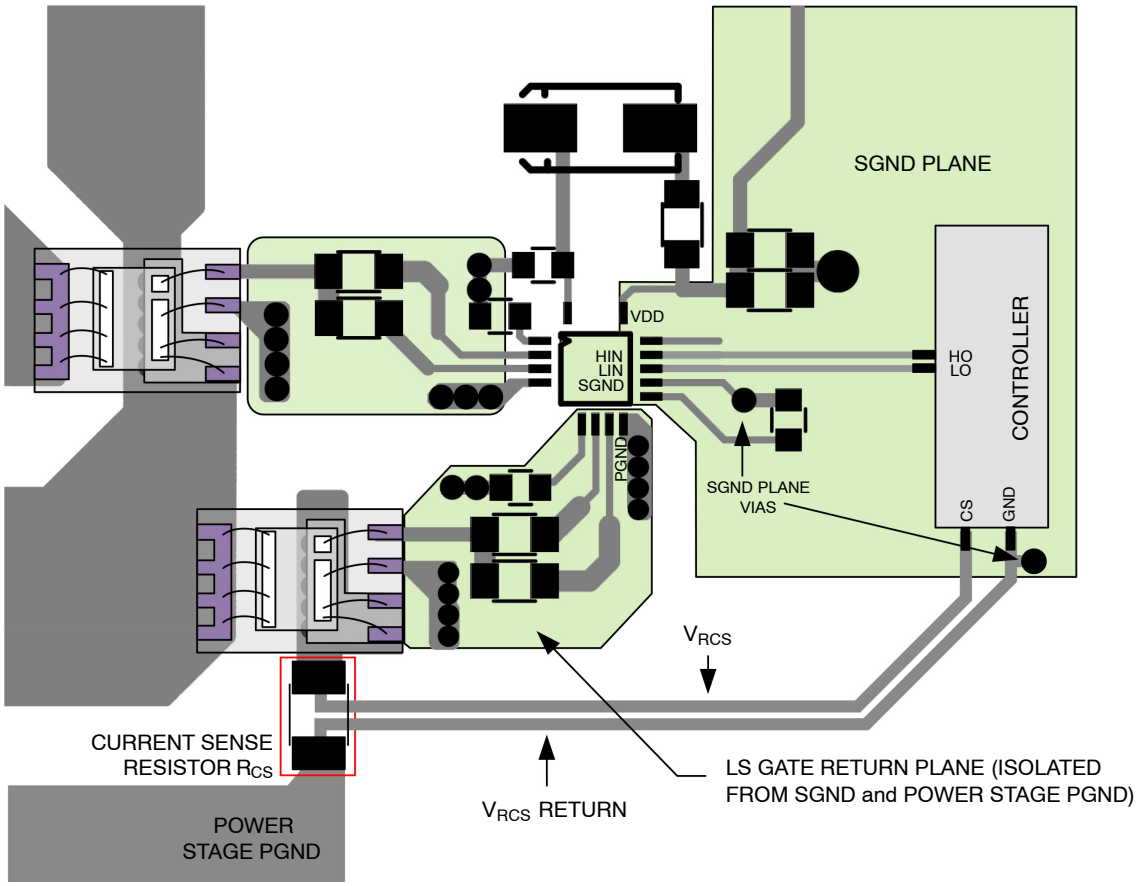

Figure 14. LS Gate Return Isolation and V_{RCS} Connection

SWITCHING PERFORMANCE VERIFICATION

The PCB design techniques illustrated in this document were used to layout a half−bridge power stage utilizing the NCP51820 driving GaNFETs.

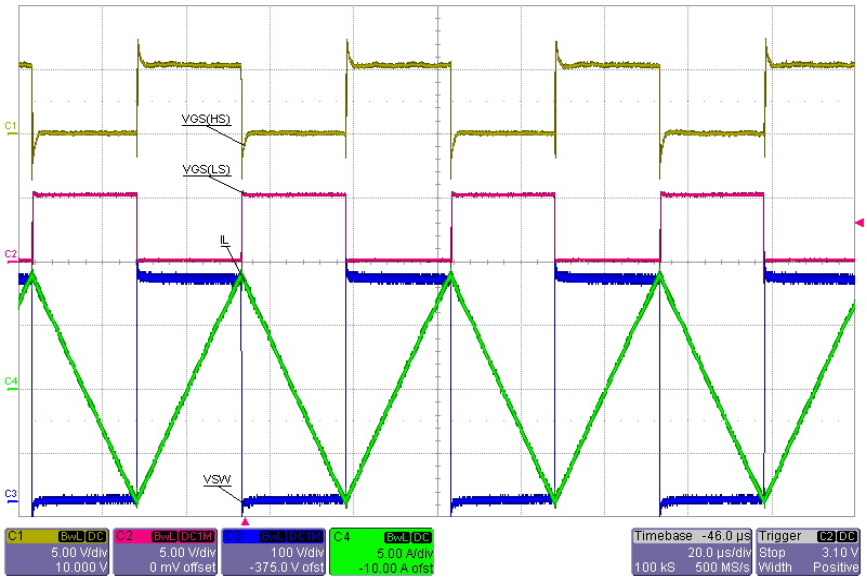

Figure 15. 650 V, 18 A, HEMT, GaNFETs, 350 V, 10 A_{PK}

Figure 15 shows steady state waveforms driving two 650 V, 18 A, 90 mΩ GaNFETs. Channel 1 (yellow) is the high−side gate−source voltage, channel 2 (red) is the low−side gate−source voltage, channel 3 (blue) is the switch−node voltage (low−side GaN V_{DS}) and channel 4 (green) is the inductor current. The slight overshoot and undershoot shown on the high−side gate−source voltage (channel 1, yellow) is a byproduct of using a high−voltage probe to measure a low−voltage floating signal, measured from gate to power, switch−node. A “truer” measurement of the gate−source voltage is shown by channel 2 (red) where the low−side GaNFET gate−source voltage is measured referenced from gate to PGND. Notice how sharp and clean the gate−drive edges are. Similarly, the switch−node voltage (channel 3, blue) shows no ringing, overshoot or undershoot.

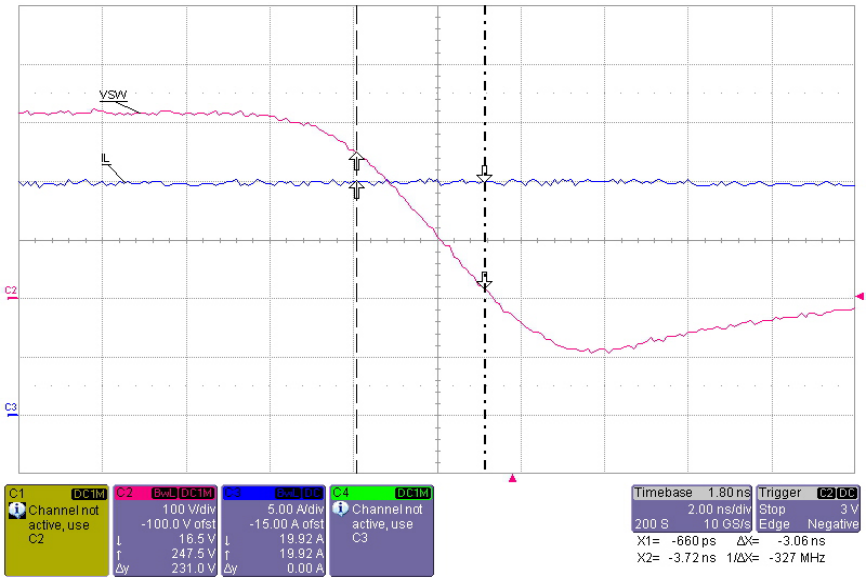

Figure 16. 600 V, 26 A, HEMT, GIT, GaNFETs, dV/dt = 75 V/ns, 320 V, 20 A_{PK}

The waveform shown in Figure 16 is a result of driving two HEMT, GIT, 600 V, 26 A, 56 mΩ GaNFETs which have higher current capability compared to the devices used in Figure 15. To achieve high dV/dt, a significant amount of drain current, I_D is required. For example, the measurement shown is taken at I_D = 20 A_{PK} resulting in a measured V_{DS}, dV/dt = 75 V/ns. The triangular, peak inductor current appears as DC only because of the time base (2 ns/div) necessary to make this measurement. The 100 V undershoot of the VSW waveform is the result of the measurement technique used to show the high dV/dt and is not actually present on the switch node.

CONCLUSION

The successful adoption of wide band gap semiconductors demands a greater awareness of the negative effects parasitic inductance and capacitance have in any high voltage, high frequency, PCB design. A thorough understanding of the importance of electrical return planes, shielding, current separation, isolation and careful routing are essential for deriving the maximum performance benefits offered from GaN technology. This paper has highlighted the most important PCB design guidelines that must be adopted for achieving a successful design using the NCP51820 for driving GaN power switches used in high−speed power topologies. These techniques have been validated with measured waveforms and shown to produce excellent results.

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