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AND9596/D

A Quick PCB Thermal Calculation for Power Electronic Devices with Exposed Pad Packages

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APPLICATION NOTE

INTRODUCTION

Thermal design of PCBs in electronic systems is critical to maintain device operating temperatures below specified limits. Although the predictions from full−field CFD simulations are accurate, the computational cost and model generation time could be fairly high. Thus, it is preferable to use a quick estimation tool to design a preliminary layout of PCBs with different heat−dissipating components.

Different from some of the existing cooling packaging options in the market today, ON Semiconductor's exposed−pad packaging solution offers standard lead−frame based board mounting in a fully encapsulated DFN and QFN molded package (see Figure 1), minimizing the thermal difference between the device and the PCB while offering near zero parasitic inductance with its layout friendly footprint.

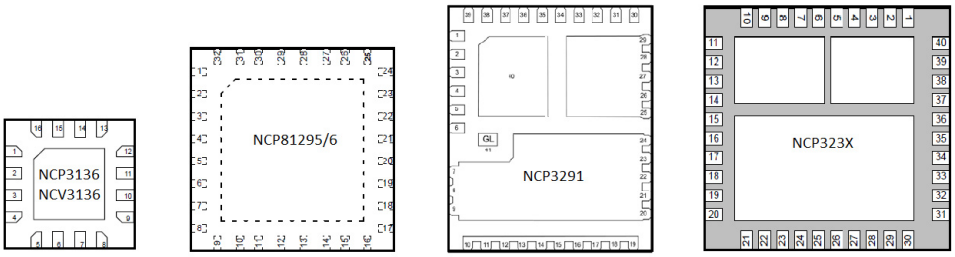


Figure 1. Typical Exposed Pad Packages for Power ICs (Top View)

THERMAL RESISTANCE MODELS FOR DEVICES AND BOARD

With thermal simulation software available today, it is possible to predict the temperature for a PCB board, even the entire system at any chosen location within that system. However many designers do not have access to thermal simulation software and thermal models for an entire PCB board, nor even would want to spend the time on a large number of lengthy computations for each set of possible cooling arrangements. So with this in mind, a fast estimation method of thermal dissipation for power electronic devices and the PCB board with thermal resistance parameters is proposed, which will rapidly provide the maximum permissible power generation by the semiconductor device for any combination of substrate and cooling situations.

For an exposed pad package placed on a PCB in natural convection (still air) environment (see Figure 2), the heat flow patterns from the package and environment can be drawn (see Figure 3). A significant point is that heat transfer efficiency from the PCB to the air is often the dominant effect on the overall temperature difference between the chip ("junction") and the air.

Heat dissipation happens mainly by conduction and convection. (Radiation can be significant in still air applications, but it is most often accommodated in simple analysis tools as an adjustment to the natural convection "film coefficient".) For handy reference, the thermal conductivities of a number of materials commonly found in electronics applications are listed in Table 1 [1]. The natural convection film coefficient "h" is an experimentally determined parameter whose value depends on all the variables influencing convection such as the surface geometry, the nature of fluid motion, the properties of the fluid, and the bulk fluid velocity. We can empirically take its

value as 15, 30, 45 W/(m^{2}K) for air velocities of 0, 1.0, 2.5 m/s [2]. (As noted above, for air velocities lower than 1 m/s, a significant fraction of this coefficient, as much as 35−40%, may actually be due to radiation, so surface emissivity may need to be considered. Shiny, metallic surfaces tend to have lower radiation contribution; matte−finish, non−metallic surfaces tend to have higher radiation contribution).

A four−resistor simplified equivalent thermal network diagram of the package and environment can be drawn (see Figure 4) with the package represented by a two−resistor model [3]. The die represents the junction node, whereas the case top and exposed pad in the bottom plate represent the “Case Node” and “Board Node” in the diagram, respectively.

Table 1. MATERIAL THERMAL CONDUCTIVITY PROPERTIES

Material	Thermal Conductivity (W/mK)
Silicon	145
Mold Compound	0.7
Lead Frame	277
Die Attach Epoxy	2.4
Copper	388
FR4 PCB	0.35
SnAgCu Solder	57.3
63Sn37Pb Colder	50

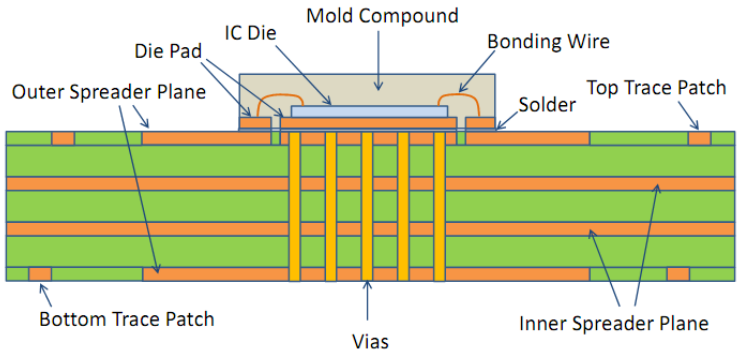


Figure 2. Exposed Pad Package on PCB

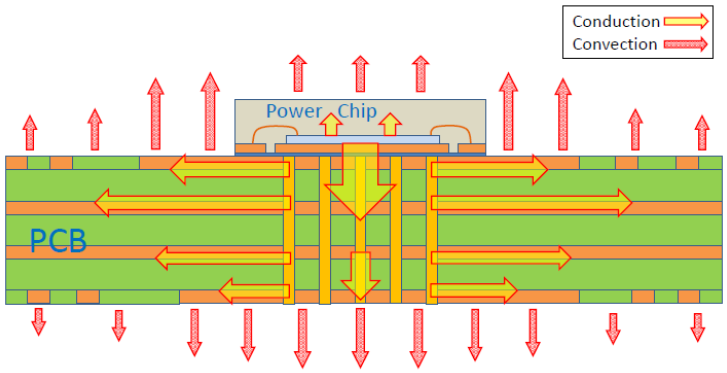


Figure 3. The Heat Flow Directions (Red Arrows)

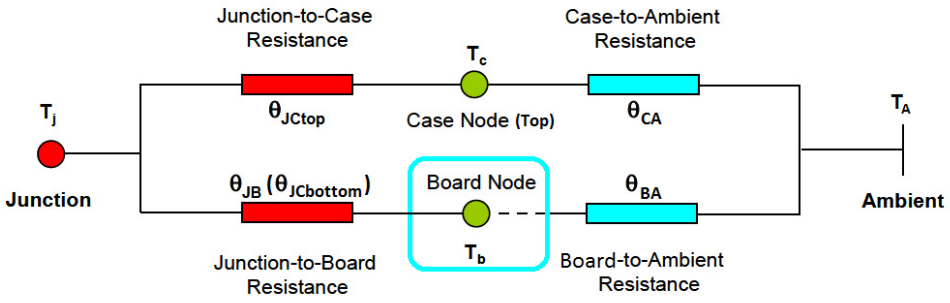


Figure 4. Equivalent Thermal Resistance Diagram of the Modified Two−resistor Model on a PCB

In many applications of exposed−pad packages, it is possible further to simplify this network from four resistors down to two resistors. Several reasonable approximations may be considered to justify this:

1. $T_B \approx T_{Cbottom}$ and $\theta_{JB} \approx \theta_{JCbottom}$
   The exposed pad packages are designed to inject heat directly into the copper plane of the board via bottom pad, and the effect of solder between the package pad and PCB pad is neglected due to its thin and with not−bad thermal conduction capability. So the bottom of the exposed pad can be taken to be the board temperature, that is $T_B \approx T_{Cbottom}$ and $\theta_{JB} \approx \theta_{JCbottom}$.
2. $\theta_{JCtop} >> \theta_{JB}$
   Take 6 × 6 mm QFN package of the NCP323X in a natural air environment, for example, we have $\theta_{JCtop} \approx 22$°C/W, while $\theta_{JB} \approx \theta_{JCbottom}$, (from approximation 1) is only 1.3°C/W.
   Thus $\theta_{JCtop} >> \theta_{JB}$.
3. $\theta_{CA} >> \theta_{BA}$
   Because convection resistances are inversely proportional to the exposed heat transfer surface area, as a general rule PCB convection resistance to air is much lower than case thermal resistance to air. For example, the total area of both sides of a 50 × 50 mm PCB is 5000 mm^2, whereas the surface area of a 6 × 6 mm QFN is only 36 mm^2. Clearly, $\theta_{CA} >> \theta_{BA}$.
4. $\theta_{JA} \approx \theta_{JB} + \theta_{BA}$
   Simple analysis of the four−resistor thermal network (Figure 4) shows that:

$$\theta_{JA} \approx (\theta_{JB} + \theta_{BA}) \parallel (\theta_{JCtop} + \theta_{CA}) \quad \text{(eq. 1)}$$

   From the 2nd and 3rd approximations above, $(\theta_{JB} + \theta_{BA}) >> (\theta_{JCtop} + \theta_{CA})$. Thus Eq.1 can be simplified as:

$$\theta_{JA} \approx \theta_{JB} + \theta_{BA} \quad \text{(eq. 2)}$$

   This means for exposed pad packages the dominant heat dissipation path is through the PCB via the bottom pad to ambient.

In summary, then, when θ_{JB} can be read from a datasheet, as, for example, the NCP81295, then only θ_{BA} remains to determine the total package/PCB system thermal resistance.

Another useful approximation with respect to the four−resistor package/PBC system is $T_J \approx T_C$.

Using the same 6 × 6 mm QFN example, the junction (T_J) to case−top (T_C), thence to ambient (T_A), thermal resistances can be calculated by conduction and convection principles. This yields the result of $\theta_{JC} \approx 22$°C/W vs. $\theta_{CA} \approx 1300$°C/W. By voltage−divider analogy, the difference ΔT_{JC} is thus only about (22/(1300 + 22)) = 1.7% of the total ΔT_{JA}. If the junction was 100°C above ambient, then the difference between junction and case would be less than 2°C.

Table 2. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	30	°C/W
Thermal Resistance, Junction−to−Top−Case	$R_{\theta JCT}$	50	°C/W
Thermal Resistance, Junction−to−Bottom−Case	$R_{\theta JCB}$	1.5	°C/W
Thermal Resistance, Junction−to−Board	$R_{\theta JR}$	1.5	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.5	°C/W

Calculation of Thermal Resistor of Board to Ambient (θ_{BA})

θ_{BA} represents the thermal resistance of the PCB, from the point at which the package puts heat into the board, to ambient. Different board sizes and properties have different θ_{BA} values. Consider a simple axisymmetric model of a PCB board as shown in Figure 5. What is particularly helpful about the axisymmetric model [4] is the outer edge of the board will be an isotherm by definition. In this model, the power IC chip can be taken as an axisymmetric heat source at the inner radius (the package), and at the exterior circular perimeter of the board we will specify a temperature rise above ambient, and also possibly a heat flow from the edge. Between the inner and outer radii, board properties are uniform, and heat is lost continuously to convection, characterized by a constant film coefficient. When the heat loss at the outer perimeter is zero, the thermal resistance of board to ambient is calculated from the circular fin formula:

The thermal resistance of board to ambient of this circle region is calculated from the circular fin formula:

$$\theta_{ab} = \frac{1}{2\pi akt\alpha} \times \frac{K_1(\alpha b)\, I_0(\alpha a) + I_1(\alpha b)\, K_0(\alpha a)}{I_1(\alpha b)\, K_1(\alpha a) - I_1(\alpha a)\, K_1(\alpha b)} \quad \text{(eq. 3)}$$

where:

- $I_0()$, $I_1()$ are the 1st kind modified Bessel functions, 0 and 1 order;
- $K_0()$, $K_1()$ are the 2nd kind modified Bessel functions, 0 and 1 order;
- k is the thermal conductivity of the PCB[15, 20, 50 W/(mK) for 2, 3, 8 oz board, respectively];
- t is PCB board thickness;
- $\alpha = \sqrt{(Nh)/(kt)}$, N is the number of surfaces cooled by h; h is the convection film coefficient (including radiation effect, if important);
- a and b are each the inner and outer radius, respectively.

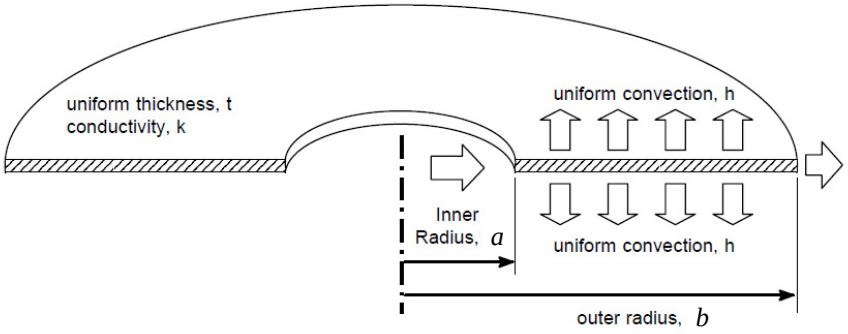


Figure 5. The Axisymmetric Model for Thermal Resistance of a PCB

While this formula may appear intimidating, Bessel functions are available in popular spreadsheet software programs. The equivalent thermal conductivity k of the board in any given application depends on the user's specific board design. It depends on the thickness/size/layer−number of copper plane, size/number of thermal vias, and copper plane pattern. The detailed modeling for thermal conductivity of the board is shown in Figure 6. It can be taken for equivalent thermal conductivity k calculations.

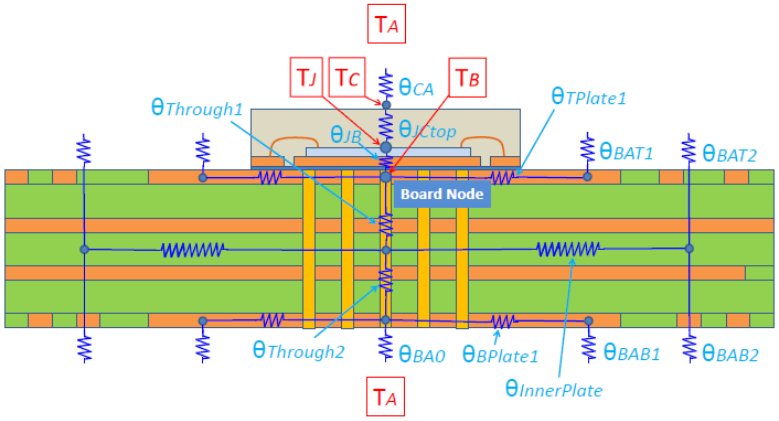


Figure 6. Thermal Resistance of 4−layer PCB to Ambient

With the guidance of above uniform axisymmetric annular board model, the total board can be divided into three annular regions (see Figure 7) according to board characteristics (see both Figure 6 and 8): Chip Region, Outer Plane Region and Effective Board Size Region.

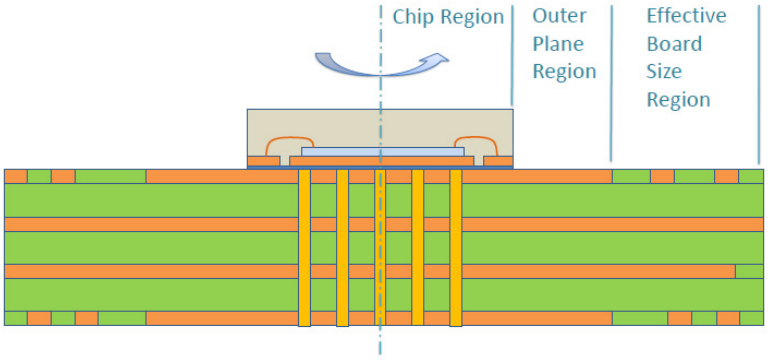


Figure 7. The Three Regions for Thermal Resistance of a PCB

Due to the adoption of the axisymmetric model, one must transform between actual board size (typically rectangular) and effective (circular) board size, based on ensuring that the total area is the same.

For a board with a inner copper plane directly connected to the power IC and its exposed thermal pad by thermal vias (see Figure 8.a), the effective board size is

$$\text{EffectiveBoardSize} = \frac{2}{\sqrt{\pi}} \times \sqrt{A} \qquad \text{(eq. 4)}$$

where A is the area of the projected pattern of all copper planes directly connected to the power IC's exposed thermal pad by thermal vias.

Similarly, there also has a convertion for outer copper plane size

$$\text{OuterCopperPlaneSize} = \frac{1}{\sqrt{\pi}} \times \sqrt{0.5 \times A} \qquad \text{(eq. 5)}$$

where A is the total area both top and bottom surface copper planes directly connected to power IC.

For chip region, the effective size is

$$\text{ChipRegionSize} = \frac{1}{\sqrt{\pi}} \times \sqrt{A_{chip}} \qquad \text{(eq. 6)}$$

where A_{chip} is the chip area of power IC.

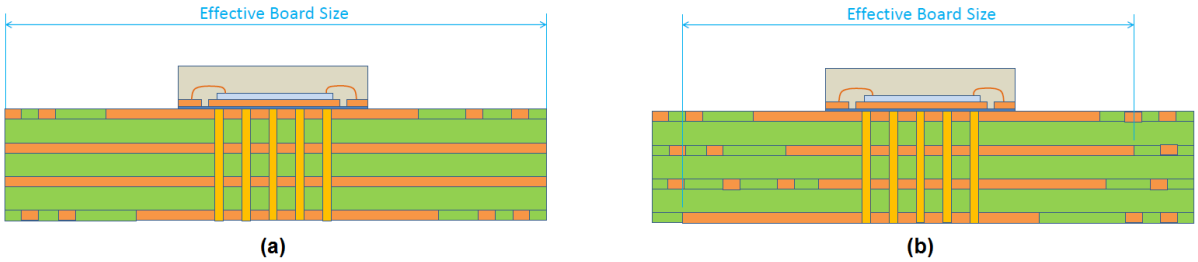


Figure 8. The Three Regions for Thermal Resistance of a PCB

Each annular region's convection and radiation resistance of the board to ambient can be calculated by Eq.3. Then we get thermal resistors of board node to ambient for three regions (see Figure 6).

For chip region:

$$\theta_{BA(Chip)} = \theta_{Through1} + \theta_{Through2} + \theta_{BA0} \qquad \text{(eq. 7)}$$

For outer plane region:

$$\theta_{BA(Outplane)} = (\theta_{TPlate1} + \theta_{BAT1}) \parallel \left(\theta_{Through1} + \theta_{Through2} + \theta_{BPlate1} + \theta_{BAB1}\right) \qquad \text{(eq. 8)}$$

For effective board size region:

$$\theta_{BA(EffectiveBoard)} = \theta_{Through1} + \theta_{InnerPlate} + \theta_{BAT2} \parallel \theta_{BAB2} \qquad \text{(eq. 9)}$$

The total thermal resistors of board to ambient is a combination of three above resistances, considering them to be a parallel resistance network from board node to ambient (see Figure 6), i.e.

$$\theta_{BA} = \theta_{BA(Chip)} \parallel \theta_{BA(Outplane)} \parallel \theta_{BA(EffectiveBoard)} \quad \text{(eq. 10)}$$

Taking an 8−layer (1 oz each) PCB with a 5×5 Q/DFN device exposed to natural convection as an example, the calculated thermal resistance vs. effective board size is shown in Figure 8, in which the outer copper plane size is normalized with chip size, ie. normalized outer copper plane size factor:

$$F = \frac{outercopperplanesize}{chipsize} \quad \text{(eq. 11)}$$

Figure 8.a is the curve chart generated according to a QFN5X5 chip PCB (Evaluation Board for NCP81295) characteristics factor. The charts in Figure 9 represent different factors affecting thermal performance, such as thickness/size/layer−number of copper planes, size/number of thermal vias, and copper plane size. The user can read the closest curve for estimating their value according to their board characteristics and effective size when using a 5×5 Q/DFN device in their project. Similar charts for other package devices are listed in Appendices.

Finally, combining package and board contributions according to Eq.10, the overall thermal resistance of the system can be obtained. When the power dissipation is known, the user can estimate the chip temperature rise.

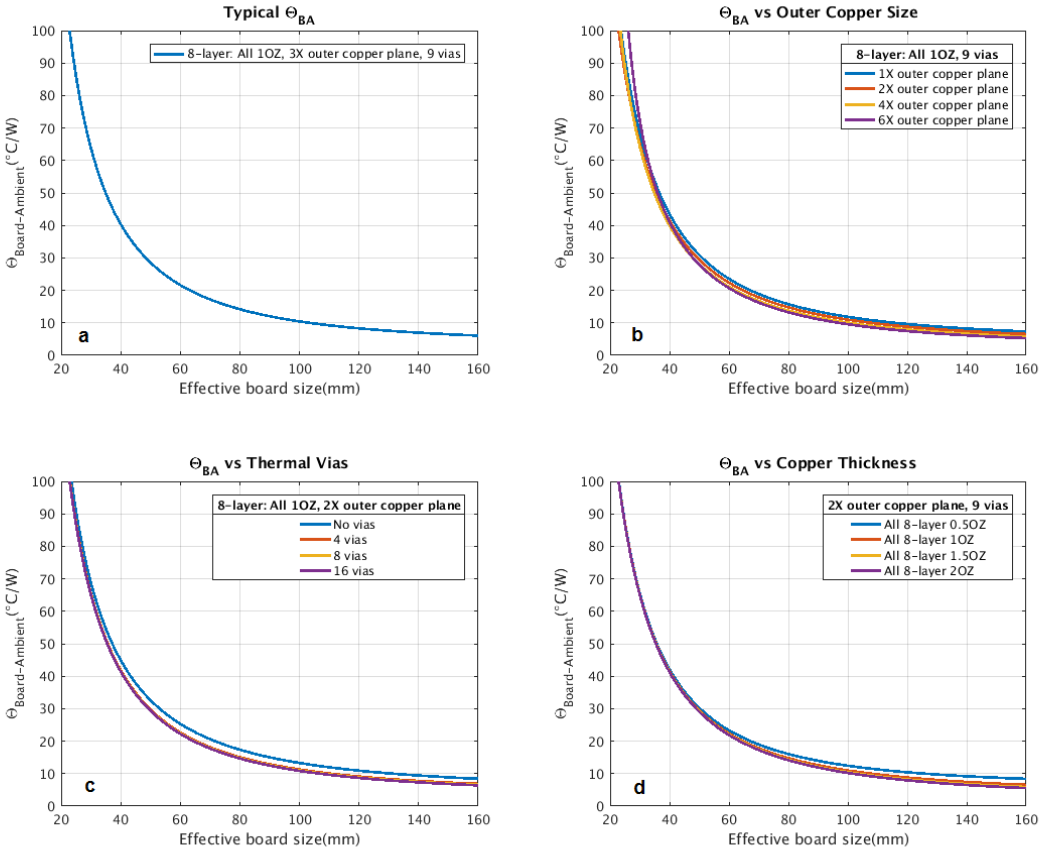


Figure 9. Thermal Resistance θ_{BA} of 8−layer PCB with D/QFN5X5 Chip (Natural Air)

Calculation Example 1: NCP81295/6 EVB

The NCP81295/6 are both 50 A, electronically re−settable, in−line fuses for use in server−based, high−current, 12 V hot−swap applications. The NCP81295/6 offers a very low 0.65 mΩ integrated MOSFET to reduce solution size and minimize power loss. It also integrates a highly accurate current sensor for monitoring and overload protection.

Their EVB board (see Figure 10) has only a partial copper plane directly connected to the exposed thermal pad by thermal vias.

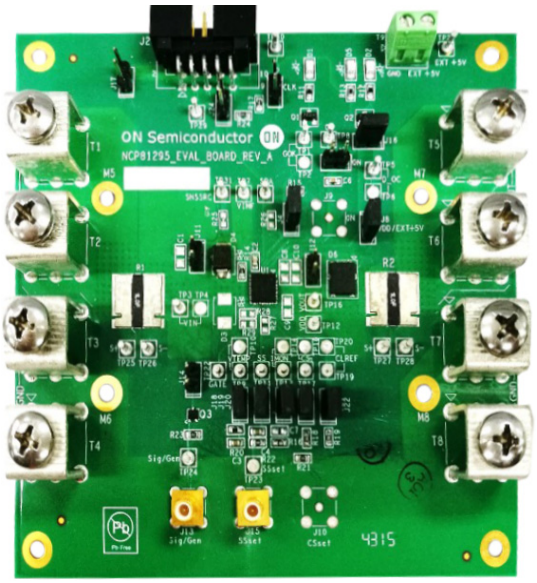


Figure 10. NCP81295/6 EVB

The Board information is below:

- Board Size: 100 × 100 mm
- Board thickness: 1.6 mm
- Layers: 8−layer PCB (All 1 OZ copper layers)
- PIC: NCP81295 (QFN5X5)

The test condition is with 50 A stable current load at 25°C. The power loss is about 1.65 W. The EVB's thermal IR image is below (see Figure 11). The top case temperature of NCP81295 is 67.1°C and the temperature rise is about 42.1°C.

Figure 11. IR image of NCP81295/6 EVB

The NCP81295/6 EVB board has following characteristic after its layout evaluation. The effective size is 60 mm and the outer copper plane size is 3X chip−size (the normalized outer copper plane size factor is 3).

Figure 8.a a matches the NCP81295/6 EVB condition. θ_{BA} of NCP81295/6 EVB can be read from Figure 8.a. The zoom−in θ_{BA} curve near 60 mm effective size is shown in Figure 12.

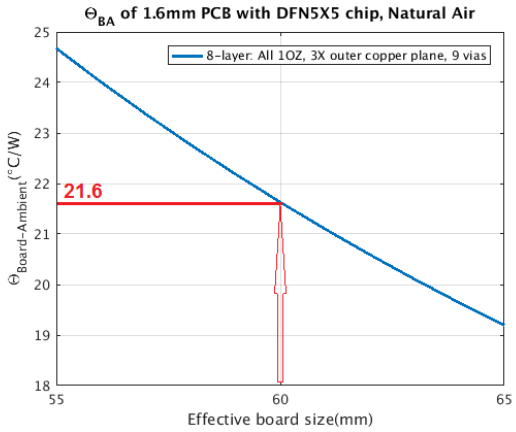


Figure 12. θ_{BA} of NCP81295/6 EVB

$$\theta_{BA} = 21.6°C/W \quad \text{(eq. 12)}$$

θ_{JC} is 1.5°/W from datasheet. Then get θ_{JA}

$$\theta_{JA} = \theta_{JC} + \theta_{BA} = 23.1°C/W \quad \text{(eq. 13)}$$

Then the calculated junction temperature (which we have already approximated to be the same as the case top temperature) of the NCP81295 on EVB board is below:

$$T_C = T_A + 1.65 \times 23.1 = 63.1°C/W \quad \text{(eq. 14)}$$

also, in passing

$$\Delta T_{JA} = 1.65 \times 23.1 = 38.1°C/W \quad \text{(eq. 15)}$$

The calculated temperature is close to the test result. The small difference of 4 °C is likely the effect of the two big shunt resistors, whose power dissipation heats the board in addition to the heating caused by the NCP81295 itself. This effects can be superimposed when the system is approximately linear.

Calculation Example 2: NCP3231 EVB

The NCP3231 is a high current, high efficiency, voltage−feed−forward voltage−mode synchronous buck converter which operates from 4.5 V to 18 V input and generates output voltages down to 0.6 V at up to 25 A DC load or 30 A instantaneous load.

The EVB board (see Figure 13) is full complete copper plane directly connected to the exposed thermal pad is by thermal vias.

The Board information is below:

- Board Size: 75 × 73 mm
- Board thickness: 1.6 mm
- Layers: 6−layer PCB (All 2 OZ copper layers)
- PIC: NCP3231 (QFN6X6)

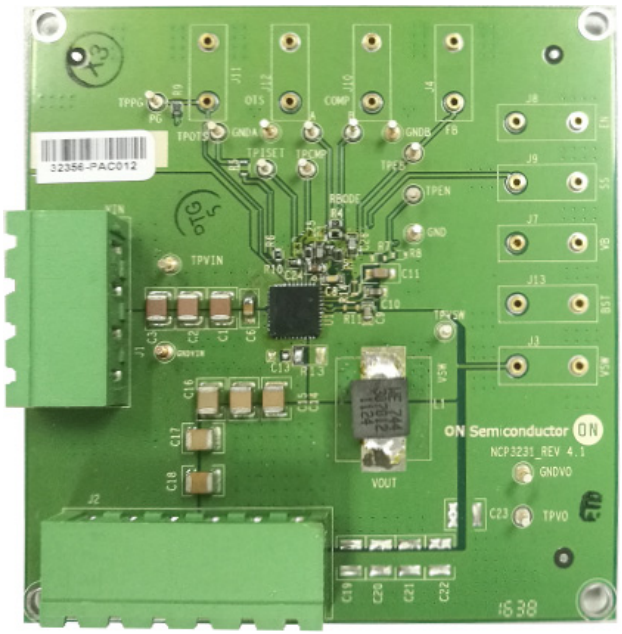


Figure 13. NCP3231 EVB

The test condition is converting 9 V to 1 V at 1 MHz frequency with 15 A stable current load at 20°C. The power loss is about 2.52 W. The EVB's thermal IR image is below (see Figure 14). The top case temperature of NCP3231 is 54°C and the temperature rise is about 34°C.

Figure 14. IR Image of NCP3231 EVB

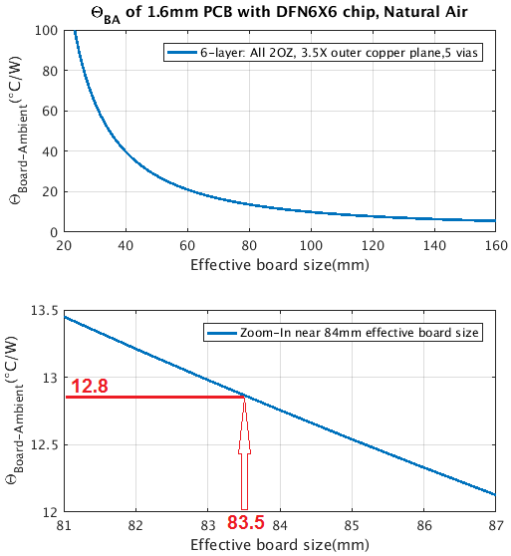


Figure 15. θ_{BA} of NCP3231 EVB

The NCP3231 EVB board has the following characteristic based on its layout evaluation. The effective size is 83.5 mm and the outer copper plane size is 3.5X chip−size (the normalized outer copper plane size factor is 3.5). Figure 15 is the curve chart generated according to this NCP3231 EVB condition. of NCP3231 EVB can be read from Figure 14:

$$\theta_{BA} = 12.8°C/W \quad \text{(eq. 16)}$$

θ_{JC} is 1.0°C/W from datasheet. Then get θ_{JA}

$$\theta_{JA} = \theta_{JC} + \theta_{BA} = 13.8°C/W \quad \text{(eq. 17)}$$

So the calculated junction temperature of the NCP3231 on the EVB board is found from:

$$T_C = T_A + 2.52 \times 13.8 = 54.8°C \quad \text{(eq. 18)}$$

also, in passing

$$\Delta T_{JA} = 2.52 \times 13.8 = 34.8°C \quad \text{(eq. 19)}$$

The calculated temperature is close to test result.

Further Discussion

Based on the earlier approximations for the NCP3231 EVB, the difference between T_C and T_J is only about 1.7% of total ΔT_{JA}. So in this example, the difference is only

$$\Delta T_{JC} = 1.7\% \times \Delta T_{JA} = 0.6°C \quad \text{(eq. 20)}$$

Sometimes we want to estimate the die temperature based on package case−top temperature measurement. We also can adopt the thermal characterization parameter Ψ_{JT} (defined in JESD 51−2 as junction−to−case−top for plastic packages) to describe a temperature difference in proportion to total device power dissipation (in contrast with an actual heat flow along a known path). The term Ψ_{JT} is a concession to the reality that it's easy to measure temperature and really difficult to measure heat flux, especially on miniscule semiconductor devices.

Sometimes we want to estimate die the temperature based on package top temperature measurement. We also can adopt the thermal characterization parameter Ψ to describe the temperature rising with total device power dissipation. The term is concession to the reality that it's easy to measure temperature and really difficult to measure heat flux, especially on miniscule semiconductor devices.

Taking the system as a whole (see Figure 4), the junction−to−case(top) thermal characterization parameter can be written as following:

$$\psi_{JC} = \frac{T_J - T_C}{P_{Totalloss}} = \frac{\theta_{JCtop}}{1 + \frac{\theta_{JCtop} + \theta_{CA}}{\theta_{JB} + \theta_{BA}}} \quad \text{(eq. 21)}$$

Taking the previous calculated NCP3231 EVB data into above formula, we get Ψ_{JC} = 0.224°C/W for the NCP3231 on its EVB. The junction temperature is gotten again

$$T_J = T_C + P_{Totalloss} \times \psi_{JC} = 54.6°C \quad \text{(eq. 22)}$$

What we need be aware of is that even when the two−package thermal resistances θ_{JB} and θ_{JCtop} are absolutely and truly constant, the corresponding Ψ_{JC} is not constant because it depends on the board characteristics too. Anyway, with Ψ_{JT}, the user can make quick die temperature estimates based on package case−top temperature measurements and knowledge of the total power dissipation.

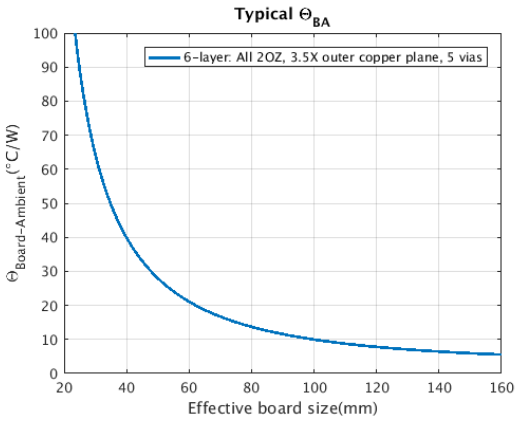
Summary

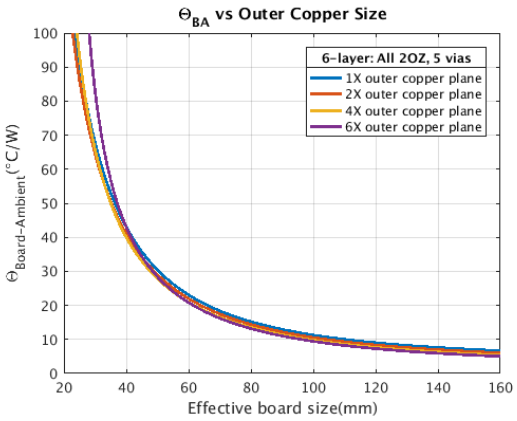
The present methodology does not rely on accurate CFD modeling. It can be extended to forced convection and other PCB constructions simply by adjusting the film coefficient values and knowledge of how the board going to be constructed (e.g. number and thickness of metal layers). A calculator using this methodology can be developed as a stand−alone or a web−based application, and would be valuable when initially laying out multiple components on PCB, prior to undertaking a computationally expensive detailed CFD simulation of the entire PCB with all components.

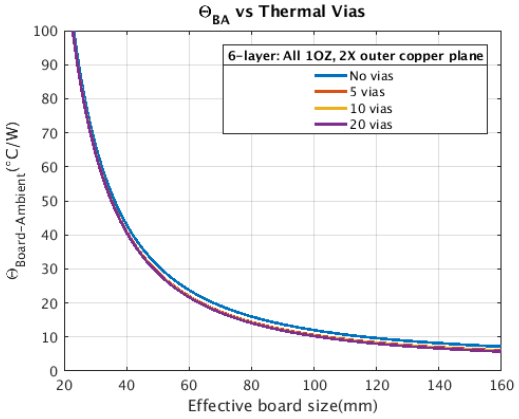
Acknowledgments

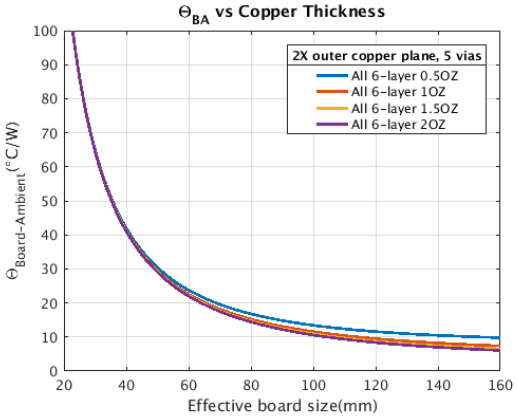
The author would like to acknowledge the generous help of two members of the Corporate Technical Ladder: Roger P. Stout and Yong Liu from ON's Corporate Research and Development division.

APPENDIX A: Θ_{BA} OF 6−LAYER PCB WITH D/QFN6X6 CHIP

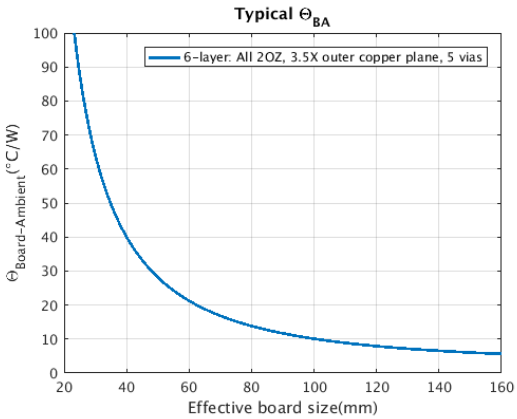


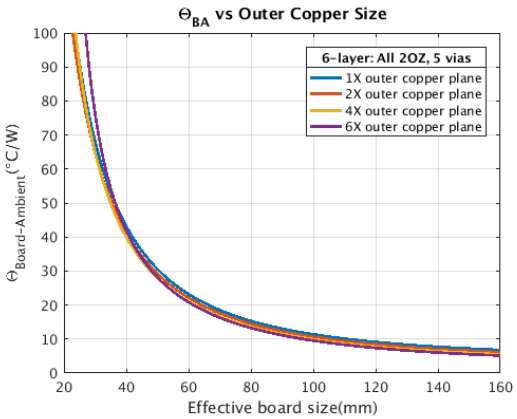


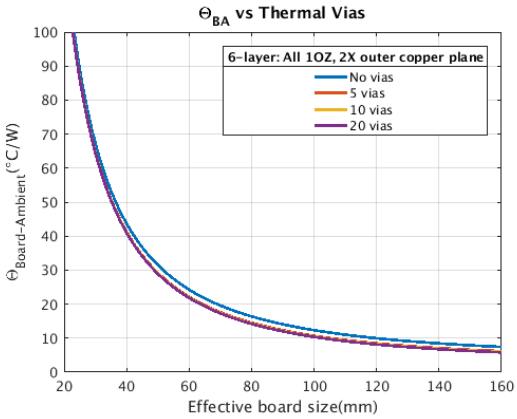


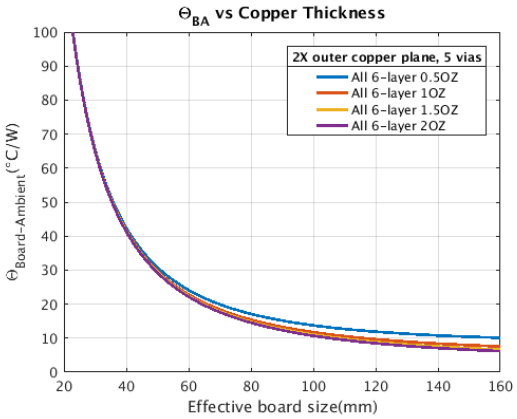


APPENDIX B: Θ_{BA} OF 6−LAYER PCB WITH D/QFN5X6 CHIP

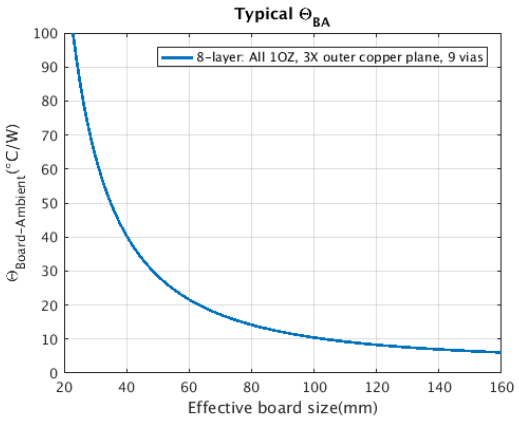


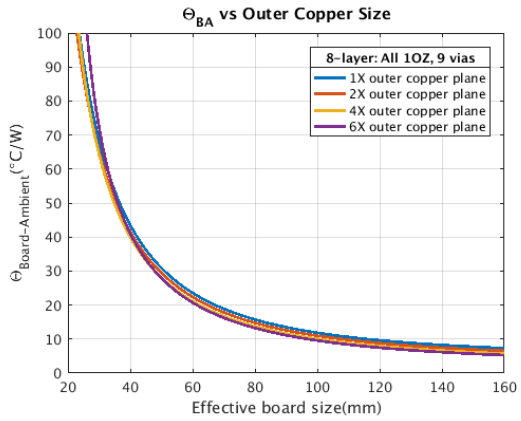


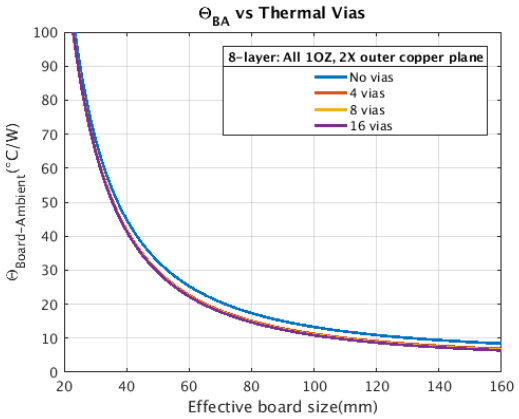


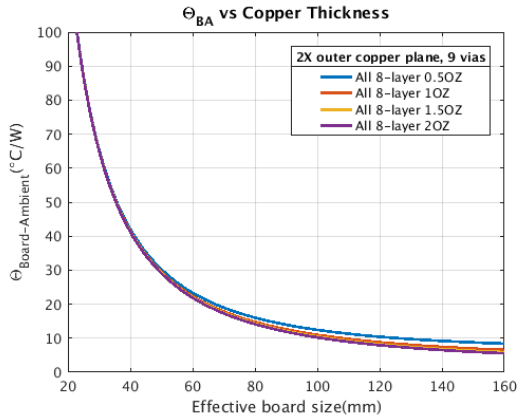


APPENDIX C: Θ_{BA} OF 8−LAYER PCB WITH D/QFN5X5 CHIP

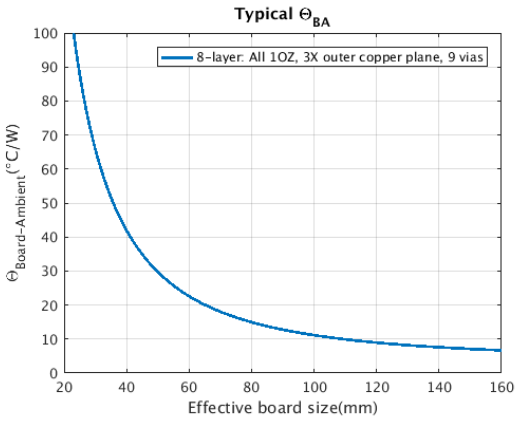


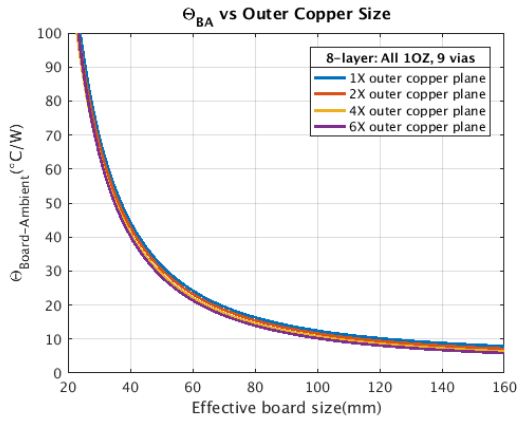


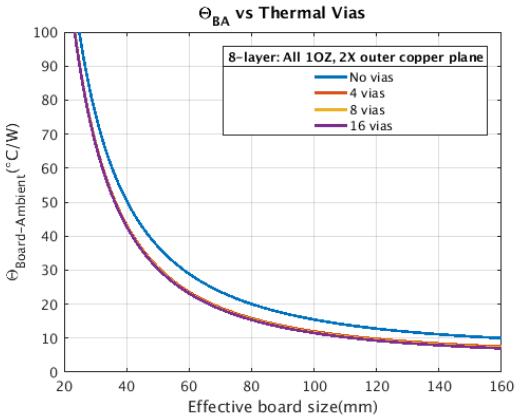


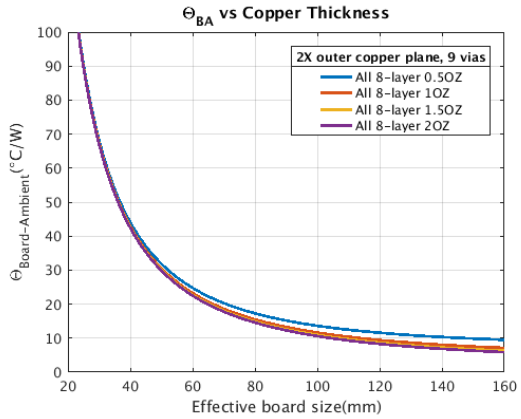


APPENDIX D: Θ_{BA} OF 8−LAYER PCB WITH D/QFN3X3 CHIP









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