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Buck Converter External Components Selection

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APPLICATION NOTE

The Buck Converter is used in SMPS (switched mode power supply) circuits when the DC output voltage has to be lower than the DC input voltage. It is extensively used when high efficiency is required, especially in battery supplied applications where it improves battery life and reduces power dissipation.

This document describes step by step how to select the external components that are used by the buck converter. Although generally applicable, this selection method is in particular of interest for the members of the NCP63xx and NCV63xx family.

BUCK CONVERTER BASICS

A synchronous buck converter is comprised of two power MOSFETs, an inductor and input/output capacitors arranged as depicted in the Figure 1. The MOSFETs maintain energy level in the inductor, and the on/off control is synchronizing to regulate the output voltage.

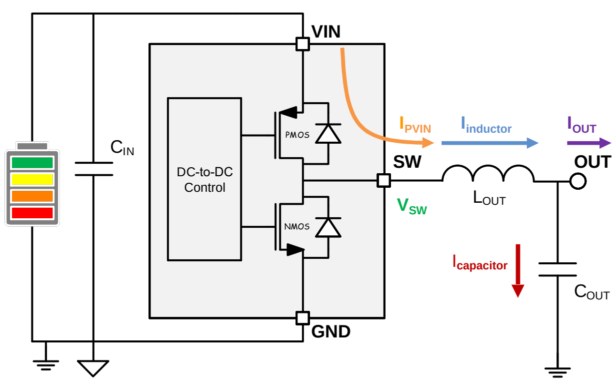


Figure 1. Synchronous Buck Converter

The PMOS connected between VIN and SW allows charging the LC filter: when ON, it transfers energy from input to output. The NMOS is off during this phase. When the PMOS turns off, the NMOS is activated and the energy stored in the inductor is provided to the output.

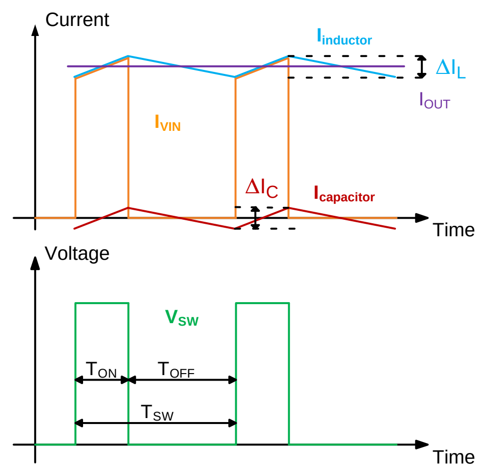


Figure 2. Synchronous Buck Converter Waveforms

The PMOS is commonly named High Side Switch (HSS) and the NMOS is Low Side Switch (LSS) or synchronous rectifier.

Figure 2 illustrates the voltage and current waveforms of the buck converter. This will help to understand the rest of this document

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{T_{ON}}{T_{SW}} = T_{ON} \cdot F_{SW}$$

$$T_{OFF} = \frac{1 - D}{F_{SW}} \quad \text{and} \quad T_{ON} = \frac{D}{F_{SW}} \qquad \text{(eq. 1)}$$

COMPONENTS SELECTION

Inductor Selection

Let's start with the governing inductor current/voltage equation to obtain relation between L and ΔI_L:

$$V_L = L \cdot \frac{dI_L}{dt}$$

During on-time, assuming ideal HSS, the voltage across the inductor is $(V_{IN} - V_{OUT})$, so we have

$$V_{LON} = \left(V_{IN} - V_{OUT}\right) = L \cdot \frac{dI_L}{dt_{ON}} = L \cdot \frac{\Delta I_L}{T_{ON}}$$

$$= L \cdot \frac{\Delta I_L}{D \cdot T_{SW}} \Rightarrow L = \frac{D\left(V_{IN} - V_{OUT}\right)}{\Delta I_L \cdot F_{SW}}$$

During off-time, assuming ideal LSS, the inductor voltage is V_{OUT}, so we have

$$V_{LOFF} = L \cdot \frac{dI_L}{dt_{OFF}} = L \cdot \frac{\Delta I_L}{T_{OFF}} = L \cdot \frac{\Delta I_L}{1 - D} \cdot F_{SW}$$

$$\Rightarrow L = \frac{V_{OUT}(1 - D)}{\Delta I_L \cdot F_{SW}}$$

Form the two previous equations we can extract:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Finally the inductance corresponding to a given current ripple ΔI_L is:

$$L = \frac{\left(V_{IN} - V_{OUT}\right) \cdot V_{OUT}}{\Delta I_L \cdot F_{SW} \cdot V_{IN}} \qquad \text{(eq. 2)}$$

Note that the inductance of the inductor is selected such that the peak-to-peak ripple current ΔI_L is approximately 20% to 50% of the maximum output current I_{OUT_MAX}. This provides the best trade-off between transient response and output ripple.

The selected inductor must have a saturation current rating higher than the maximum peak current which is calculated by:

$$I_{L\_SAT} = I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

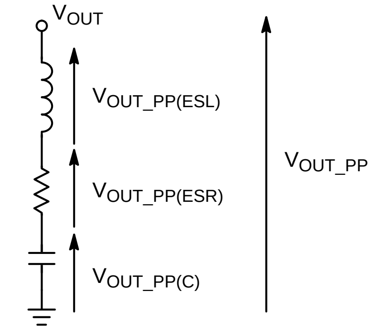
Moreover the inductor must also have a high enough current rating to avoid self-heating effect. A low DCR is therefore preferred to limit IR losses and optimize the total efficiency.

Output Capacitor Selection

The output capacitor selection is determined by the output voltage ripple and the load transient response requirement.

Ripple

For a given peak-to-peak ripple current ΔI_L in the inductor of the output filter, the output voltage ripple across the output capacitor V_{OUT_PP} is the sum of three components as shown below:



$$V_{OUT\_PP} = V_{OUT\_PP(ESL)} + V_{OUT\_PP(ESR)} + V_{OUT\_PP(C)}$$

With

- $V_{OUT\_PP(C)}$ is the ripple voltage of the capacitor
- $V_{OUT\_PP(ESR)}$ is the ripple voltage due to the ESR of the capacitor
- $V_{OUT\_PP(ESL)}$ is the ripple voltage generated by the ESL of the capacitor

$V_{OUT\_PP(C)}$ Equation:

From the Figure 2, we can extract the inductor and capacitor currents, and illustrate the charge of the capacitor:

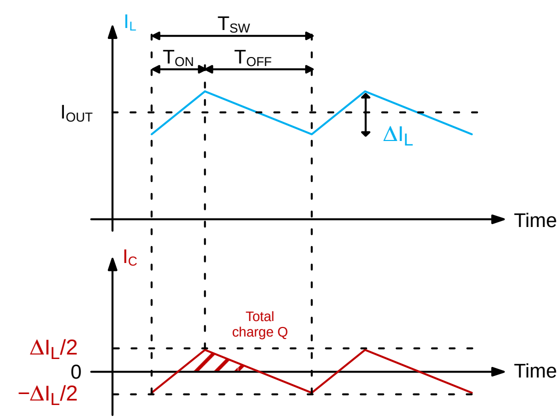


Figure 3. Inductor and Capacitor Current Waveforms

We can see that the capacitor current waveform is the same as the inductor current waveform, but without the I_{OUT} component.

The basic capacitor current/voltage equation is:

$$I_C = C \cdot \frac{dV_C}{dt} \Rightarrow dt \cdot I_C = C \cdot dV_C$$

And the relation between charge and capacitor is:

$$Q = C \cdot dV_C$$

Knowing that the charge is the area of the positive portion of the $I_C(t)$ waveform (in red in Figure 3). This area can be easily expressed as the area of a triangle:

$$Q = \frac{1}{2} \cdot \left(\frac{\Delta I_L}{2}\right) \cdot \left(\frac{T_{SW}}{2}\right) = \frac{\Delta I_L}{8 \cdot F_{SW}}$$

So

$$V_{OUT\_PP(C)} = \frac{\Delta I_L}{8 \cdot C \cdot F_{SW}} \qquad \text{(eq. 3)}$$

$V_{OUT\_PP(ESR)}$ Equation:

The $V_{OUT\_PP(ESR)}$ due to the ESR can be extract easily thanks to the IxR formula: The ESR can be modeled as a resistor in series with the capacitor

$$V_{OUT\_PP(ESR)} = \Delta I_L \cdot ESR \qquad \text{(eq. 4)}$$

$V_{OUT\_PP(ESL)}$ Equation:

Again, let’s start with the governing inductor current/voltage equation:

$$V_{ESL} = L_{ESL} \cdot \frac{dI_{L_{ESL}}}{dt} \Rightarrow V_{ESL} = L_{ESL} \cdot \Delta I_L \cdot \left(\frac{1}{T_{ON}} + \frac{1}{T_{OFF}}\right)$$

$$= L_{ESL} \cdot \Delta I_L \frac{F_{SW}}{D \cdot (1 - D)}$$

By using $D = \frac{V_{OUT}}{V_{IN}}$ and $\Delta I_L = \frac{(V_{IN} - V_{OUT})V_{OUT}}{L \cdot F_{SW} \cdot V_{IN}}$ we have

$$V_{OUT\_PP(ESL)} = L_{ESL} \cdot \frac{V_{IN}}{L} \qquad \text{(eq. 5)}$$

In applications with all ceramic output capacitors, the main ripple component of the output ripple is $V_{OUT\_PP(C)}$. The minimum output capacitance can be calculated based on a given output ripple requirement $V_{OUT\_PP(C)}$ in continuous current mode (CCM):

$$C_{PP} = \frac{\Delta I_L}{8 \cdot V_{OUT\_PP(C)} \cdot F_{SW}} \qquad \text{(eq. 6)}$$

Example:

3 MHz DCDC, V_{IN} = 3.3 V, V_{OUT} = 1.1 V, L = 0.470 μH

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})V_{OUT}}{L \cdot F_{SW} \cdot V_{IN}}$$

$$= \frac{(3.3 - 1.1)\,1.1}{0.00000047 \cdot 3000000 \cdot 3.3} = 520\ \text{mA}$$

With 10 mV of desired output ripple, the minimum output capacitor will be:

$$C_{PP} = \frac{\Delta I_L}{8 \cdot V_{OUT\_PP(C)} \cdot F_{SW}}$$

$$= \frac{0.520}{8 \cdot 0.01 \cdot 3000000} = 2.2\ \mu\text{F}$$

Load Transient

For the estimation of the capacitor during load transient, the starting point is that the total energy of the output stage has to be constant during the transition.

The total energy of the output stage is:

$$E = E_C + E_L = \frac{1}{2}C \cdot V_C^{\,2} + \frac{1}{2}L \cdot I_L^{\,2}$$

When the load current changes from load to no load, this will introduce temporary an increase of the output voltage (this is generally named output overshoot V_{OV}).

The energy with load is:

$$E = \frac{1}{2}C \cdot V_{OUT}^{\,2} + \frac{1}{2}L \cdot I_{LPEAK}^{\,2}, \quad I_{LPEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

The energy without load is:

$$E = \frac{1}{2}C \cdot \left(V_{OUT} + V_{OV}\right)^2$$

The energy preceding the load change has to be equal to the energy after the load change:

$$\frac{1}{2}C \cdot V_{OUT}^{\,2} + \frac{1}{2}L \cdot I_{LPEAK}^{\,2} = \frac{1}{2}C\left(V_{OUT} + V_{OV}\right)^2$$

Finally

$$C_{LT} = \frac{L \cdot I_{LPEAK}^{\,2}}{\left(V_{OUT} + V_{OV}\right)^2 - V_{OUT}^{\,2}} \qquad \text{(eq. 7)}$$

Example:

3 MHz DCDC, V_{IN} = 3.3 V, V_{OUT} = 1.1 V, L = 0.470 μH.

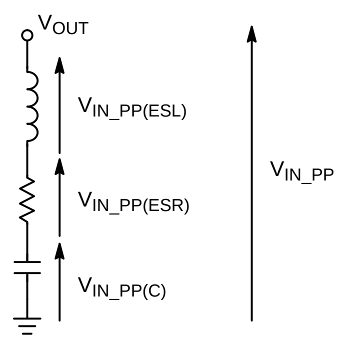
3 A load transient, 50 mV overshoot:

$$C_{LT} = \frac{L \cdot I_{IPEAK}^{\,2}}{\left(V_{OUT} + V_{OV}\right)^2 - V_{OUT}^{\,2}}$$

$$= 0.00000047 \cdot \frac{(3 + 0.26)^2}{(1.1 + 0.05)^2 - 1.1^2} = 44\ \mu\text{F}$$

Input Capacitor Selection

One of the input capacitor selection requirements is the input voltage ripple. For a given output current I_{OUT}, the input voltage ripple across the output capacitor V_{IN_PP} is, like the output capacitor, the sum of three components as shown below:



$$V_{IN\_PP} = V_{IN\_PP(ESL)} + V_{IN\_PP(ESR)} + V_{IN\_PP(C)}$$

With:

- $V_{IN\_PP(C)}$ is the ripple voltage of the capacitor
- $V_{IN\_PP(ESR)}$ is the ripple voltage due to the ESR of the capacitor
- $V_{IN\_PP(ESL)}$ is the ripple voltage generated by the ESL of the capacitor

$V_{IN\_PP(C)}$ Equation:

The current flowing into the input capacitor is:

- The difference between input and inductor currents during the ON-time
- The input current during the OFF-time

During the OFF-time, the capacitor is charged with current I_{IN}, while during the ON-time it is discharged. In steady state the charge and discharge of the capacitor is equal and generates the input voltage ripple.

By using the governing capacitor current/voltage equation during OFF-time we have:

$$I_{IN} = C_{IN} \cdot \frac{dV_C}{dt} = C_{INPP} \cdot \frac{V_{IN\_PP(C)}}{T_{OFF}} \Rightarrow C_{INPP} = \frac{I_{IN} \cdot T_{OFF}}{V_{IN\_PP(C)}}$$

With $I_{IN} = D \cdot I_{OUT}$ and $T_{OFF} = \frac{1 - D}{F_{SW}}$

The minimum input capacitance with respect to the input ripple voltage $V_{IN\_PP(C)}$ is:

$$C_{INPP} = \frac{I_{OUT}(D - D^2)}{V_{IN\_PP(C)} \cdot F_{SW}} \qquad \text{(eq. 8)}$$

$V_{IN\_PP(ESR)}$ Equation:

The $V_{IN\_PP(ESR)}$ due to the ESR can be extract easily thanks to the IxR formula: The ESR can be modeled as a resistor in series with the capacitor, and the I_{IN} extracted from I_{OUT} (see Figure 4). Generally the ripple current is low compare to output current, so the input current is assimilated to square current (0 to/from I_{OUT})

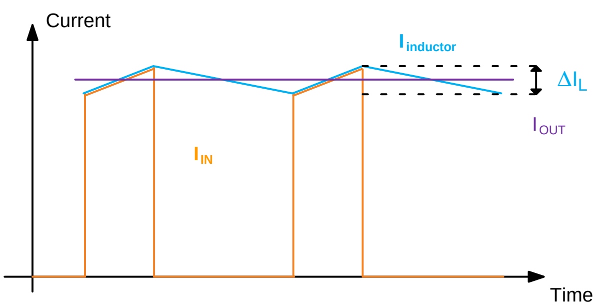


Figure 4. Input and Output Current Waveforms

$$V_{IN\_PP(ESR)} = \Delta I_{IN} \cdot ESR$$

So

$$V_{IN\_PP(ESR)} = I_{OUT} \cdot ESR \qquad \text{(eq. 9)}$$

$V_{IN\_PP(ESL)}$ Equation:

Again, let's start with the governing inductor current/voltage equation:

$$V_{ESL} = L_{ESL} \cdot \frac{dI_{IN}}{dt}$$

With input current approximated to spare current

$$V_{IN\_PP(ESL)} = L_{ESL} \cdot \frac{I_{OUT}}{dt} \qquad \text{(eq. 10)}$$

To minimize the input voltage ripple and get better decoupling at the input power supply rail, a ceramic capacitor is recommended due to low ESR and ESL.

Example:

3 MHz DCDC, V_{IN} = 3.3 V, V_{OUT} = 1.1 V, I_{OUT} = 3.0 A, L = 0.470 μH.

With 50 mV of desired input ripple, the minimum input capacitor will be:

$$C_{INPP} = \frac{I_{OUT}\,(D - D^2)}{V_{IN\_PP(C)} \cdot F_{SW}} = \frac{3 \cdot \left(\frac{1.1}{3.3} - \frac{1.1}{3.3} \cdot \frac{1.1}{3.3}\right)}{0.05 \cdot 3000000} = 4.4\ \mu F$$

Summary

Table 1. SUMMARY

Components	Equation
Output Inductor	$L = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{\Delta I_L \cdot F_{SW} \cdot V_{IN}}$
Output Capacitor	**For Ripple** $C_{PP} = \frac{\Delta I_L}{8 \cdot V_{OUT\_PP(C)} \cdot F_{SW}}$ **For Transient Load** $C_{LT} = \frac{L \cdot I_{IPEAK}^2}{(V_{OUT} + V_{OV})^2 - V_{OUT}^2}$
Input Capacitor	$C_{INPP} = \frac{I_{OUT}(D - D^2)}{V_{IN\_PP(C)} \cdot F_{SW}}$

NCP63xx and NCV63xx Family

The NCP63xx and NCV63xx family of products are synchronous buck converters with both high side and low side integrated switches. Neither external transistor nor diodes are required for proper operation.

The feedback and compensation networks are also fully integrated. The high switching frequency allows the use of smaller size output filter components: This contributes to reducing overall solution size.

During external component selection, please verify compatibility with the recommended components described in the datasheet.

PUBLICATION ORDERING INFORMATION

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