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Power Stage Design Guidelines for the NCL30000 Single Stage CrM Flyback LED Driver

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APPLICATION NOTE

Introduction

Single stage critical conduction mode (CrM) flyback converters require different design considerations compared to fixed frequency or quasi-resonant (QR) flyback converters. Information is presented in this application note on establishing design parameters for the power stage of an LED driver. This includes the design of the transformer, power component selections, and EMI filter design as well as the startup and biasing circuitry of the NCL30000 LED driver controller. To illustrate the design process, an example power supply will be used. The key design objectives are as follows:

- V_{in} of 90−305 Vac
- PF > 0.98 Typical
- I_{out} of 350 mA
- V_{out} Range of 12 to 50 Vdc
- Maximum P_{out} of 17.5 W
- Efficiency of 85%
- Compliance with FCC Class B

A Microsoft® EXCEL® spreadsheet design tool available at www.onsemi.com was developed specifically for the NCL30000 controller. Design parameters are entered and the tool calculates key operating points and aids in transformer design. Calculations shown below are patterned off the design tool. Modifications for a specific LED driver design are easily calculated. The schematic for this LED driver is shown in Figure 1.

Transformer Design

Single stage high power factor flyback converters must draw predominately sine-shaped current to maintain high power factor. This means the converter must process power in a sine-squared manner due to the product of sine wave voltage times sine wave current. An LED load draws a nearly constant average power from the power supply output capacitor. To support this average load, the flyback power components must be capable of processing peak power of up to two times the average output power. In this case, a flyback transformer designed to handle a peak power of 42 W is required to power a 17.5 W LED load with efficiency factored in.

The NCL30000 is a variable frequency CrM controller and as such the transformer determines the operating frequency for a given set of input and output conditions. In understanding this behavior, it is helpful to view the flyback transformer as a coupled inductor. During the power switch on-time the current ramps up in the primary winding inductance storing energy in the core. When the switch turns off, the current will flow in the secondary winding delivering stored power to the load circuit. A Zero Current Detection (ZCD) circuit monitors when the energy stored in the core is depleted and signals to turn the power switch back on allowing the current to ramp up once again. Since the input voltage is a rectified sine wave shape and the on-time is fixed, the energy stored in the primary inductance each cycle will follow a sine-squared shape.

The on-time is established by the applied voltage acting on the primary inductance to develop the required energy storage. The off-time is set by the output voltage and secondary inductance as the energy is drained from the core. While numerous factors (efficiency, size, line variation etc) affect the choice of switching frequency, key factors for LED drivers include achieving high efficiency and meeting the EMI requirements therefore controlling the maximum switching frequency is important.

Applicable limits for EMI begin at 150 kHz and the required levels provide significant challenge in a low cost, compact design. Selecting a maximum switching frequency below 150 kHz places the first harmonic outside the requirement range. A natural reduction in harmonic amplitudes and design of practical input filters eases EMI compliance. For this design example, a maximum switching frequency of 100 kHz at 305 Vac is targeted. Minimum switching frequency is used when designing the transformer. The design spreadsheet presents the maximum switching frequency at high line based on entering the minimum frequency. Selecting the optimum minimum frequency is an interactive process.

The maximum switching frequency occurs under conditions of maximum input voltage and maximum output power. The high input voltage charges the primary inductor rapidly and the higher load drains the stored energy quickly.

Flyback transformer design has wide latitude in parameter selection. The design of this transformer will start with establishing the transformer turns ratio. The maximum ratio is controlled by the voltage stress on the switching FET and the minimum is controlled by the voltage stress on the output rectifier.

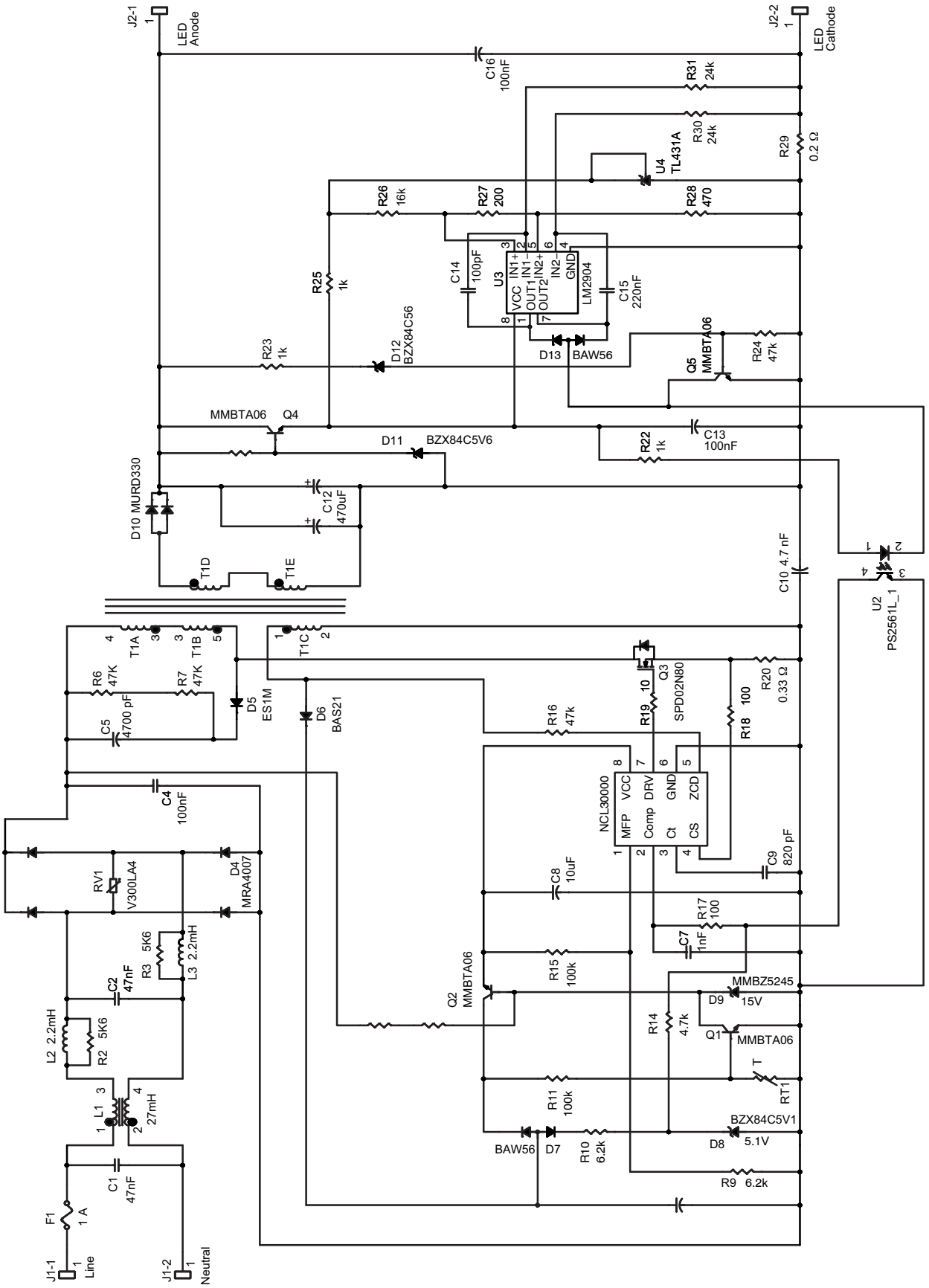

Figure 1. Wide Input Main 350 mA Load Schematic

FET Switch

The NCL30000 drives an external power FET which controls the current in the flyback transformer primary. An external FET allows optimization for a particular application balancing performance, cost, and size constraints. The demonstration board was designed to accept the surface mount DPAK or through-hole TO−220 power packages. The choice between these options depends largely on dissipation and thermal management issues. The 17.5 W target application in 50°C ambient works well with a DPAK package.

After determining the required drain to source voltage rating, many designers focus almost exclusively on FET on resistance as the final criteria. Due to high voltage switching, the FET output capacitance should also be considered. This capacitance must be charged each time the FET is turned off and discharged when the FET is turned on. The associated dissipation is often significant. A balance between reduced conduction losses of a low on resistance FET and minimizing switching losses of a low capacitance FET should be investigated. Some empirical testing may be required to reach an optimal solution. High performance FETs featuring low on resistance and low capacitance are available and the selection represents a tradeoff between efficiency and system cost.

Given the high input voltage for this application, an 800 V FET is selected. Applying a 0.8 stress ratio reduces the maximum applied voltage to 640 V. The maximum transformer turns ratio is computed using the allowable FET voltage, peak input voltage, and secondary output voltage.

$$N_{max} = \frac{V_{ds} - \sqrt{2} \cdot V_{in}}{V_{out}} = \frac{640 - \sqrt{2} \cdot 305}{50} \quad \text{(eq. 1)}$$

$$= 4.17 \text{ maximum turns ratio}$$

Output Rectifier

The output rectifier must conduct the current from the transformer secondary winding to the output filter capacitor. Selecting a rectifier with low forward voltage drop will reduce losses and improve overall efficiency. Secondary current in a flyback converter follows a ramping shape where the peak current is much higher than the average output current. A rectifier with a rating at least 5 to 10 times the average current is typical. The NCL30000 is a critical conduction mode controller which means the current in the output rectifier will fall to zero before initiating the next switching cycle. CrM operation dramatically reduces losses by avoiding rectifier recovery losses. Even so, a rectifier with moderately fast recovery displays lower capacitance and will enhance efficiency. The MURD330, a 300 V, 3 A, 50 ns rectifier is selected for low forward voltage, fast recovery, and to support the high maximum input voltage range.

Applying a 0.8 stress ratio results in a maximum reverse stress of 240 V for this rectifier. The formula below determines the minimum transformer turns ratio based on peak input voltage, rectifier stress, and output voltage.

$$N_{min} = \frac{\sqrt{2} \cdot V_{in}}{V_r - V_{out}} = \frac{\sqrt{2} \cdot 305}{240 - 50} \quad \text{(eq. 2)}$$

$$= 2.27 \text{ minimum turns ratio}$$

At this point, the turns ratio must be selected between the maximum and minimum ratios calculated above. Practical transformer design may dictate a certain number of turns depending on the core and wire sizes. For this design example, the EFD25 core will be used. Triple insulated wire is chosen to meet safety isolation requirements. Through an iterative process, a turns ratio of 3.8 provides a good fit for the windings.

The next calculations are power switch on-time and primary inductance at the low line condition of 90 V ac or 127 V peak and maximum delivered power of 17.5 W. The switching frequency is adjusted to meet transformer construction parameters. At 90 Vac, the switching frequency was chosen as 45 kHz. This transformer design will follow the formulae shown below which have been compensated for single stage CrM converter applications.

$$t_{on} = \frac{1}{f_{SW}\left(\frac{V_{min}}{N \cdot V_{out}} + 1\right)} = \frac{1}{45000\left(\frac{127}{3.8 \cdot 50} + 1\right)} \quad \text{(eq. 3)}$$

$$= 13.3 \ \mu s$$

Primary inductance is calculated from the efficiency, desired switching frequency, minimum input voltage, on-time, and output power.

$$L_{pri} = \frac{\eta \cdot f_{SW} \cdot V_{min}^{\ 2} \cdot t_{on}^{\ 2}}{4 \cdot P_{out}} \quad \text{(eq. 4)}$$

$$= \frac{0.85 \cdot 45000 \cdot 127^{\ 2} \cdot 13.3 \ \mu^2}{4 \cdot 17.5} = 1.57 \text{ mH}$$

Primary current in a flyback transformer ramps to a peak value each cycle. Maximum current occurs at the peak of the rectified sine wave input waveform following the formula below.

$$I_{pkpri} = \frac{V_{min} \cdot t_{on}}{L_{pri}} = \frac{127 \cdot 13.3 \ \mu}{0.00157} = 1.08 \text{ A} \quad \text{(eq. 5)}$$

Peak primary current of 1.08 A is suitable for the 2 A SPD02N80C3 power FET from Infineon. This FET has on resistance of 2.7 Ω and a low output capacitance of 13 pF.

Secondary current for this CrM converter starts at a peak value determined by the transformer turns ratio and falls to zero in a time determined by the winding inductance and output voltage.

$$I_{pksec} = I_{pkpri} \cdot N = 1.08 \cdot 3.8 = 4.1 \text{ A} \quad \text{(eq. 6)}$$

As previously mentioned, this single stage flyback transformer must support peak power of twice the average power. Core flux density is directly related to power level and therefore this transformer must support the flux at the peak power point. Core loss is proportional to maximum flux density while temperature rise is based on average transformer dissipation. Given that the maximum flux

density occurs only for a short time at the peak of the rectified sine wave input the allowable flux can be higher than conventional flyback transformers which operate at a nearly constant flux level. Maximum flux level is dependant on core material and should be evaluated at the maximum operating temperature. In this case, a peak flux density of 3200 Gauss is selected.

An EFD25 core was selected due to its low profile construction. This core has a cross sectional area of 0.58 cm^2. Primary turns follow the formula below:

$$N_{pri} = \frac{L_{pri} \cdot I_{pkpri} \cdot 10^8}{B_{max} \cdot A_c} = \frac{0.00157 \cdot 1.08 \cdot 10^8}{3200 \cdot 0.58} \quad \text{(eq. 7)}$$

$$= 92 \text{ turns}$$

The secondary winding is found using this formula:

$$N_{sec} = \frac{N_{pri}}{N} = \frac{92}{3.8} \approx 24 \text{ turns} \quad \text{(eq. 8)}$$

Construction Considerations

The primary winding is constructed in two layers with the secondary positioned between the layers to reduce leakage inductance. Half the primary or 46 turns of #28 wire fills one layer on the bobbin. Turns are placed closely with no overlaps. The same approach is used for the remaining half of the primary after the secondary is placed.

The secondary winding is configured as two parallel windings in one layer. 24 turns is realized when the two windings are series connected. This allows a series connection of the windings for 50 V/350 mA applications or a parallel connection for 25 V/700 mA LED applications. The secondary winding uses #26 triple insulated wire for compliance with safety agency isolation requirements. Constructing the secondary using two pieces of this wire wound in 12 turns fills one even layer across the bobbin. The winding should be smooth with no overlaps providing an even base for subsequent windings.

The primary bias winding is positioned on top of the second layer of primary winding. A minimum of 10.2 V is needed to maintain NCL30000 operation; however the isolation diode D7 and primary regulator Q2 require about 2 V to maintain proper control. For this circuit configuration, the bias winding should maintain at least 12.2 V. The primary side discrete regulator allows proper operation across the wide output range of 12 – 50 Vdc, design of this will be discussed in the biasing section.

For this example the minimum secondary voltage is 12 V (4 LEDs at a minimum Vf of 3 V) and the secondary turns are 24. Note alternate designs may have different secondary voltage and number of turns. In that case a different number of bias winding turns may be required. Bias winding turns is related to the secondary winding turns by the following formula:

$$N_{bias} = N_{sec} \cdot \frac{V_{bias}}{V_{sec}} = 24 \cdot \frac{12.2}{12} = 24.4 \text{ turns} \quad \text{(eq. 9)}$$

Leakage inductance between windings will raise the effective bias winding voltage compared to the results of the formula above. This elevated voltage can become too high with the maximum 50 volt output. In most applications the turns can be reduced to compensate and in this case 22 turns is selected to reduce the maximum bias voltage. Detailed winding and insulation information can be found in the magnetic design sheet.

EMI Filter

The EMI filter attenuates the switching current drawn by the power converter reducing the high frequency harmonics to within conducted emissions limits. The filter must not degrade the power factor by introducing a phase shift of the current with the line-to-line or X capacitors. Low total capacitance will minimize this effect. Balancing these attributes is a performance tradeoff considering the wide input voltage requirements.

Given the complexity of the circuit, an empirical approach was taken. Starting with selecting C4 as 100 nF a two-stage L−C differential mode filter comprised of 2.2 mH for L2 and L3 together with 47 nF for C2 performed well. Differential inductors L2 and L3 display a self-resonance which degrades the filter effectiveness in the resonant range. Connecting a resistor across these inductors effectively dampens the resonance providing smoother filter performance. This comes at the expense of somewhat lower attenuation at high frequencies due to the shunting path around the inductor. The resistor is selected based on the self−resonance of the inductor. This damping resistor is typically chosen to be slightly lower than the effective impedance of the inductor at the point of resonance. Determine the actual resonant point from an inductance analyzer or a conducted EMI plot. In this case, a pronounced peak was evident on the conducted EMI plot at about 500 kHz. Inductor impedance at this frequency is:

$$X_L = 2 \cdot \pi \cdot f_{resonance} \cdot L$$
$$= 2 \cdot \pi \cdot 500,000 \cdot 0.0022 = 6.9 \text{ k}\Omega \quad \text{(eq. 10)}$$

In this application, 5.6 kΩ performs well as a damping resistor. A 27 mH common mode inductor and 47 nF for the first X capacitor C1 complete a filter design meeting Class B conducted emissions limits.

Capacitive coupling in the power transformer contributes to common mode emissions. Adding a decoupling capacitor close to the transformer provides a path for the common mode currents minimizing emissions. In this 17.5 W application, 4.7 nF performed well. Select a capacitor with “Y1” rating to meet safety guidelines.

Conventional power supplies utilizing large filter capacitors after the input rectifier bridge display high surge current when AC power is applied. Inrush limiting devices are often employed to mitigate the surge current which can cause component failure or nuisance tripping of circuit breakers. The low input capacitance approach taken in this

design to meet high power factor has the added benefit of not needing inrush current limiting.

A fuse is often required in a system which must meet safety agency requirements. The fuse will likely become a ‘safety critical’ part meaning the sourcing must be controlled. A distinct advantage is the fuse will open during fault testing in a repeatable manner instead of some other component in the power path which may fail unpredictably complicating the safety approval process. The capacitors in the input filter do present some small inrush current. Over time, the cumulative effects of powering the converter can cause metal migration in the fuse element leading to fuse failure. A fuse rated two or three times the maximum operating current will support the inrush current without heating thus avoiding the metal migration issue.

Startup Circuit and Primary Bias

When power is applied, the user expects illumination to occur with minimal delay. Virtually all power converters utilize energy from the rectified line to charge the bias network at start up. After normal steady state operation is achieved an alternate source of primary bias is usually provided to minimize dissipation. There is a tradeoff between short start up delay and dissipation. Ideally, startup of an LED driver should be less than 1 second. The NCL30000 was specifically designed to draw < 35 μA at startup to support rapid start with minimal dissipation.

When power is applied, a resistor connected between the rectified ac line and V_{CC} charges up the V_{CC} capacitor. When the voltage on V_{CC} reaches 12 V nominal, the internal references and logic of the NCL30000 are turned on and the part starts switching. The turn on comparator has hysteresis (2.5 V nominal) to ensure sufficient time for the auxiliary winding to start supplying current directly to the V_{CC} capacitor. Based on a startup time of 8 ms and a running current of 3 mA, the minimum size of the capacitor can be selected:

$$C_{start} = \frac{I_{run} \cdot T_{start}}{V_{hyst}} = \frac{0.003 \cdot 0.008}{2.5} \cong 10\ \mu F \quad \text{(eq. 11)}$$

R11 and R15 also require current of approximately 12 V / (100k // 100k) = 240 μA giving a total current drain of 275 μA after adding in the 35 μA NCL30000 start current. The balance of the current from the start resistor will charge the start capacitor in a target time of 250 ms. The minimum 90 Vac line voltage peak charges the EMI filter capacitor during start up to $90 \times \sqrt{2} = 127$ V. This voltage is applied across the start resistor and is sufficiently high to approximate a constant current characteristic. Start resistor value follows the approximation shown below:

$$R_{start} \leq \frac{V_{min}}{\frac{C \cdot dV_{start}}{dT} + I_d} = \frac{127}{\frac{10\mu \cdot 12}{0.25} + 275\mu} = 168\ k\Omega \text{ (eq. 12)}$$

A target value of 94 kΩ was chosen to ensure reliable start up.

A separate transformer winding is provided as the source of primary bias power as detailed in the transformer design section. As the LED voltage increases, so will the bias winding voltage. Since this design example targets a range of LED forward voltages from 12 – 50 Vdc, a discrete linear regulator comprised of a bipolar transistor and zener diode limits the maximum voltage delivered to the NCL30000 below the 20 V maximum. A 15 V zener provides sufficient voltage to operate the primary circuitry and minimizes power loss under higher output voltage conditions.

If the load is well defined to a narrow range of LED forward voltage, the primary bias regulator is not necessary. The transformer turns ratio for the bias winding can be set to provide approximately 12 to 15 V. The maximum voltage should be limited to less than 18 V worst case providing margin on the NCL30000 maximum rating of 20 V. If necessary, a dropping resistor and zener diode can be included to assure the input voltage is not exceeded.

An optional thermal shutdown is implemented with positive temperature coefficient (PTC) thermistor RT1. This thermistor is placed close to the switching FET Q3 sensing temperature stress related to load and surrounding ambient temperature. Situations resulting in excessive temperature will cause RT1 to switch to high impedance turning on Q1. This transistor will in turn shut off Q2 removing the bias power from the NCL30000 and stopping all switching. When RT1 cools down, normal operation will resume. Shutdown temperature is controlled by selecting the transition temperature for RT1. Thermistors are available in a wide range of temperatures to match requirements of a particular application.

Output Filter

As previously discussed, a high power factor isolated single-stage converter processes power in a sine squared manner at twice the line frequency. Unlike traditional flyback converters which have energy storage capacitors on the primary and secondary side, virtually all the storage with a power factor corrected single stage converter is found on the secondary side. As a result, more output capacitance is required to store energy when the peak of the 100 or 120 Hz rectified sine wave is greater than the average power drawn by the LED load. Conversely, the capacitors release the stored energy to the load when the rectified sine wave falls below the target output power. As a storage capacitor charges and discharges some ripple current is developed in the LED load. The magnitude of ripple current is controlled by the amount of filter capacitance and is a complex relationship involving the constant voltage nature of the LEDs and their intrinsic resistance. Increasing the capacitance reduces the peak-to-peak LED ripple content.

While dependent on the characteristics of the LED selected, high brightness high power LEDs can normally tolerate 30 to 40% current ripple or more. The measurement is referenced as a peak-to-peak value meaning 350 mA average current will display 100 to 140 mA peak-to-peak ripple. In this 350 mA application, two 470 μF capacitors are sufficient to limit ripple to 30%. Holding output power constant, for a 700 mA design two 1000 μF output

capacitors would be required, but lower voltage rating capacitors can be used. Ultimately the allowable maximum operating current of the specific LEDs used determines the amount of ripple that can be tolerated, but for some high brightness LEDs on the market, the output capacitance can be reduced further as the LEDs can tolerate higher maximum currents.

The feedback control is comprised of a fast and a slow current loop. In this example, the fast loop is set to a level just above the peak of the output ripple current. Reducing output capacitance will increase the peak current which may rise to a level activating the fast current loop which would degrade power factor performance. If the ripple current is increased by changing capacitor value the threshold of the fast control loop must be reset to a level higher than the peak output current. Information on setting this threshold can be found in the NCL30000 datasheet.

Electrolytic capacitors should be selected to match the LED driver lifetime with the end application operating requirements. Higher temperature rated capacitors enhance lifetime for an optimal solution. LED ripple current requirements in single stage converters generally require enough capacitance that capacitor ripple current is well below the capacitor ratings. Quality capacitors typically will provide lifetime commensurate with expectations and some manufacturers have specific capacitor lines intended for lighting applications.

Secondary Bias

The average mode feedback compensation is intentionally set to a low frequency as described in the feedback section of the NCL30000 datasheet. The relatively large feedback compensation capacitor must charge to normal operating voltage after initial power up which introduces significant delay in achieving regulation. This delay can lead to overshoot in LED current. Minimizing the required voltage change on the compensation capacitor allows the feedback loop to take control of the output quicker therefore reducing over-current conditions. Maintaining a low bias voltage reduces the required change in compensation capacitor voltage. For this example, a bipolar transistor and 5.6 V zener diode are employed to provide secondary bias voltage of about 5 V. This bias transistor minimizes power loss compared to a simple resistor and zener diode solution and allows the LED driver to operate over a very wide range of output voltage. This circuit will support as few as 4 LEDs and up to 15 LEDs.

The secondary bias can be optimized if the application uses a specific number of LEDs. Fewer components and better efficiency can be realized by limiting the output voltage range and adding a secondary bias winding to the transformer.

Conclusion

While the design of the power stage of a CrM flyback converter is more complex than a traditional fixed frequency flyback, the benefits of a single stage converter which can achieve high power factor and energy conversion in a single stage are critical for LED lighting applications. The spreadsheet design tool provides a streamlined approach to designing a single stage high power factor CrM flyback converter based on the NCL30000 LED controller. Design parameters are easily changed and effect on overall design is easily assessed. Key parameters for transformer design are presented greatly simplifying the task of transformer design.

Additional Application Information and Tools

Evaluation board NCL30000LED3GEVB is available for this 90 – 305 Vac design example. The Microsoft EXCEL spreadsheet tool and NCL30000 datasheet are available at the ON Semiconductor website. A sample transformer winding sheet is provided in the Appendix which details requirements for the transformer developed in this application note.

MAGNETICS DESIGN DATA SHEET

Inductance: 1.57 mH
Bobbin Type: 10 pin horizontal CSH−EFD25−1S−10P
Core Type: EFD25/13/9−3C90
Core Gap: Gap for 1.57 mH, ~0.016 inches

Winding Number/Type				Turns/Material/Gauge/Insulation Data		
Step	**Winding**	**Start**	**Finish**	**Turns**	**Material**	**Notes**
1	1/2 Primary	6	3	46	#28	Wind in one layer
2	Insulate			1	Mylar Tape	
3	Secondary	Fly1	Fly2	12	#26 TEX−E Triple insulated	Wind bifilar with two strands of wire. Fly leads exit top of bobbin over pins 6−10
		Fly3	Fly4			
4	Insulate			1	Mylar Tape	
5	1/2 Primary	3	5	46	#28	Wind in one layer
6	Insulate			1	Mylar Tape	
7	Pri Bias	1	2	22	#28	Spread evenly in one layer
8	Insulate			3	Mylar Tape	
9	Assemble				Gap	Final core wrap
10	Shield				Copper	Add shield over core
11	Insulate				Mylar Tape	Insulate shield

Hipot: 3 kV from Primary to Secondary for 1 minute.

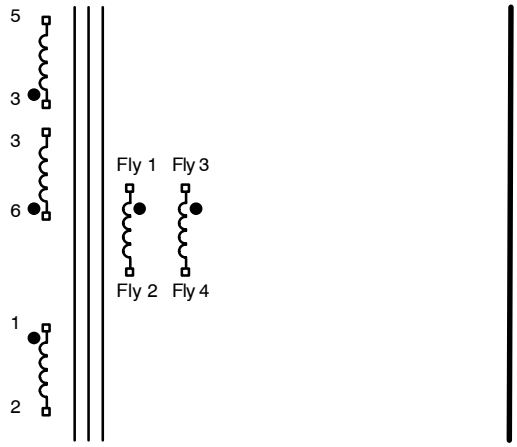

Figure 2. Schematic

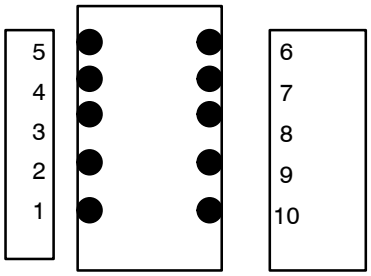

Figure 3. Bobbin Pinout − Bottom View

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