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AND8327/D

Stability Analysis in Multiple Loop Systems

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Loop stability analysis usually starts from an open−loop Bode plot of the plant under study, e.g. the power stage of a buck or a flyback converter. From this diagram, the designer can extract phase and gain data within the frequency range of interest. His job then consists in identifying a compensator structure which will lead to the selected crossover frequency affected by the right phase margin. The final step requires the study of the total loop gain, the power plant followed by the compensator, showing that the poles/zeros placed on the compensator ensure stability once the loop is closed. If this operation is rather straightforward with single loops, the operation becomes more complicated with converters implementing weighted feedback. This paper capitalizes on the Ref. [1] work and explores different ways to apply the technique to power converters featuring multiple feedback paths.

The TL431, a Multiple Loop System

The TL431 alone, can be modeled as a multiple loop feedback system. Figure 1 shows a TL431 classically wired in a type−2 configuration, as described in Ref. [2]. From this schematic, one can identify so−called slow and fast lanes.

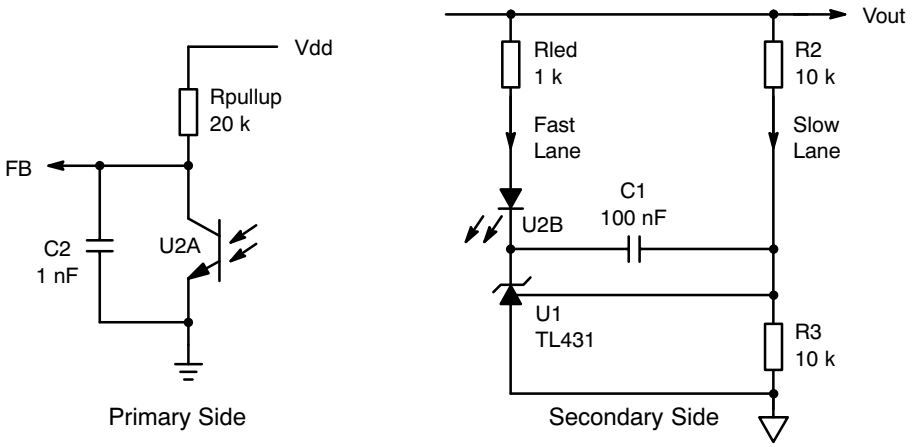

Figure 1. A TL431 Wired in a Classical Configuration, Observing the dc Voltage of a Converter

The TL431 can be seen as a programmable zener also called a shunt regulator. When the output voltage changes, e.g. because of a load variation, the information is conveyed to the inverting input of the TL431 via R_2/R_3 and asks the programmable zener to pump more or less current into the optocoupler LED. It does so by adjusting its cathode voltage. By this way, the feedback signal observed on the primary side also changes and instructs the controller to alter its operating point. If the output voltage variations are too fast, the frequency sensed by R_2 exceeds the pole position introduced by C_1 and the ac contribution of this path to the feedback signal becomes null: the TL431 no longer changes its operating point and the LED cathode is now fixed. However, as the LED cathode is fixed, the anode still senses an output voltage variation via R_{led}. This current variation propagates via the optocoupler and affects the feedback voltage. Therefore, even if you increase C_1, it has no effect in rolling off the loop gain since R_{led} always senses the output voltage. The transfer function of such a system can be written in the following form [2]:

$$\frac{V_{FB}(s)}{V_{out}(s)} = G_1(s)\left(1 + \frac{1}{sR_2C_1}\right) \qquad \text{(eq. 1)}$$

where $G_1(s)$ represents the mid−band gain brought by the optocoupler CTR, the LED and the pull−up resistors associated to the capacitor C_2. From this expression, we can actually see the presence of two loops by developing Equation 1:

$$\frac{V_{FB}(s)}{V_{out}(s)} = G_1(s) + \frac{G_1(s)}{sR_2C_1} \qquad \text{(eq. 2)}$$

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The loop gain of such a system could be measured by breaking the loop at the feedback point. Unfortunately, depending on the converter configuration, this solution can sometimes be difficult to implement. The best is then to measure the loop gain from the secondary side. In this particular example, both the fast and slow lanes share a similar entry point. The total loop gain could therefore be measured as suggested by Figure 2:

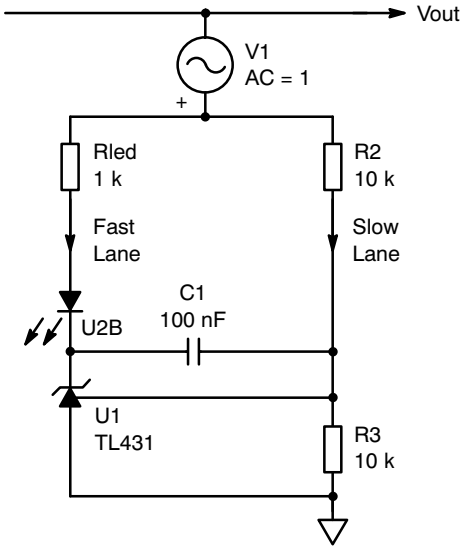

Figure 2. When Both Slow and Fast Lanes are Connected Together, the Measurement is Easy to Run

A stimulus source is inserted in series with the output voltage and both slow and fast lanes are ac swept. The voltage observed on the feedback pin is therefore proportional to both inputs and is representative of what Equations 1 and 2 predict.

In Figure 3, we can see the presence of a LC filter, added to remove unwanted high frequency spikes, typical of a flyback converter.

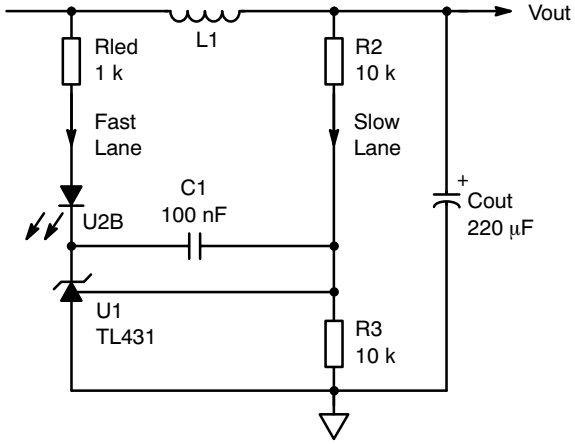

Figure 3. The Presence of the LC Filter Splits Both Lanes

In this schematic, it is not possible to sweep both inputs together as they are separated by the LC filter. Fortunately, we can apply the superposition theorem as we are dealing with a linear system. At first, we will sweep the slow lane while keeping the fast lane to a bias level, totally disconnected from the output voltage. A dc voltage supplied by an external source will do. This is what Figure 4 shows. The precision of the 5 V source is not relevant here as it only serves bias purposes. The ac source actually represents an injection transformer, classically used in loop stability studies. The A and B probes go to a network analyzer which will compute

$$20\log_{10}\left(\frac{B}{A}\right),$$

displaying a loop gain equal to

$$\frac{G_1(s)}{sR_2C_1}$$

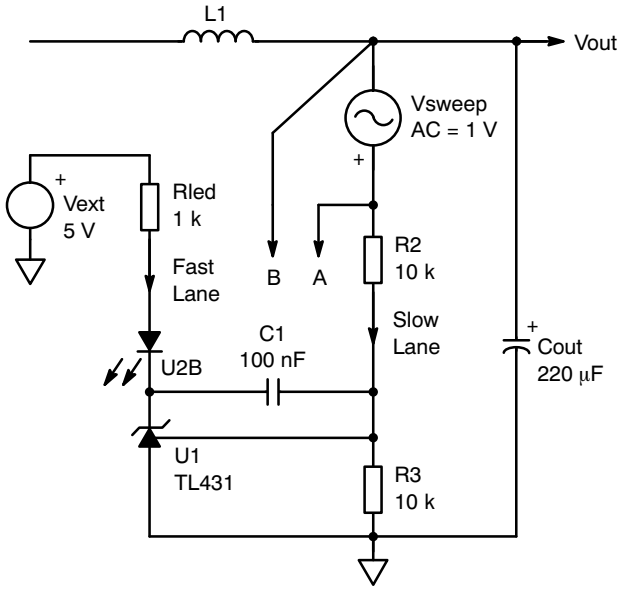

Figure 4. The Fast Lane is ac Disconnected from the Circuit and Only the Slow Lane Receives a Stimulus

Then, once the plot is saved, the configuration needs to be changed to the other input, as suggested by Figure 5. In this circuit, the upper R_2 terminal is connected to a dc voltage whose value must equal the regulated voltage whereas the fast lane input is now ac swept:

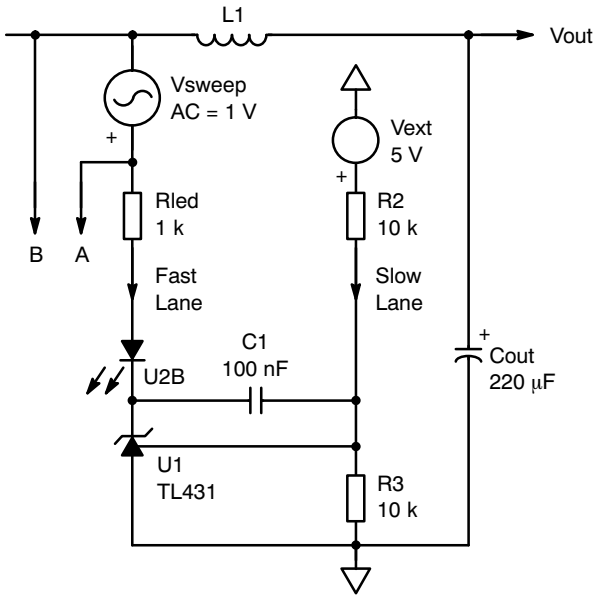

Figure 5. The Fast Lane is Now ac Swept as the Slow Lane is Simply dc Biased

The dc adjustment might be a little difficult given the open−loop gain brought by the TL431 and the sensitivity on the external bias. The network analyzer still computes $20\log_{10}(B/A)$ for the fast lane but this time, it plots a loop gain equal to $G_1(s)$.

Combining Signals Together

Once we have both slow and fast lanes loop plots on the screen, how can we combine them? Can we just sum up the gain and phase diagrams, respectively expressed in dB and degrees? Certainly not, it would correspond to cascaded gain blocks and not paralleled paths. We need to vector sum both output signals and reconstruct the final signal which expresses the combination of both loops. Using Euler notation, we can express the slow lane signal by a rotating vector affected by a module A_1 and a phase φ_1:

$$\overrightarrow{V_{out,slow}} = A_1(\cos\varphi_1 + j\sin\varphi_1) \qquad \text{(eq. 3)}$$

Using a similar notation, we can write the fast lane expression:

$$\overrightarrow{V_{out,fast}} = A_2(\cos\varphi_2 + j\sin\varphi_2) \qquad \text{(eq. 4)}$$

To reconstruct and plot the final gain curve combining both signals − the signal observed on the feedback pin once all loops are closed − we need to separate the real and imaginary portions of the two lanes and sum them together:

$$\mathrm{Re}(\overrightarrow{V_{FB}}) = A_1\cos\varphi_1 + A_2\cos\varphi_2 = X \qquad \text{(eq. 5)}$$

$$\mathrm{Im}(\overrightarrow{V_{FB}}) = A_1\sin\varphi_1 + A_2\sin\varphi_2 = Y \qquad \text{(eq. 6)}$$

The rotating vector obtained at the end will be of the following form:

$$\overrightarrow{V_{FB}} = X + jY \qquad \text{(eq. 7)}$$

Where we can now extract a module and an argument:

$$\|\overrightarrow{V_{FB}}\| = \sqrt{Y^2 + X^2} \qquad \text{(eq. 8)}$$

$$\arg\overrightarrow{V_{FB}} = \tan^{-1}\left(\frac{Y}{X}\right) \qquad \text{(eq. 9)}$$

Plotting $20\log_{10}$ of Equation 8 and the phase returned by Equation 9 should give the Bode plot we are looking for.

SPICE Application

Before rushing to the laboratory to apply this technique, let's give it a try with a SPICE simulation and check that our equations give the correct answers. Figure 6 depicts the TL431 circuit ready to be ac swept, both inputs being connected together. The sweep technique uses an old trick with L_1 and C_3 which open the loop in ac but keep it closed in dc. The closed path in dc helps to automatically adjust the voltage on the upper terminal of R_2 to obtain a 2.5 V on the feedback output, right in the middle of the available dynamic. This ensures a circuit properly biased without the need to tweak anything else. The bias points appearing in Figure 6 confirms the right values. Once the ac sweep is run the Bode diagram appears in Figure 7 and confirms the presence of an origin pole, a low frequency zero, a high frequency pole and a mid−band gain in between. The phase boost peaks to 134° at a frequency of 380 Hz where the gain reaches 23 dB. Now, let us separate the two lanes by applying the technique we described earlier. The exploration of the fast lane requires a simple dc bias on the divider network, again provided by the operational amplifier. Figure 8 portrays the circuit we have implemented. The modulation signal enters the fast lane through the ac source V_{sweep} whereas L_1 and C_4 prevent any injection in the slow lane: both loops are fully decoupled from each others. For the slow lane sweep, Figure 9 shows the adopted sketch: the upper LED resistor is simply hooked to a dc source and the ac stimulus now sweeps the slow lane through the LC network. Again, there is no ac link between both inputs.

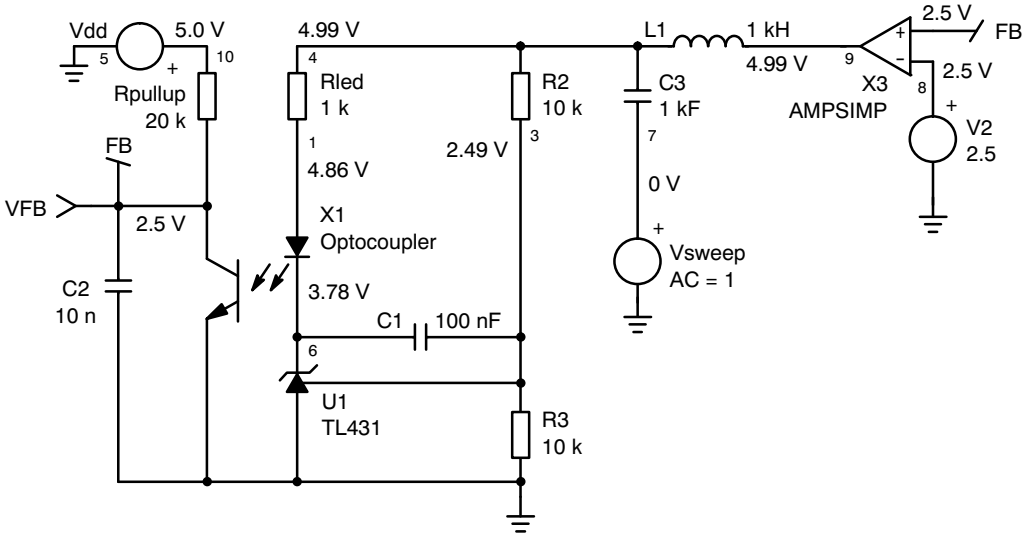

Figure 6. The Type 2 Compensator Based on a TL431 and Adapted for a SPICE Simulation

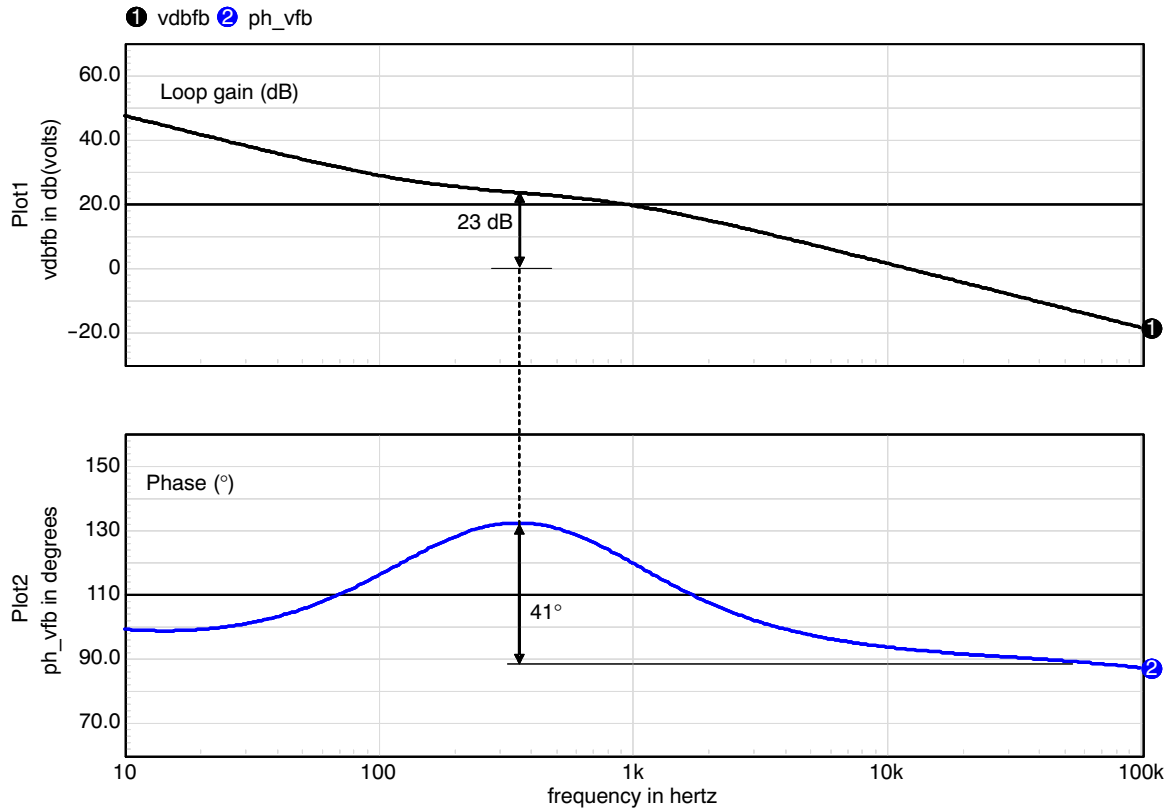

Figure 7. ac Results of the Type 2 Compensator, Highlighting the Presence of Two Poles and One Zero

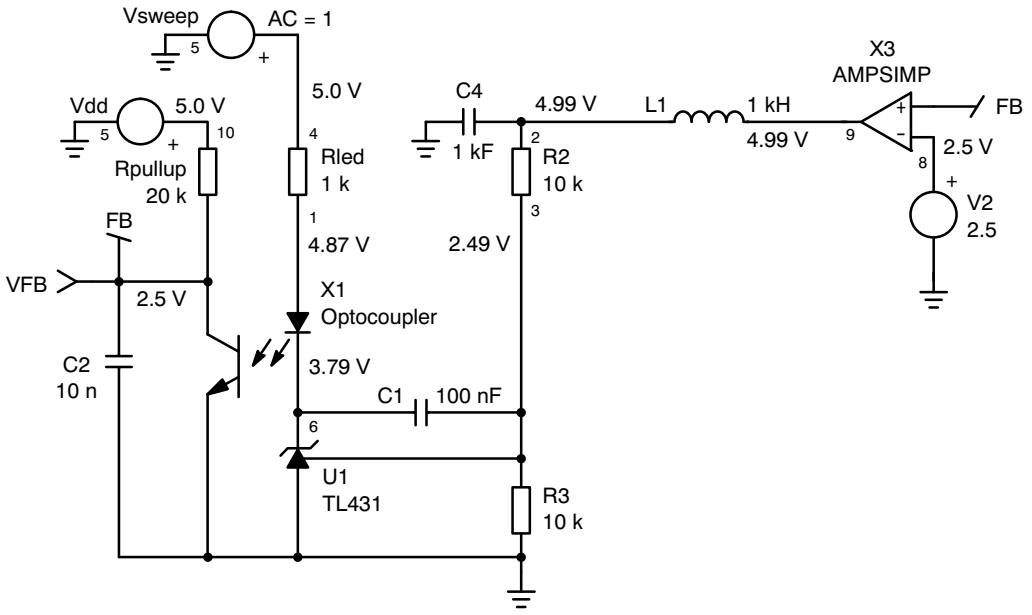

Figure 8. The Fast Lane Sweep Requires a Clear Separation between Both Lanes

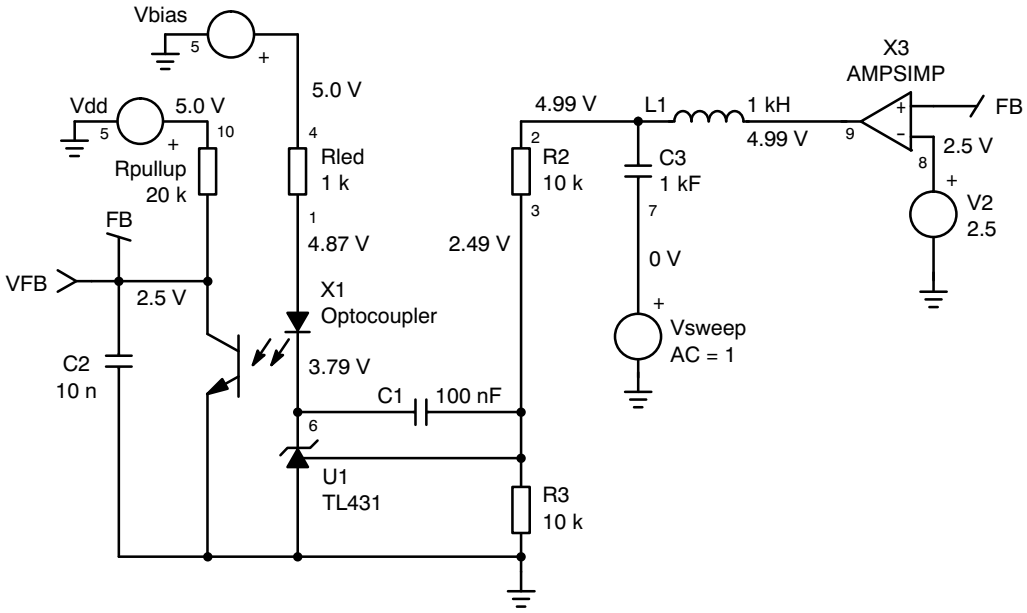

Figure 9. In the Slow Lane Sweep, the Fast Lane Input Goes to a Fixed dc Bias

SPICE offers the possibility to extract the imaginary and real parts from an ac simulation. This is what Figure 10 shows where the real curves of both the fast and slow sweeps have been gathered in the upper portion. The lower section of the figure contains the imaginary portions of both lanes. The graphical viewer can easily manipulate waveforms and the sum of both imaginary and real curves already appears on the picture.

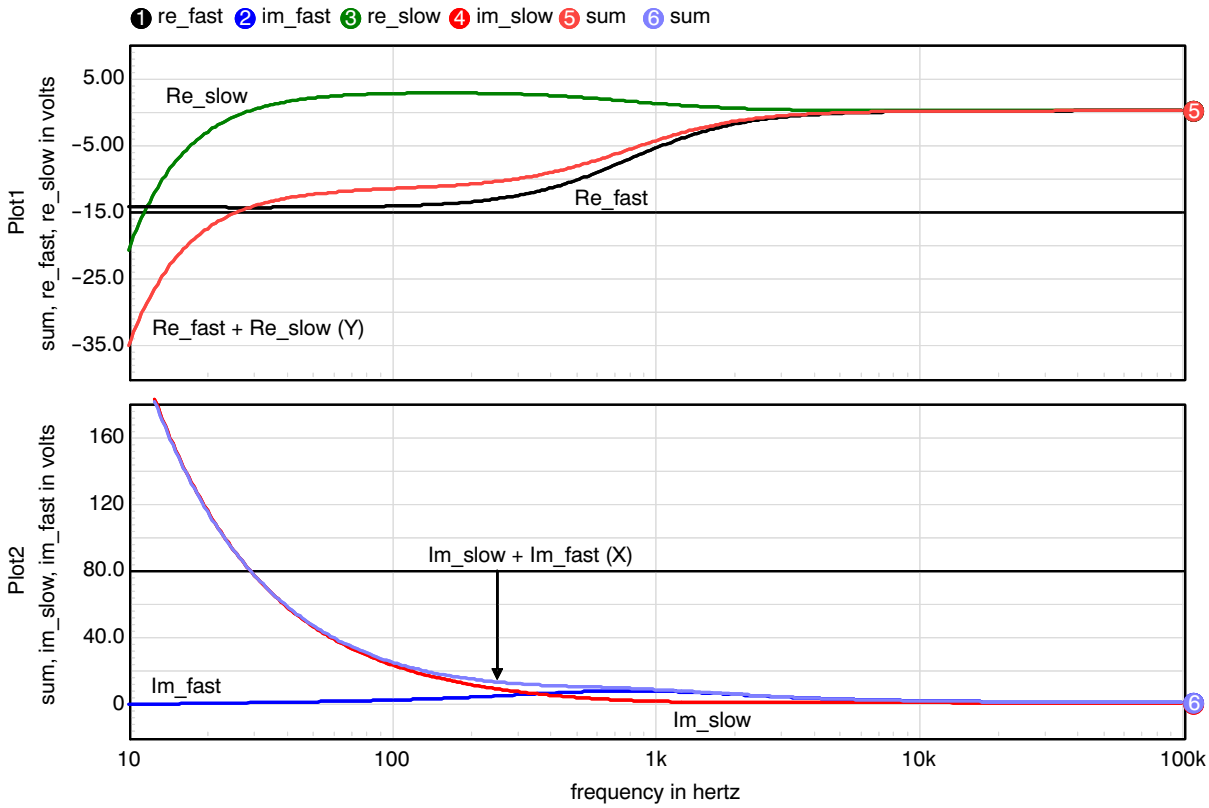

Figure 10. This Plot Gathers the Real and Imaginary Portions of the Feedback Signal Collected when the Fast and Slow Lanes are Separately ac Swept

Once we reached that point, we can apply Equations 8 and 9 via the graphical viewer internal script. The resulting waveforms are displayed on Figures 11 and 12 then compared to Figure 7. They are identical gain wise (Figure 11), despite different signs on the phase in Figure 12 (the $\tan^{-1}$ function is modulo 180°).

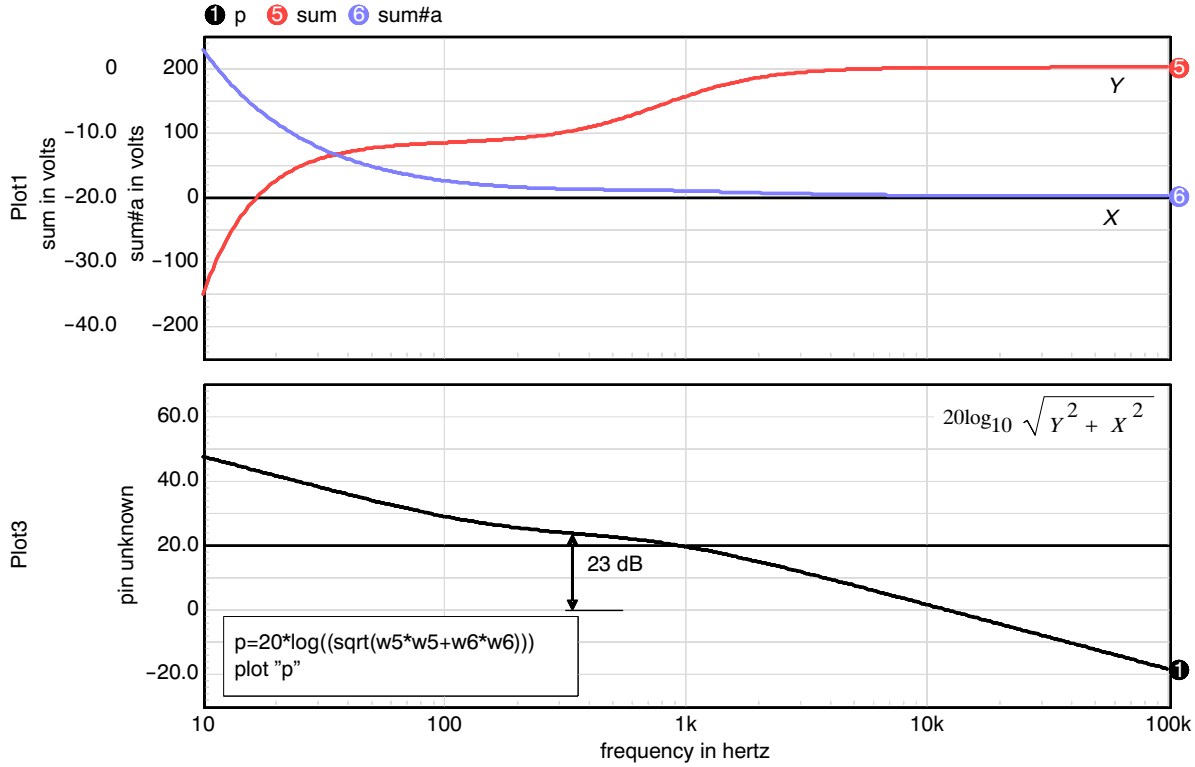

Figure 11. Once Mathematical Calculations are Made, the Amplitude Response Reveals the Classical Type 2 Function we are Looking For

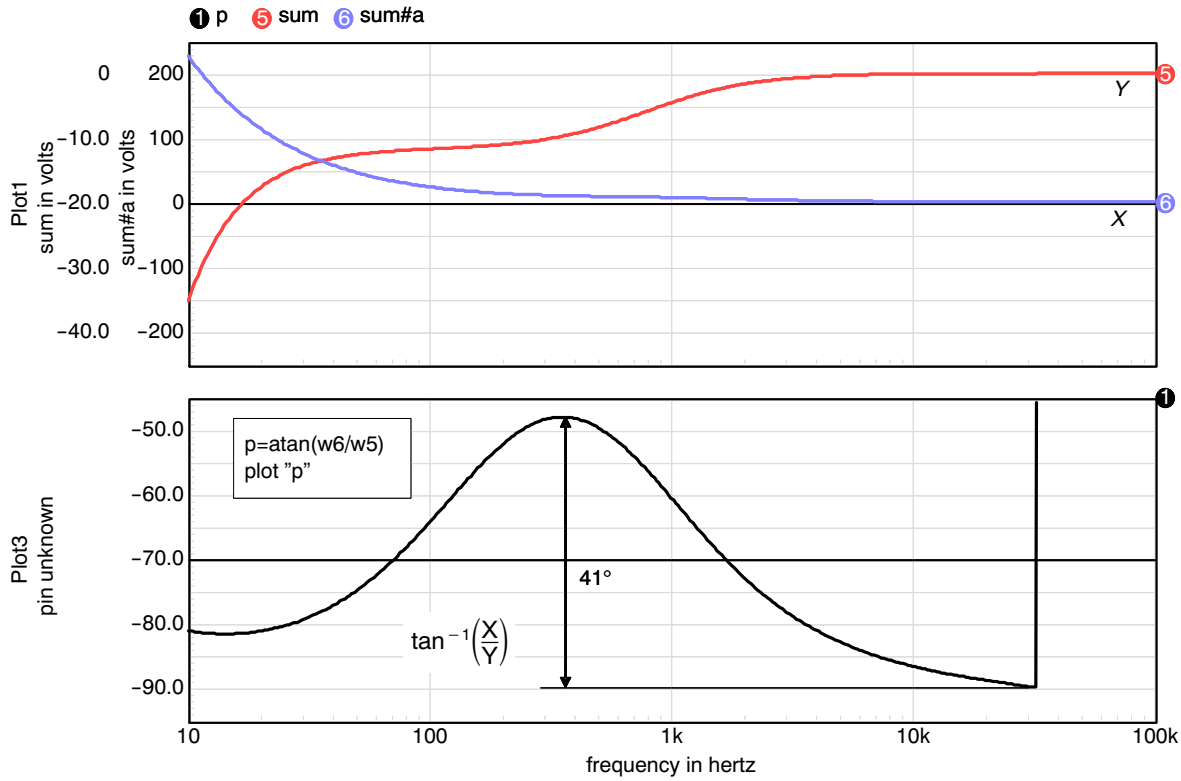

Figure 12. Calculating the Argument Leads to a Similar Result for the Phase, Showing a Boost of 41°

Combining Data with a Network Analyzer, a Real Case Example

To check the validity of our assumptions, we have built a 65 W power supply based on a classical UC3843 controller. The internal op−amp is disabled via a pull−up resistor connected to the reference voltage. Figure 13 shows the adopted schematic:

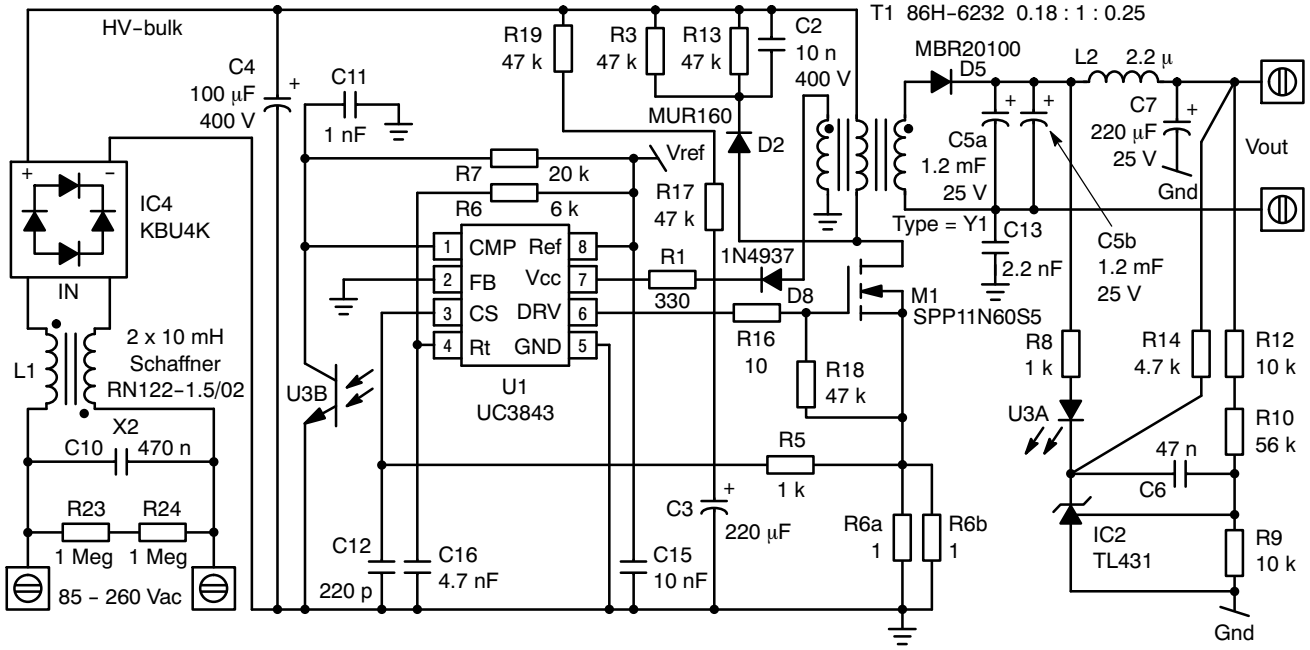

Figure 13. The Schematic of the 19 V/3 A Adapter Features a UC3843 with a TL431 on the Secondary Side

The output voltage is regulated by a TL431 wired in a type 2 configuration. The fast lane (optocoupler lane) and the slow lane (TL431 resistor divider) are separated by an LC filter which is placed to further attenuate the various high−frequency output spikes inherent to the flyback stages. In order to measure the loop response of our adapter with a network analyzer, we are going to use the method described in the first part of this document. The main advantage of this method lies in the measurement operations confined on the isolated secondary side only.

We will first start by sweeping the slow lane, while the fast lane is biased to 19 V (output voltage value) with a dc voltage source (Figure 14):

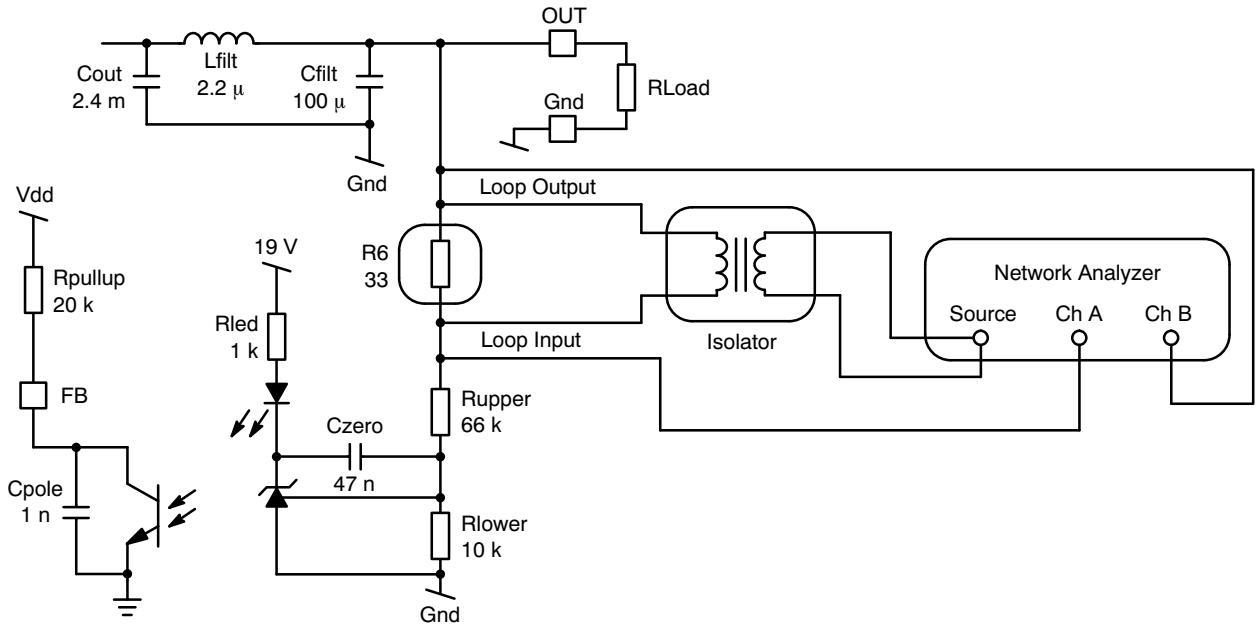

Figure 14. The Slow Lane is Individually Biased while the Second Loop is ac Swept

The injection voltage source is implemented with a wideband isolation device and a 33 Ω resistor. Voltage probes are used to measure the loop input and output signals with respect to ground. The network analyzer directly computes

$$20\log_{10}\left(\frac{\text{Ch B}}{\text{Ch A}}\right)$$

We obtained the Bode plots shown in Figure 15.

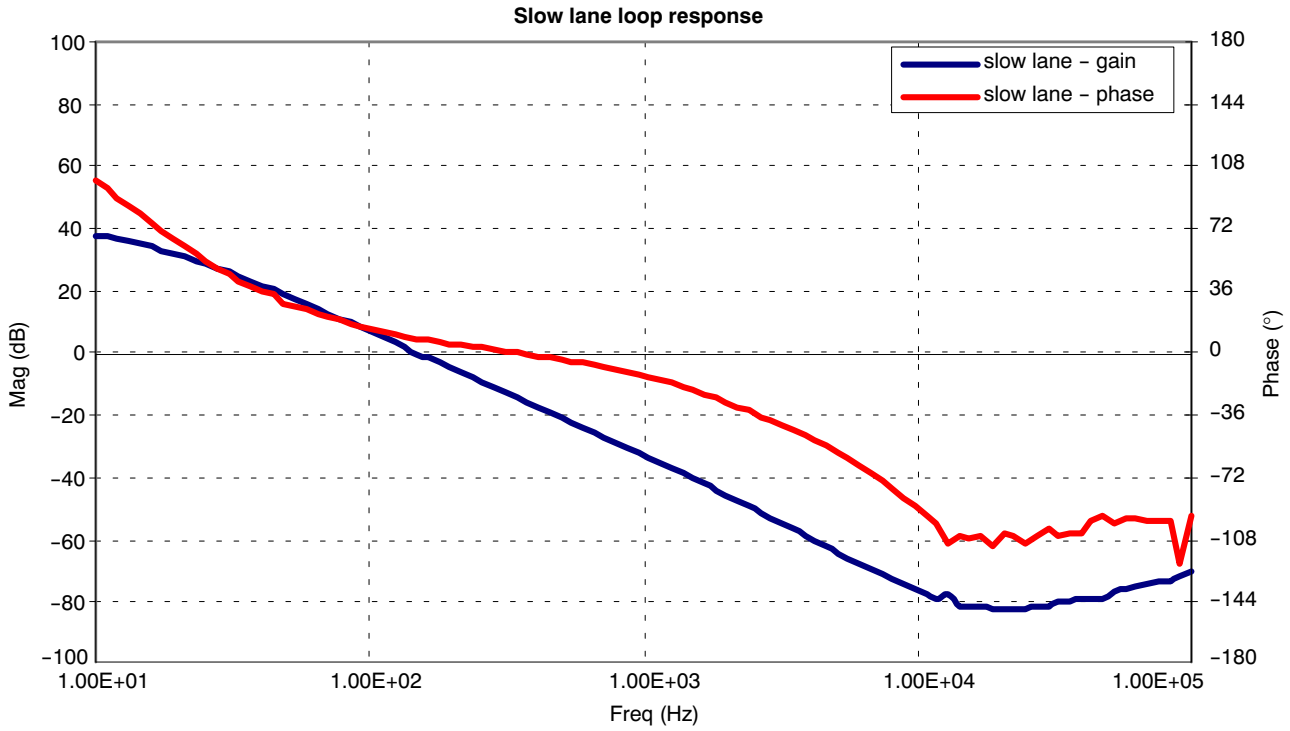

Figure 15. Slow Lane Loop Response Obtained with the Network Analyzer

The slow lane loop gain starts with a −1 slope because of the origin pole formed by ($R_{upper} = R_{12}+R_{10}$, $C_{zero} = C_6$). The power stage pole f_p is around 20 Hz and corresponds to:

$$f_p = \frac{1}{\pi R_{load} C_{out}}$$

where R_{load} is the output load resistor and C_{out} is the sum of C_{5a} and C_{5b} (Figure 13). After f_p, the power stage gain decreases with a −2 slope until it reaches the 8 kHz pole formed by (R_{pullup}, C_{pole}) of our type 2 compensator:

$$f_{pc} = \frac{1}{2\pi R_{pullup} C_{pole}}$$

Now that we have the slow lane loop plot, we can paste the network analyzer data into excel. We have a 3−column data table with the frequency (Hz), magnitude (dB) and phase (degrees). Using Euler notation, we will calculate the real and the imaginary part of the slow lane vector:

$$\overrightarrow{V_{out,slow}} = A_1(\cos\varphi_1 + j\sin\varphi_1) = x_1 + jy_1 \quad \text{(eq. 10)}$$

Excel will compute the following formulas:

$$x_1 = 10^{A_1/20}\cos\left(\varphi_1\frac{\pi}{180}\right) \quad \text{(eq. 11)}$$

and

$$y_1 = 10^{A_1/20}\sin\left(\varphi_1\frac{\pi}{180}\right) \quad \text{(eq. 12)}$$

The Excel syntax corresponding to these equations are:

$$x_1 = \text{POWER}(10; A_1/20) \cdot \text{COS}(\varphi_1 \cdot \text{PI}()/180) \quad \text{(eq. 13)}$$

$$x_2 = \text{POWER}(10; A_1/20) \cdot \text{SIN}(\varphi_1 \cdot \text{PI}()/180) \quad \text{(eq. 14)}$$

Further to slow lane measurement, we have to run the same operation for the fast lane loop. We inject the ac signal in the fast lane while the slow lane is disconnected from the output voltage and biased with a dc voltage source. This dc voltage must be manually adjusted to fix the operating point corresponding to the output load used. As the TL431 is very sensitive to small voltage variations, we can use a resistor between the dc source and the resistor divider to adjust the output voltage (See Figure 16).

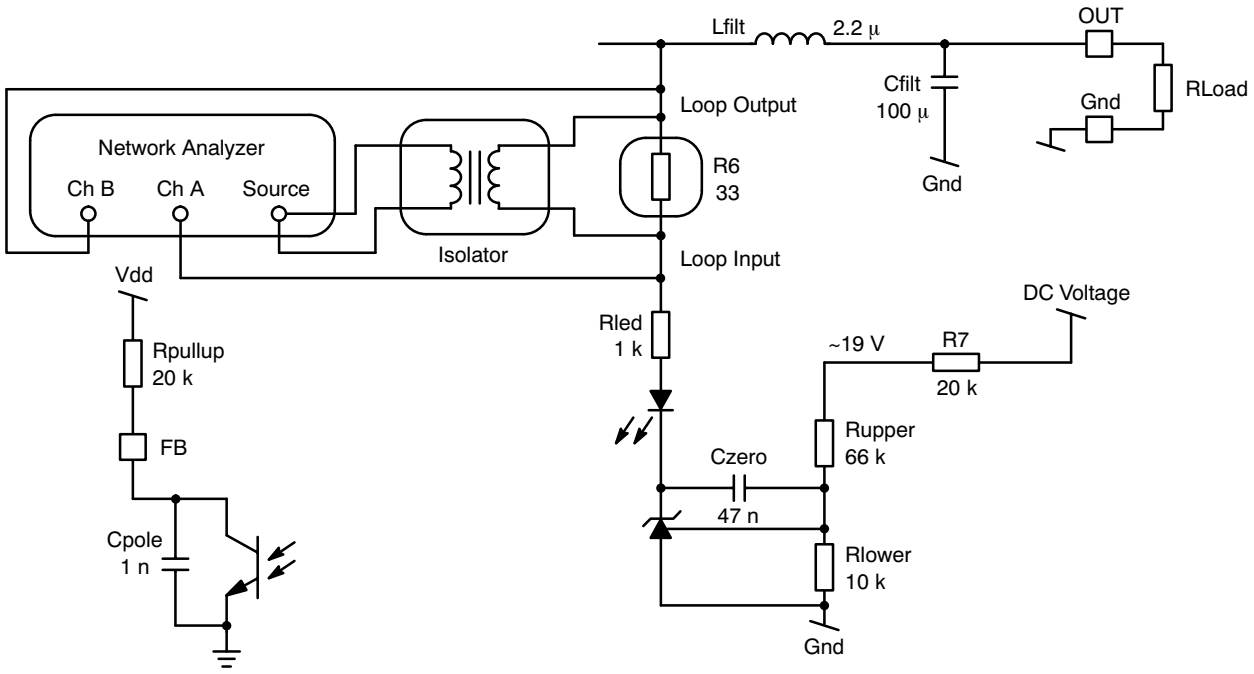

Figure 16. For the fast lane sweep, the slow lane is ac−decoupled from the converter output. Care must be taken to avoid output runaway during this measurement!

Figure 17 details the fast lane loop response. The power stage pole f_p is around 20 Hz and corresponds to:

$$f_p = \frac{1}{\pi R_{load} C_{out}}$$

After f_p, the power stage gain decreases with a −1 slope until it reaches the 8 kHz pole formed by (R_{pullup}, C_{pole}) of our type 2 compensator:

$$f_{pc} = \frac{1}{2\pi R_{pullup} C_{pole}}$$

On Figure 13 schematic, C_{pole} corresponds to C_{11} and the R_{pullup} resistor is R_7.

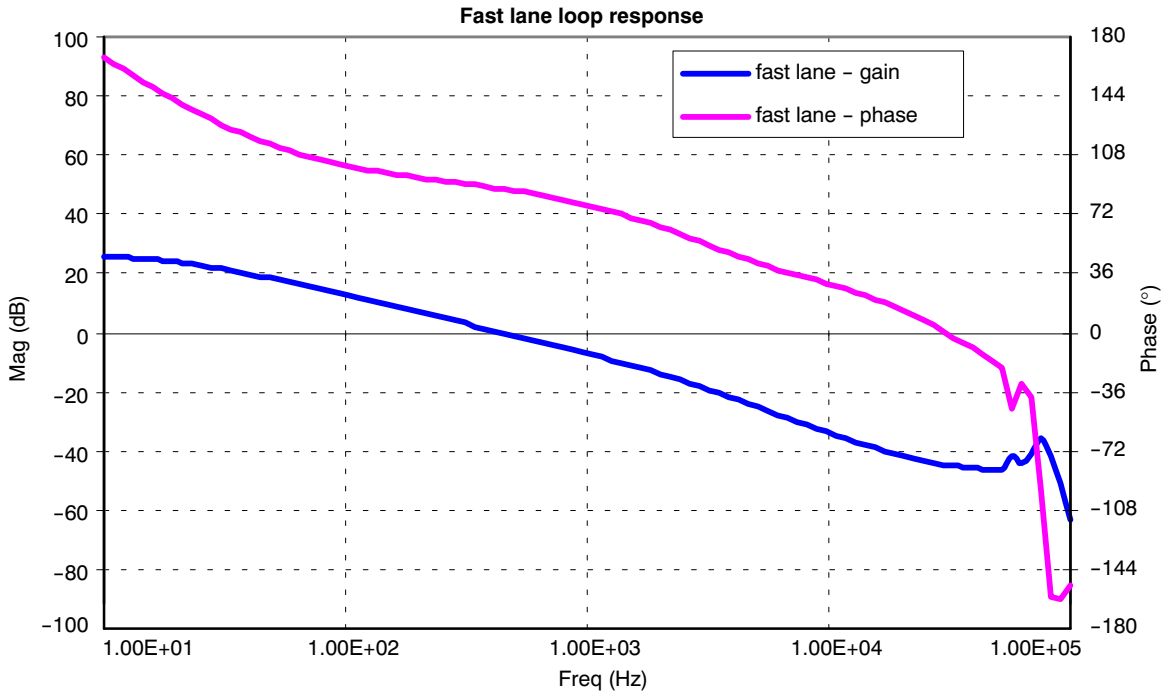

Figure 17. Fast Lane Loop Response Obtained with the Network Analyzer. The Slow Lane is Externally Biased with a dc Power Supply

Once the network analyzer data has been exported to Excel, we compute the real and the imaginary parts of the fast lane loop vector:

$$x_2 = 10^{A_2/20}\cos\left(\varphi_2\frac{\pi}{180}\right) \quad \text{(eq. 15)}$$

$$y_2 = 10^{A_2/20}\sin\left(\varphi_2\frac{\pi}{180}\right) \quad \text{(eq. 16)}$$

Then we can sum the real and the imaginary contributions to obtain the total loop vector:

$$\overrightarrow{V_{FB}} = (x_1 + x_2) + j(y_1 + y_2) = X + jY \quad \text{(eq. 17)}$$

Finally, we extract the final loop gain and phase by entering Equations 8 and 9 in Excel:

$$Loop_{gain} = 20 * LOG(SQRT(X \wedge 2 + Y \wedge 2); 10) \quad \text{(eq. 18)}$$

$$Loop_{phase} = DEGREES(ATAN(Y/X)) \quad \text{(eq. 19)}$$

Figure 18 shows the reconstructed loop gain and phase plots.

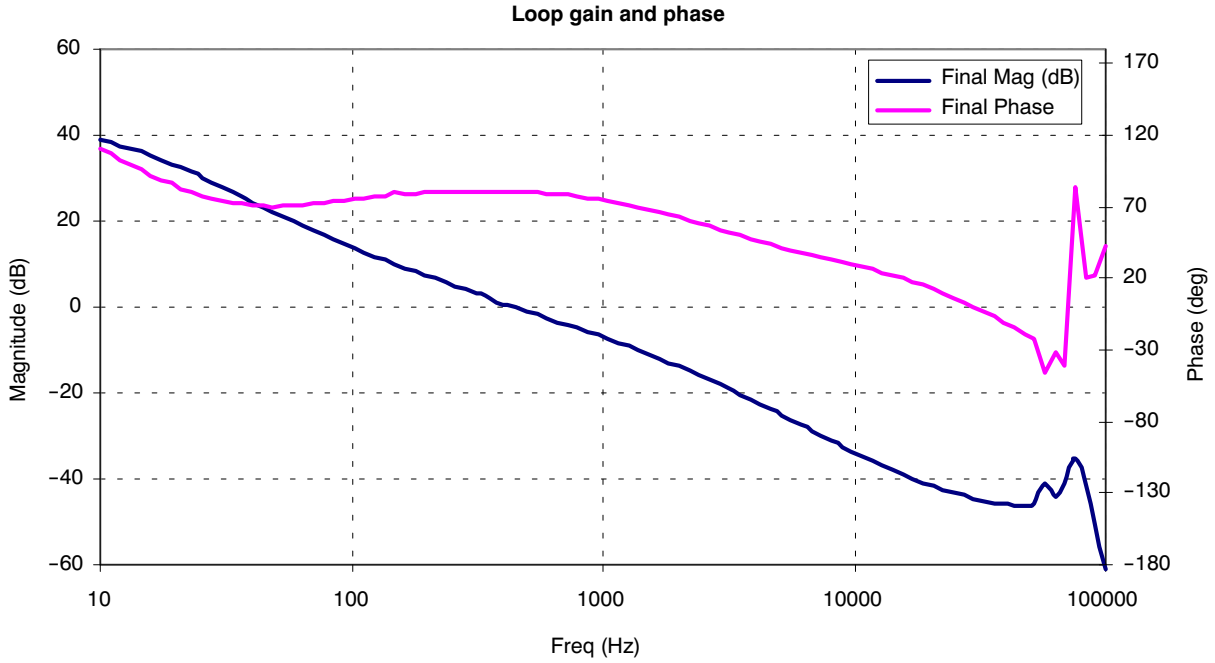

Figure 18. The Final Bode Plot Combines the Information Obtained from Individual Loop Measurements

Because the arctangent function is defined on a]−90°; +90°[interval, some parts of the resulting curve could exhibit a negative phase rotation caused by the calculation. We have corrected these particular points by adding 180° to their phase calculation result. The reconstructed Bode plot shows a clean response and does not differ from classical loop analysis carried on a current−mode converter.

Weighted Feedback on a Forward Converter

Let's now apply a similar methodology to a multi−output power supply: in such an application, two different voltage outputs are regulated using a common TL431, using a weighted sum configuration (see Figure 19). The resistors connecting each output to the TL431 reference pin are calculated taking into account a relative weight of each output in the feedback.

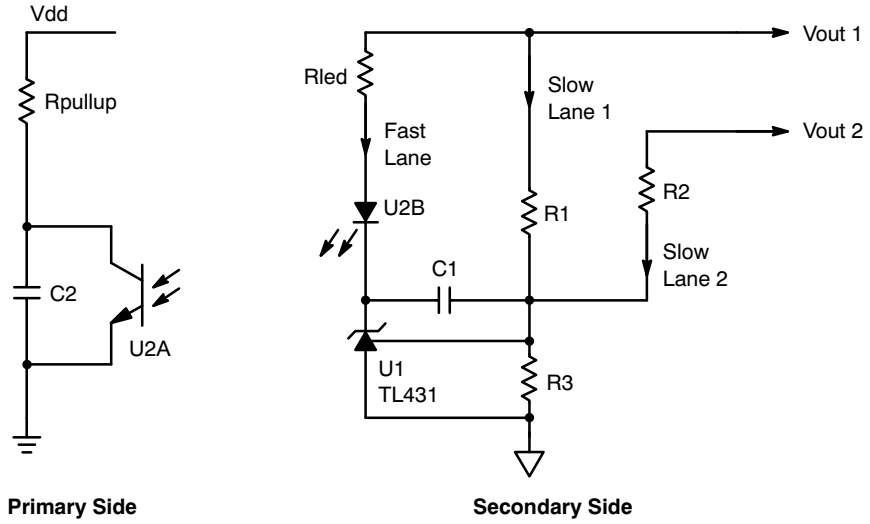

Figure 19. The TL431 Wired in a Two−output Weighted Feedback Configuration

This technique offers a way to improve cross−regulation in a multi−output converter by affecting a weight to certain outputs whose precision or load constraints are more important than the others. Of course, the sum of all weight must equal 100% at the end. In the ATX world, weighted feedback is often encountered in the so−called Silver boxes and Figure 20 represents a simplified two−output version of such a converter. In this 2−switch forward converter, the two outputs (5 V and 12 V) are also coupled via their respective output inductors. Each output contributes to 50% in the control loop, which uses a TL431 featuring a type 2 compensation.

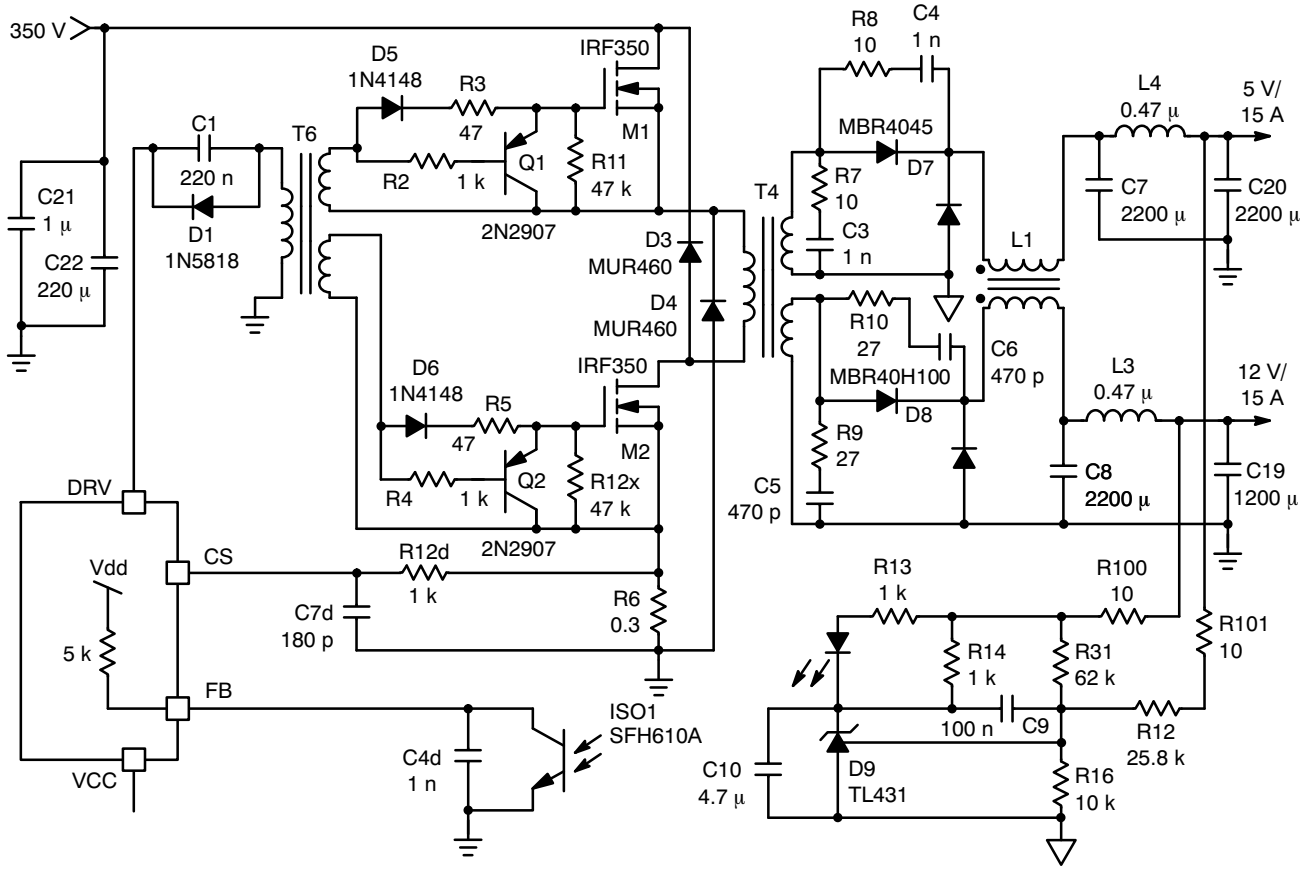

Figure 20. Schematic of the Two−switch Forward Power Supply featuring a Weighted Feedback with TL431

There are 2 loops we need to measure: one is a combination of the fast and slow lanes observing the +12 V output. The other one is the +5 V loop entering the TL431 via the slow lane.

We have mentioned before that measuring the loop at the feedback input of the controller is not practical. As demonstrated in Ref. [3], in order to correctly measure the gain and phase of the feedback loop, the ac stimulus must be injected between a low impedance node (on the power supply output side) and a high impedance node (on the control side). When the injection is done as described previously, i.e. between the output of the power supply and the feedback circuitry, the condition is optimal: the output impedance of the observed point is low, and the input impedance of the feedback path is high. But if we want to open the loop between the optocoupler and the feedback pin of the controller, the conditions are not favorable: the output impedance of the optocoupler is high (this is the pull up resistor in a common−emitter configuration), whereas the input impedance of the FB pin can sometimes be affected by internal dividers or pull−up resistors (it was 5 kΩ in our example). We can anyway find a way to perform this measurement by inserting a buffer between the optocoupler and the controller as Figure 21 illustrates. Using an NPN transistor in a common−collector configuration, the output impedance is made low compared to the input impedance of the feedback pin.

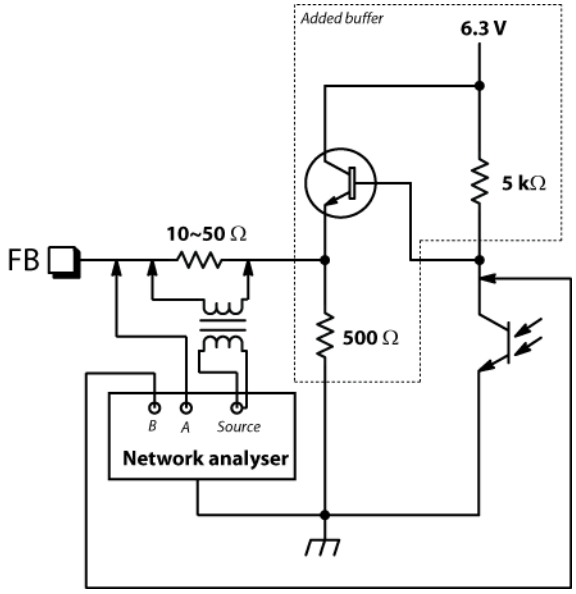

Figure 21. An NPN Buffer Allows Performing the Loop Gain Measurement on the Primary Side

The result is plotted on Figure 22. This loop measurement done at the feedback pin is clearly not correct: the gain plateaus at low frequencies; and the phase increases again at higher frequencies, so much that the gain margin cannot be measured. This is clearly not a valid measurement.

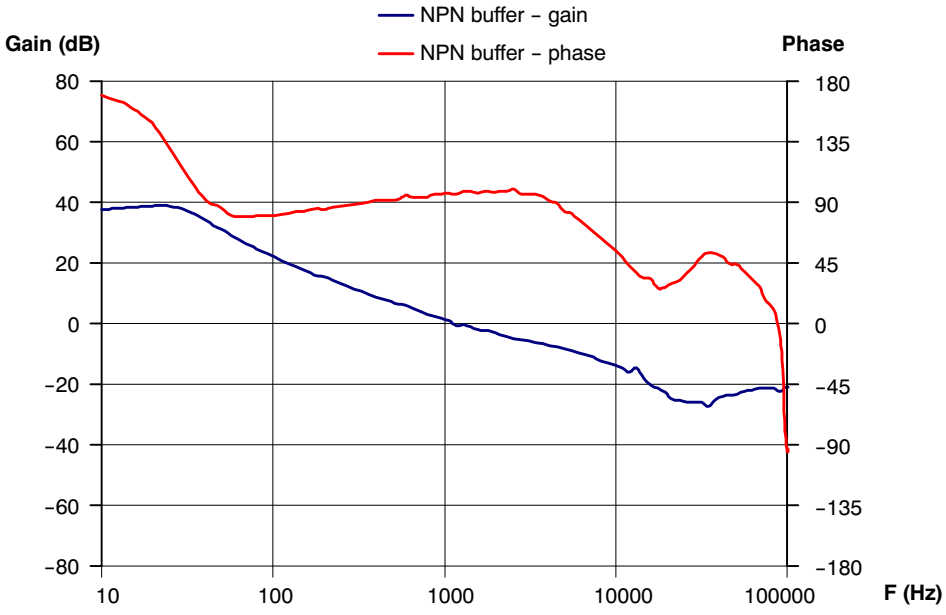

Figure 22. Bode Plot Obtained using the NPN Buffer on the Primary Side

We will now measure one of the two loops independently, while biasing the other one with an external dc supply, as we did before. Individual measurement results are shown on Figures 23 and 24. Combining the two using the Excel® spreadsheet delivers the result of Figure 25.

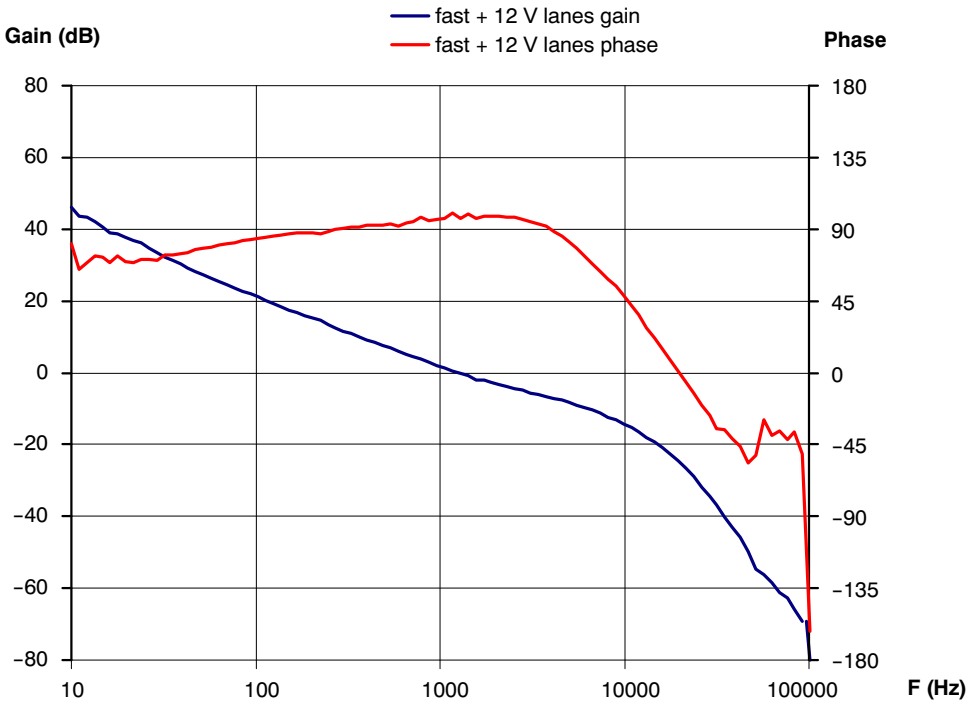

Figure 23. Fast Lane and 12 V Slow Lane Loop Response Obtained with the Network Analyzer

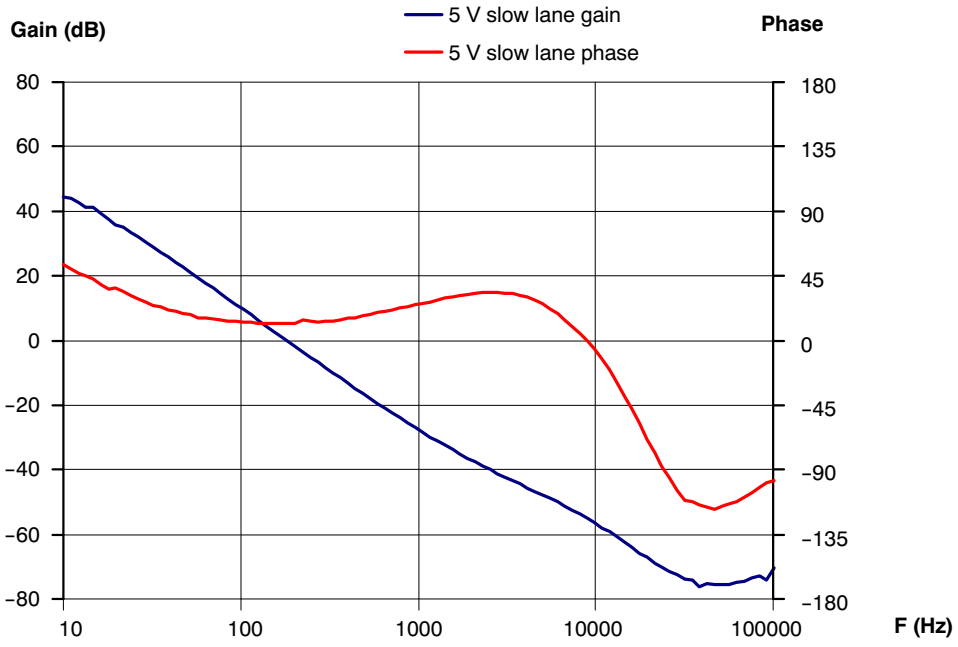

Figure 24. 5 V Slow Lane Loop Response Obtained with the Network Analyzer

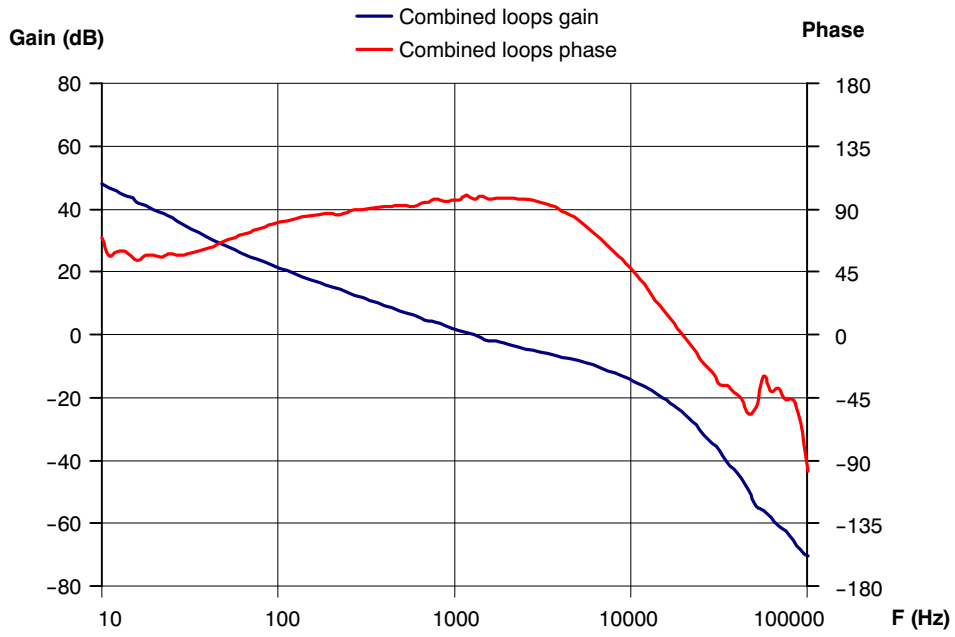

Figure 25. The Final Bode Plot Combines the Information Obtained from Individual Loop Measurements

As expected, the 2−loop measurement is now valid over the whole frequency range, with a constant slope of −20 dB per decade for the gain at low frequency, and a phase that keeps on decreasing after the crossover frequency. To verify the validity of the approach, we have gathered Figure 25 and Figure 22 on a common graph which appears on Figure 26. The gain and the phase curves in the vicinity of the cross over frequency are similar.

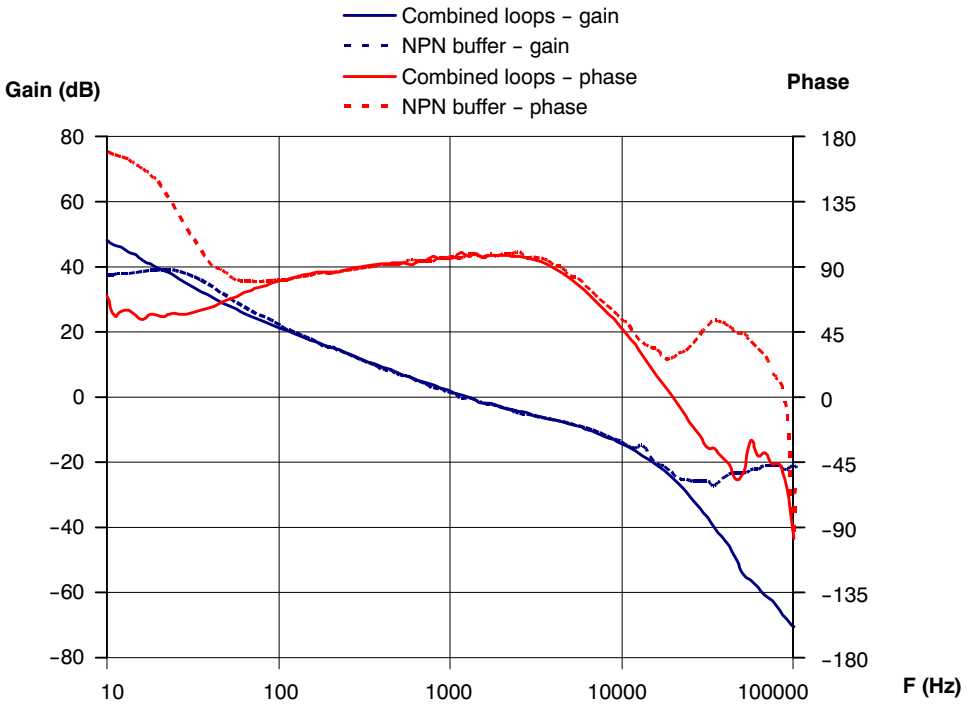

Figure 26. Comparing the Combined Bode Plot Obtained from Individual Loop Measurements to the Primary Measurement (with NPN Buffer)

Conclusion

Measuring the frequency response of a multi−loop switch−mode power supply can be a real challenge, especially when all the regulation circuitry is kept on the secondary side. This is often the case with modern current mode controllers where the feedback input directly controls the peak current. Hopefully a simple method exists which combines individually measured loops with a simple mathematical manipulation. As demonstrated in this paper, this method is applicable to a wide range of applications.

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