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NCP1351 Modeling Using the PWM Switch Technique

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APPLICATION NOTE

This document describes the average modeling of the NCP1351 a fixed on time / variable off time controller. The advantage of using an average model is that you can perform ac simulations of your power supply to study the stability of your system. Another advantage is that transient simulations with the averaged model are faster compared to transient simulations with a cycle−by−cycle model. The model is very simple to use and can be downloaded from ON website.

Presentation of the PWM Switch Technique

The Pulse Width Modulation switch model was developed by Vatché Vorpérian (Jet Propulsory Laboratory, Passadena, CA) in 1986. His approach consisted in modeling the switch network alone (power switch + diode) by averaging the voltage and current waveform in the circuitry.

He obtained a 3 terminal model (node A, C and P) where:

- Node A represents the active node, the switch terminal not connected to the diode
- Node C is the common node, the junction between the power switch and the diode
- Node P is the passive node, the diode terminal not connected to the switch

The input variables are the current in node A, the voltage V_{ap}; the output variables are the current in node C and the voltage V_{ap} (Figure 1).

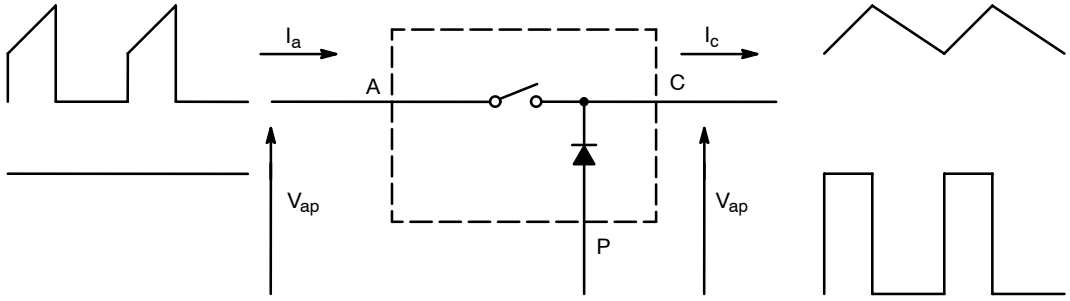


Figure 1. PWM Switch and its Variables

The PWM switch is invariant i.e. the PWM switch electrical structure is the same whatever converter we consider. For this reason, we will use a buck−boost converter for the study, because of simplicity but also because the flyback topology where the NCP1351 is used is derived from buck−boost.

Modeling the Switching Network

Figures 2 and 3 show the switching network in the buck−boost circuit and its equivalent implementation in PWM switch.

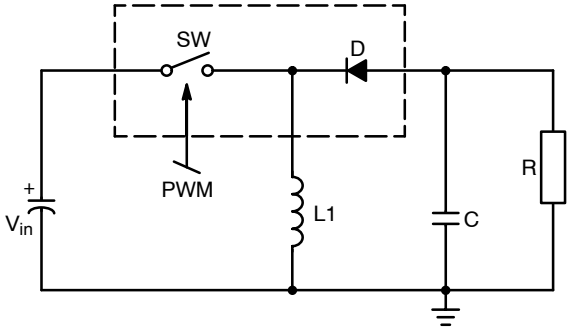


Figure 2. Buck−Boost Converter

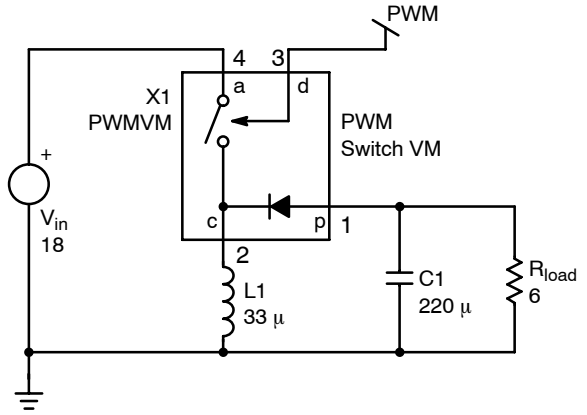


Figure 3. PWM Switch in the Buck−boost Converter

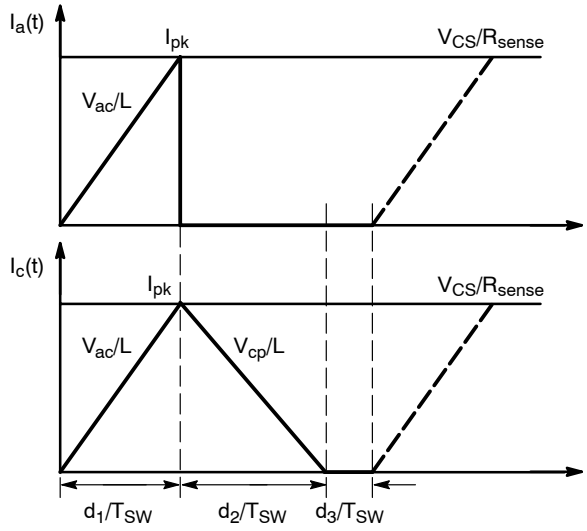


Figure 4. The Current Waveforms in DCM: I_a, I_c

The average current flowing in the C terminal is given by the following equation [1]:

$$I_C = \frac{V_{CS}}{R_{sense}} - d_2 T_{SW} \frac{V_{CP}}{L}\left(1 - \frac{d_1 + d_2}{2}\right) \quad \text{(eq. 1)}$$

According to Figure 4, the following expressions for the terminal voltages and currents can be easily verified [2]:

$$V_{ac} = L\,\frac{I_{PK}}{d_1 T_{SW}} \quad \text{(eq. 2)}$$

$$V_{cp} = L\,\frac{I_{PK}}{d_2 T_{SW}} \quad \text{(eq. 3)}$$

$$I_a = \frac{I_{PK}}{2}\,d_1 \quad \text{(eq. 4)}$$

$$I_c = \frac{I_{PK}}{2}\,(d_1 + d_2) \quad \text{(eq. 5)}$$

The average current in terminal A is deduced from equations (4) and (5):

$$I_a = I_c\,\frac{d_1}{d_1 + d_2} \quad \text{(eq. 6)}$$

Once the switch network has been identified in the original circuit, a simple rotation of the PWM switch model leads to the final implementation. This step is necessary to unveil the various variables in play.

Averaging the PWM Switch Waveforms

NCP1351 is a fixed peak−current variable−t_{off} current−mode converter without internal ramp compensation. We will first consider the DCM mode to derive the equations since further developments will show that the model automatically toggles from DCM to CCM. The method consists of identifying current, voltage waveforms in the switch terminals (Figure 4 and Figure 5) and averaging them over one switching period.

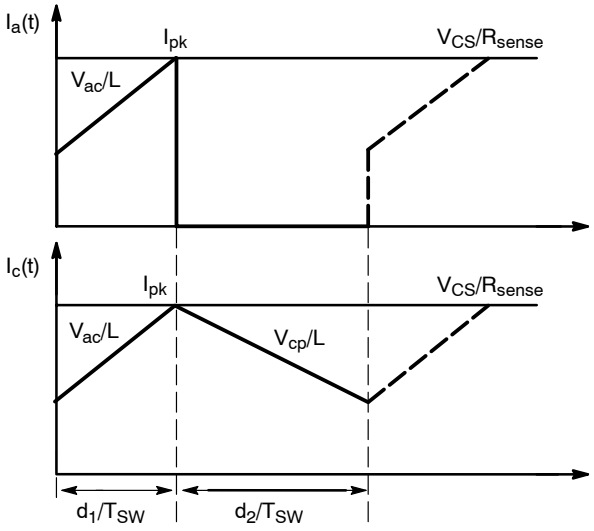


Figure 5. The Current Waveforms in CCM: I_a, I_c

The average on−time duty cycle d_1 is solved from Equations (2) and (3)

It is necessary to clamp the duty cycle d_1 value between 0.01 and 0.9 (1 to 90% duty−cycle) to avoid convergence issues.

$$d_1 = \frac{d_2 V_{cp}}{V_{ac}} \quad \text{(eq. 7)}$$

d_2 expression is derived from Equations (2) and (5)

$$d_2 = \frac{2 L I_c}{d_1 T_{SW} V_{ac}} - d_1 \quad \text{(eq. 8)}$$

We clamp d_2 value between 0.01 and $(1- d_1)$. When d_2 is equal to $(1- d_1)$, we are in CCM [1].

In the NCP1351, the loop controls the switching frequency by adjusting the end−of−charge voltage threshold of the C_t capacitor (see Figure 6). The capacitor is charged by a constant current source I_{Ct} and the threshold voltage V_{fbint} is proportional to the feedback current injected into the FB pin by the optocoupler.

The switching period equation is:

$$T_{SW} = \frac{C_t V_{fbint}}{I_{ct}} \quad \text{(eq. 9)}$$

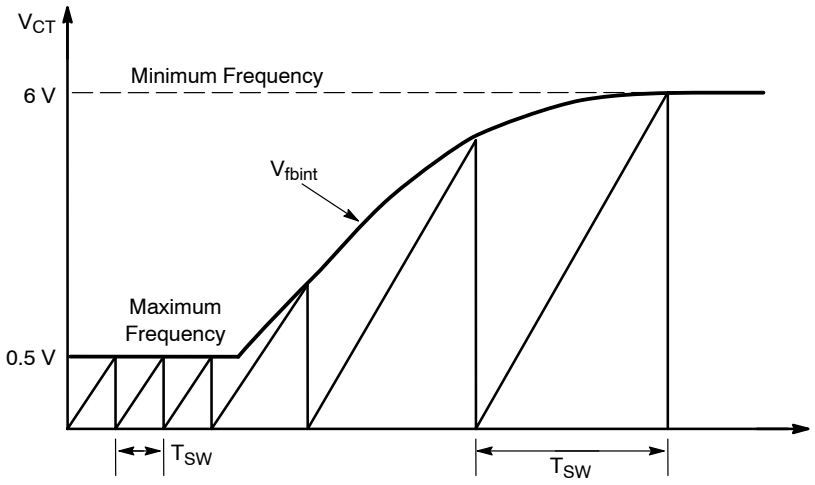


Figure 6. The Switching Frequency is Controlled by the Charge of Ct Capacitor

NCP1351 is a current mode converter without ramp compensation. The controller is thus subject to subharmonic oscillations when operating in CCM. The subharmonic oscillations are modelled by a capacitor connected between C and P terminal during CCM. The capacitor value is frequency−dependent and is calculated by the following expression [3]:

$$C_S = \frac{4}{L(\pi F_{SW})^2} \quad \text{(eq. 10)}$$

A separate in−line equation disconnects the capacitor during DCM. The electrical implementation of all the equations derived above is shown on Figure 7.

Modeling the FB Section

To avoid acoustic noise problems, the NCP1351 compresses the peak current as the load becomes lighter. From the datasheet, we can extract the values of CS current as a function of FB current.

$$I_{CS} = \begin{cases} 250\ \mu A \text{ if } I_{fb} < 60\ \mu A \\ 790\ \mu A - 9\ I_{fb} \text{ if } 60\ \mu A < I_{fb} < 80\ \mu A \\ 70\ \mu A \text{ if } I_{fb} > 80\ \mu A \end{cases} \quad \text{(eq. 11)}$$

A behavioral current source is used to model I_{CS}. The model for the peak current compression is shown on Figure 8.

The feedback current controls the switching frequency by changing the timing capacitor end−of−charge−voltage V_{fbint}. To do so, the optocoupler injects current into the FB pin which is actually a bipolar current−mirror input. This current is then adjusted by the feedback loop depending on the operating region (full power, compression or standby). The resulting current flows into a 45 kΩ resistor which develops a voltage proportional to the FB current. This signal becomes the C_t capacitor ending voltage.

Thus, the relation between feedback current I_{fb} and V_{fbint} is:

$$V_{fbint} = V_{offset} + 45\ kI_{FB} \quad \text{(eq. 12)}$$

It is also important to model the pin FB current mirror because the dynamic resistance of the input mirror transistor directly influences the loop gain. Figure 7 shows the way we implemented the model of the FB modulator.

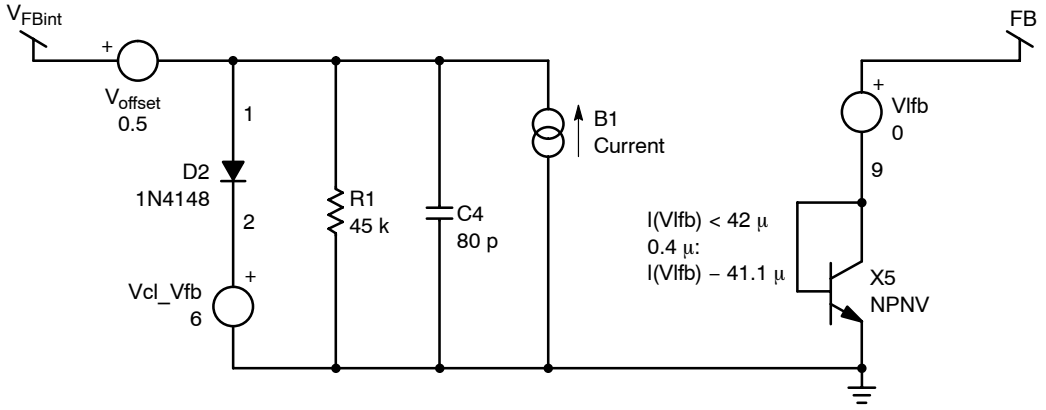


Figure 7. Feedback Modulator Model

Complete Average Model and Application

The complete averaged model of NCP1351 is shown below.

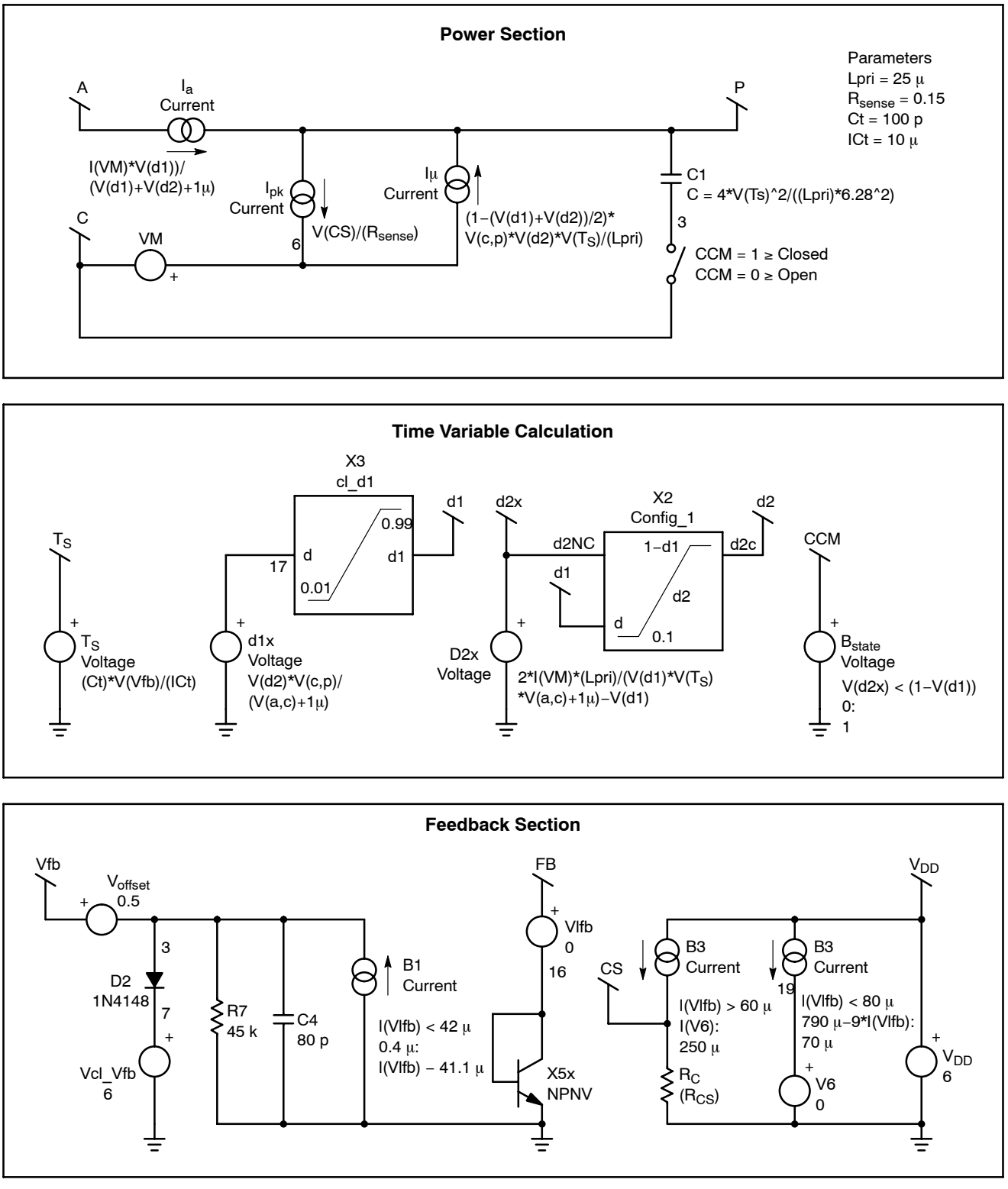


Figure 8. Complete Averaged Model of NCP1351

All the elements in Figure 8 are encapsulated into a subcircuit as shown below:

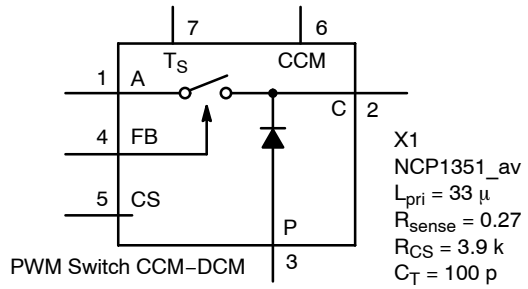


Figure 9. The PWM Switch Encapsulated into a Sub Circuit

- A, C and P are the power terminals.
- FB is the feedback input. Connect it to optocoupler emitter.
- The CCM pin indicates the operating mode (CCM or DCM):
  1. if equal to “1”, the converter is in CCM
  2. if equal to “0”, the converter is in DCM
- Ts and CS respectively indicate the switching period (1 μV = 1 μs) and the CS level. Place voltage probes on the schematic to see their values or display the operation bias points

The model expect the values of your primary inductance, sense and CS resistors and the value of the timing capacitor C_t. Defaults values for these parameters are indicated on Figure 9.

The Model in a Flyback Converter

The following schematic describes the NCP1351 averaged model implementation in a flyback converter. This schematic can be downloaded from the website. Then, you will just need to enter your own power supply design values in the different components.

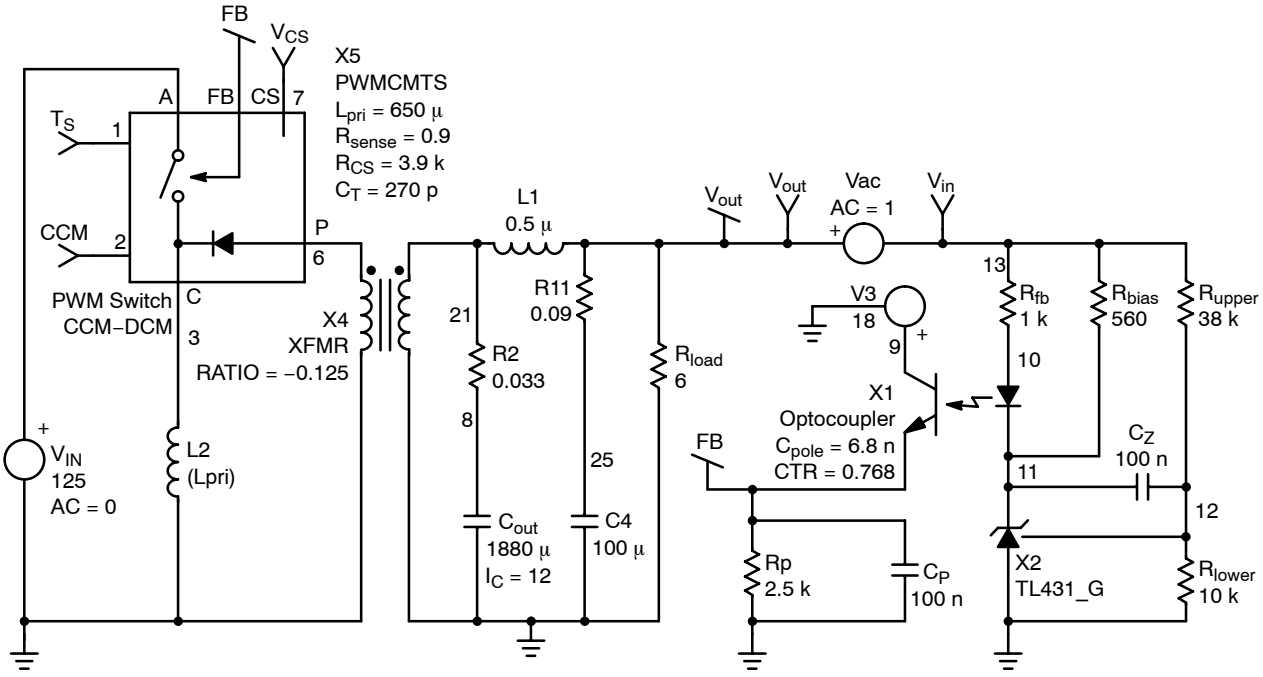


Figure 10. The NCP1351 Model in a Flyback Converter

As an example we implemented a 12 V, 2 A flyback converter with secondary output filter. For the feedback, we have chosen a TL431, but you can also use a zener diode. R_p is the optocoupler pulldown resistor and C_p places a pole in the compensation transfer function. Typical values for these components are shown on the schematic. We have also represented the ESR of output capacitors to be closer to real application and also because it influences the ac response of the power stage.

Validating the Model: Model versus Reality

In order to test the model, we built a 20 W buck−boost converter with NCP1351 as the MOSFET controller. The design specifications are:

Input voltage: 16 V – 20 V dc

Output voltage: 12 V @ 1.7 A

As we used a P−channel MOSFET for the power switch, the DRV signal from NCP1351 needs to be inverted. We selected a MC33151 for that purpose. The output power is regulated with a zener diode and an optocoupler. The optocoupler simplifies the FB path as we need to pull the FB up from a negative output voltage.

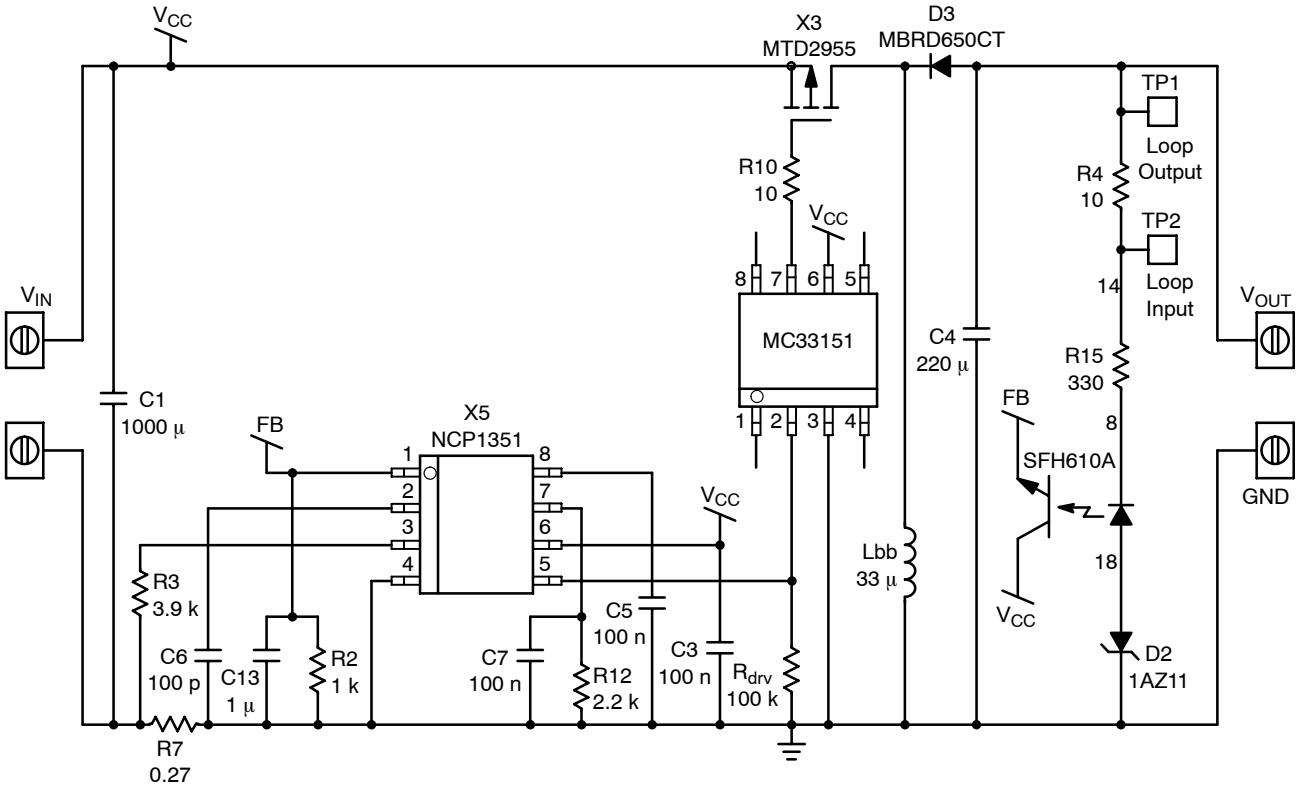


Figure 11. The Buck−boost Board Application Schematic Shows an Optocoupler in the FB Chain

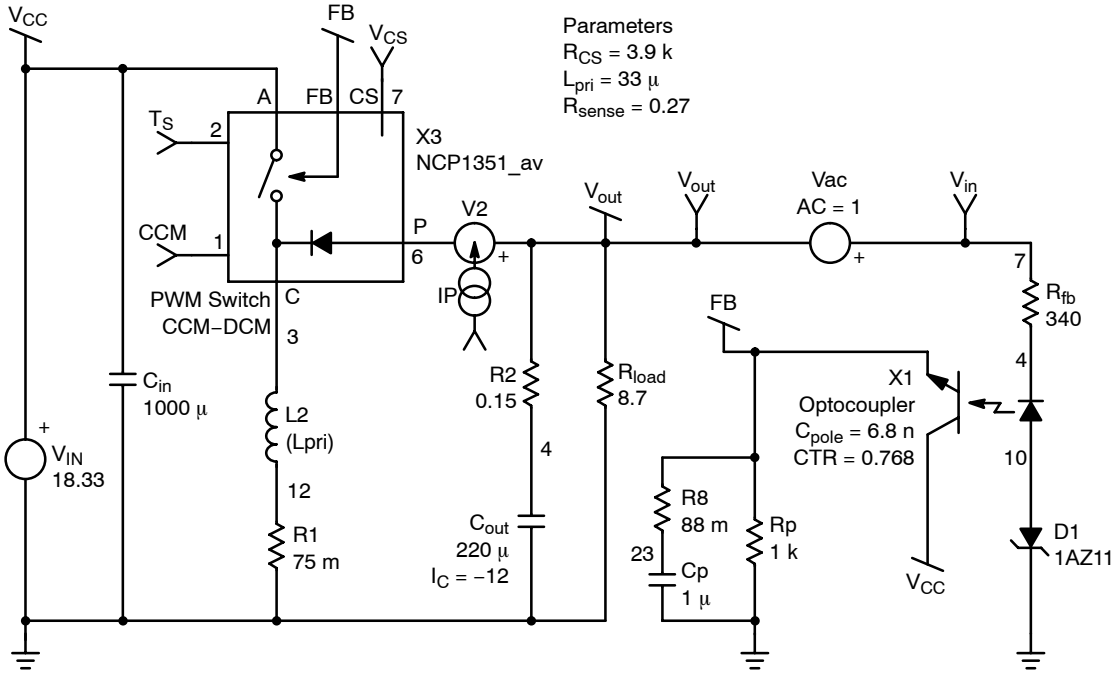


Figure 12. The Buck−boost Model Implemented in SPICE

As we said in the previous section, it is important to include the dc resistance of the self and the ESR of the capacitors in the model to better fit reality.

Operating Point

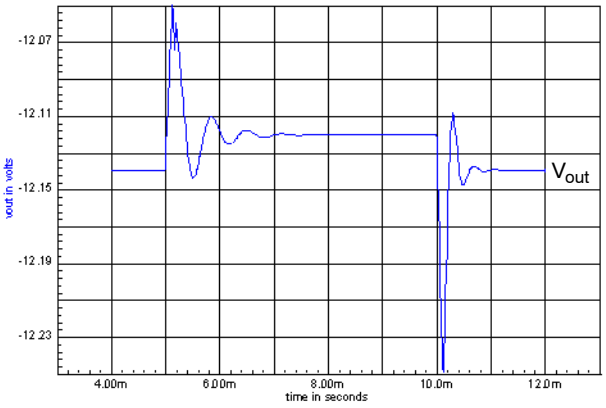
We ran operating point simulations for different loads. We obtain the following results for the switching period:

Load Current – I_{load}	Simulated Period – T_{sw}	Measured Period – T_{sw}
1.4 A	11.7 μs	13.7 μs
0.6 A	17 μs	17.4 μs
0.09 A	22.3 μs	21 μs

In high current conditions, the forward drop voltage in the diode and the ohmic losses in the MOSFET can degrade the bias point as these effects are not taken into account in our model. However, at a low output current, these losses become negligible and the simulation better fits the measurement.

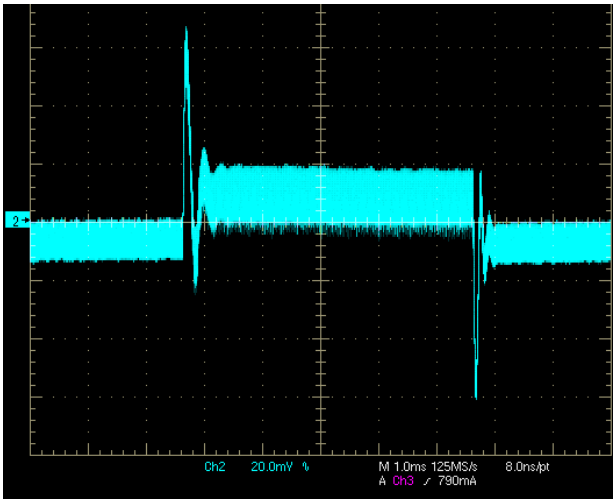
Load Step Response

We compared the simulated and the measured response for a load step from 0.5 A to 1.4 A swept with a slew−rate of 10 mA/μs (Figure 13 and Figure 14).



Scale : Y = 20 mV / div, X = 1 ms / div

Figure 13. Simulated Load Step Response



Scale : Y = 20 mV / div, X = 1 ms / div

Figure 14. Measured Load Step Response

The simulated results are very close to measurements. The first voltage peak corresponding to a transition from 0.5 A to 1.4 A is well predicted with a simulated value of 80 mV versus 70 mV for the measurement. For a transition from 1.4 A to 0.5 A, the model is less precise and the simulation response is 40 mV higher than the measurement. This may come from the internal C_s capacitor that is brutally disconnected between C and P terminal since we are toggling from CCM to DCM. A solution would be to disconnect this capacitor for transient simulations only.

Measuring the Loop Response

The loop measurement represents an important task to confirm the validity of the assumptions during the theoretical design stage. The measurement principle is shown below:

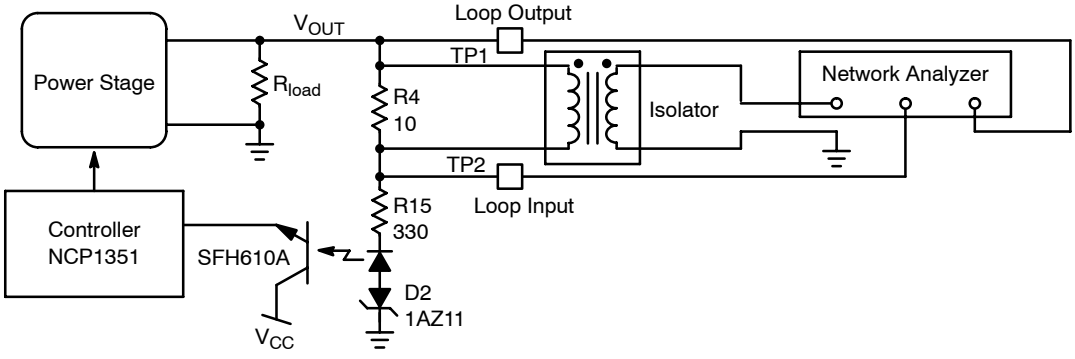


Figure 15. Loop Response Measurement Principle

The voltage injection source is implemented with a wide band isolation device together with a 10 ohm resistor. See reference [4] for more information about this technique. Voltage probes are used to measure the loop input and output signals with respect to ground on either side of the injection point.

Results in CCM

To obtain correct measurements, it is necessary to choose an operating point outside the peak current compression zone. We have selected V_{in} = 18 V and a output current of 1.4 A. The switching frequency is 73 kHz. The below figures represent the measured and simulated loop gain and phase for a 1.4 A output current.

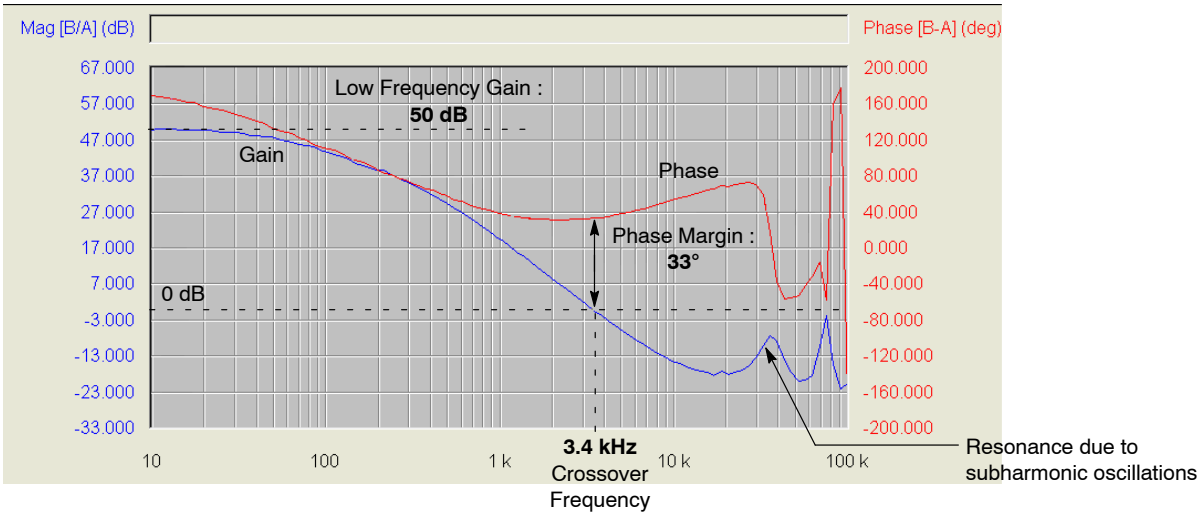


Figure 16. Measured Loop Response in CCM

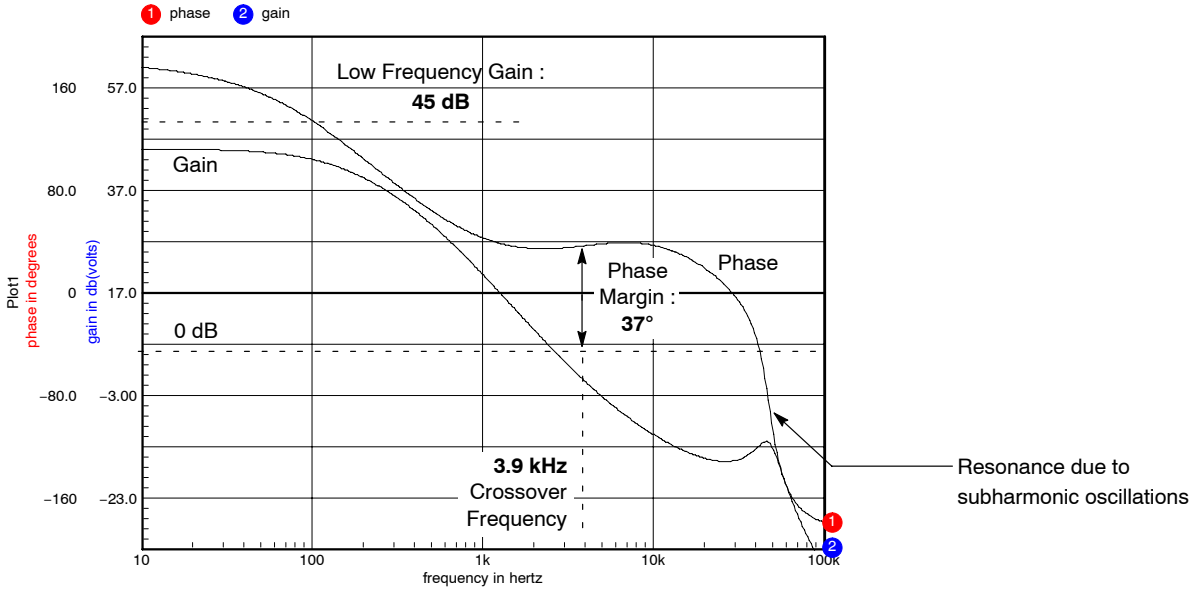


Figure 17. Simulated Loop Response in CCM

The simulated loop response is very close to reality. We have a variation of 10% between measurement and reality, which is acceptable because what we need is an indication about phase margin (greater than 455) and crossover frequency to be sure we will remain stable in all operating cases. In our example, we have a phase margin smaller than 455. This is clearly not acceptable as a design goal but as our primary aim was to validate the model, we did not pay a particular attention to improve this figure.

Results in DCM

We also compared the simulated and measured loop response in DCM for a 0.06 A output current. The input voltage is 18 V and the switching frequency is 33 kHz (Figure 18 and Figure 19).

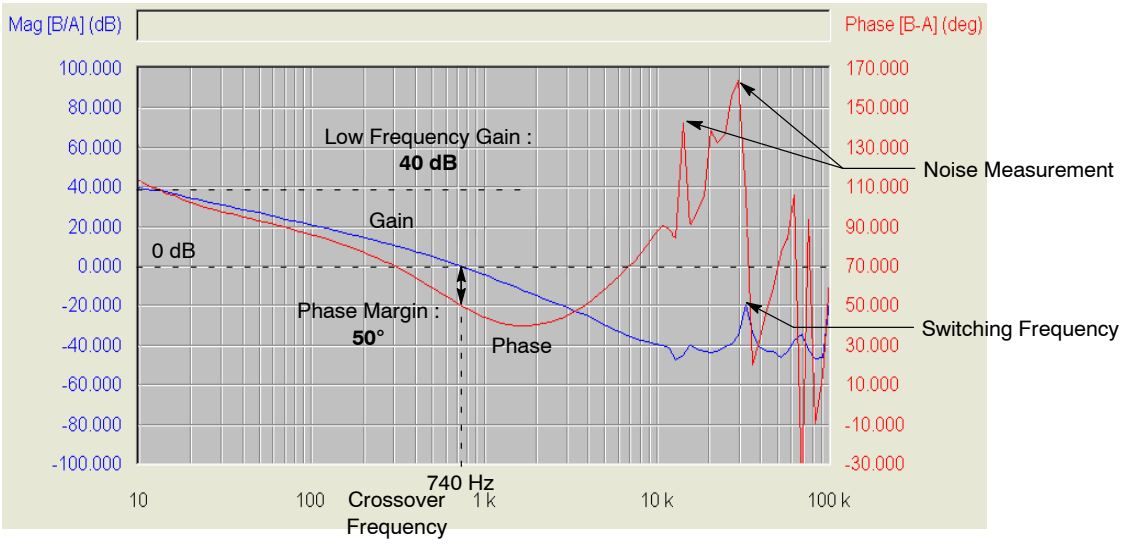


Figure 18. Measured Loop Response in CCM

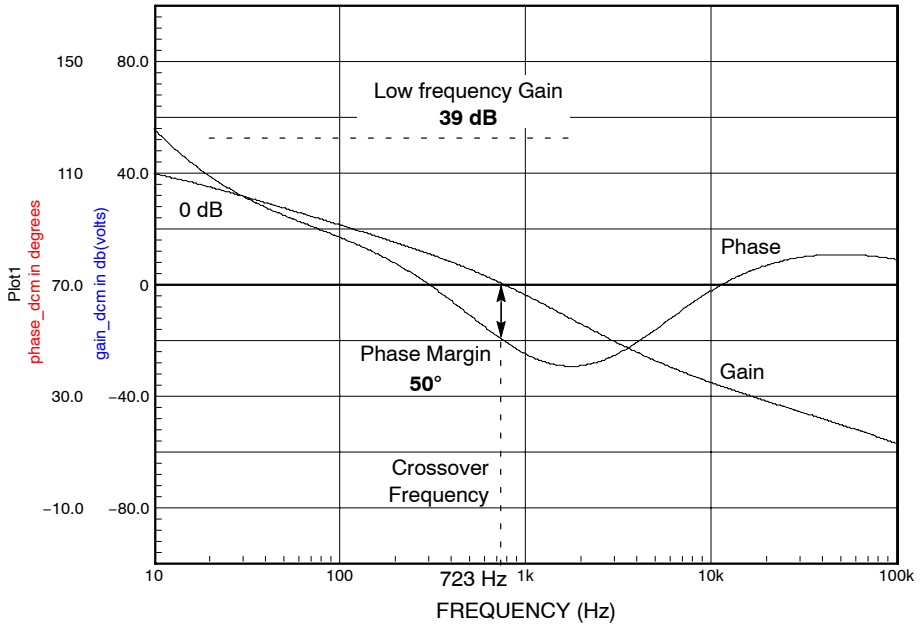


Figure 19. Measured Loop Response in DCM

Again, we have a good correlation between measured and simulated loop response in DCM. The error ratio between simulation and measurement is less than 2%, the model is thus accurate to predict the DCM behavior. Here, we have a greater phase margin because the right half plane zero in the control to output transfer function of the buck−boost disappears, thus improving the system stability.

Conclusion

An averaged model of NCP1351 has been derived using the PWM Switch modeling technique.

The model has been validated by experimental measurements on a buck−boost converter using NCP1351 as the controller. Several aspects of the model have been tested and compared to measurements: operating point, load step, and loop gain and phase response. There is a good correlation between the model and the measurements. We can conclude that the model is a good tool to predict the small−signal response of a NCP1351−based power supply.

This model has been derived using INTUSOFT's IsSpice and CADENCE's OrCAD. Both versions are uploaded on ON Semiconductor website (www.onsemi.com). A cycle−by−cycle model also exists and is available from the same location.

References

1. Christophe Basso, “The PWM Switch concept included in mode transitioning SPICE models”, PCIM 2005
2. Vatché Vorpérian, “Simplified Analysis of PWM converters using the model of the PWM switch, Part I (CCM) and II (DCM)”, Transactions on Aerospace and Electronics Systems, Vol 26, N°3, May 1990.
3. Vatché Vorpérian, “Analysis of current−mode controlled PWM converters using the model of the current−controlled PWM switch”, Power Conversion October 1990 proceedings.
4. www.ridleyengineering.com

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