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A Comparison of LVDS, CMOS, and ECL

Prepared by: Fred Zlotnick
ON Semiconductor

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APPLICATION NOTE

INTRODUCTION

ECL is a high performance technology that has been available for the designer since the 1960s. It has always been at least an order of magnitude better in propagation delay and skew when compared with CMOS and TTL logic. ECL is fabricated with unsaturated logic and low–level differential drive. Its performance is a vast improvement over all other logic families. In the late 1960s, when the standard TTL family offered 20 ns gate delay and the CMOS 4000 family had delays of 100 ns or more, MECL–10K offered 1 ns delay. Since then, CMOS logic families have progressed remarkably and now offer approximately ~2 ns delay. However, ECL logic is now at 150 ps delay, still 25 times faster than similar function CMOS.

ECL and Positive ECL (PECL) are the same product. All ECL can be run as PECL. It was commonplace to run ECL at –5.2 V, but this was never necessary. Modern ECL is quite different from MECL–10K. There were three common schemes: –5.2 V, +5.0 V (PECL), and +3.2 V. Operating voltage is now down from 5.2 V to as low as 2.5 V. Unlike CMOS, bipolar ECL parts do not degrade with lower voltage. As long as the device is specified to operate at that voltage, performance is substantially the same at any voltage within the operating range. The critical speed/delay specifications on a modern low–voltage ECL device are the same at 2.5 V as 3.3 V.

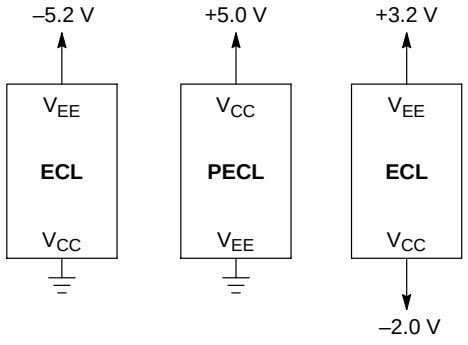

Figure 1. MECL–10 0K Same Product Used With Different Supply Options

ECL has used differential signaling since its inception. The output of an ECL device is taken from an emitter, and is normally about 50 Ω. Since the source impedance of the driver was a close match to most transmission wires, it was only necessary to terminate the line at the receiver input. This case represents a doubly–terminated transmission line, the ideal case. The signaling level is +/–.400 V. Designers using ECL logic usually designed 50 Ω traces or twisted pairs and terminated with a 50 Ω resistor.

As with CMOS, today's ECL is designed with very small, sub–micron transistors. Since older ECL (such as MECL–10K families) used junction isolation with large parasitics, large amounts of current were needed to overcome the parasitics. Modern ECL uses oxide isolation techniques, thereby reducing parasitics considerably and raising the operating range of the devices. Oxide isolation and the very high f_τ of the devices combine to lower the power and raise the frequency of the device. Many of today's ECL gates can be toggled at >3.0 GHz.

CMOS technology was created in the 1960s and began life as the venerable 4000 series. CMOS was low power and slow. Clocking rates beyond 10 MHz was rare. These devices used 10 μ "metal gates." As technology progressed, poly–silicon gates replaced metal gates and the geometry shrank to today's sub–micron size. Products like ALVC/VCX use 0.5 μ or smaller geometry and offer 2 ns delay and 24 mA of drive. VCX parts have toggle frequency specifications of >150 MHz.

CMOS became the workhorse of the semiconductor industry. One of the severe limitations to speed and power was the "rail–to–rail" operation of standard CMOS. A VCX or ALVC device, driving from rail–to–rail from a 3.3 V supply, swings in excess of 2.0 volts. In order to overcome the capacitance typically found on a bus structure, a terminating resistor is used. To get the fastest speed possible, a resistor of 100 Ω is usually selected to drive 24 mA per circuit. The parallel resistor needs to be this low to overcome the high shunt capacitance that can be found on the bus. A value of 100 pf or more is not uncommon. The resistor alone creates a load of 75 mW per circuit. An "X8" arrangement would be 560 mW. It is now clear that low voltage CMOS is not synonymous with low power.

By reducing the output swing and driving terminated transmission lines, improvements can be made. Several years ago, a specification called LVDS was approved by the EIA. The EIA–644 specification specifies a voltage swing and set of voltage levels. Interestingly, EIA–644 does not specify the technology. Typically implemented in submicron CMOS, the LVDS products on the market initially promised high performance and low power. Some of the more exuberant promoters have foretold the death knell of ECL rather prematurely.

LVDS, like CMOS, accomplishes its high performance by using small voltage swings and matched transmission lines. Some devices are available that use a scheme similar to what has been shown. The transmitter is a push–pull set of N–Channel transistors fed from a current source. The current source is limited to 3.5 mA and drives +/–350 mV into the receiver. The receiver is a differential amplifier with a threshold of about 100 mV. If the signal exceeds this threshold, the receiver switches. Since the predominant power is dissipated in the resistor, the power is simply the Vcc voltage multiplied by the current, or 13 mW/driver. Devices such as the one above can transmit signals perhaps as high as 200 MHz over tens of meters.

This signaling scheme can be integrated into ASICs/FPGAs and ASSPs. Compared to standard CMOS, there is quite a reduction of power. Signaling beyond 200 MHz is now available.

How does this compare to modern ECL? EIA–644 is useful for point–to–point communications, but is not very useful for point–to–multipoint communications. A new specification called Bus–LVDS (BLVDS) was created. It was thought that since the transmit/receive I/Os are high impedance, all that was necessary was to doubly terminate. Nearly all manufacturers of BLVDS parts recommend 27 Ω double termination. This requires about 12 mA to get the required voltage swing of +/–200 mV. It is then evident that the power per output section is about 40 mW. An octal device would require 320 mW (~ approximately 100 mA at 3.3 V) to drive the terminating resistors. The LVDS388 is an 8–bit, octal transceiver manufactured in submicron CMOS technology. The manufacturer specifies its operation to 200 MHz and provides the following chart at 3.3 V.

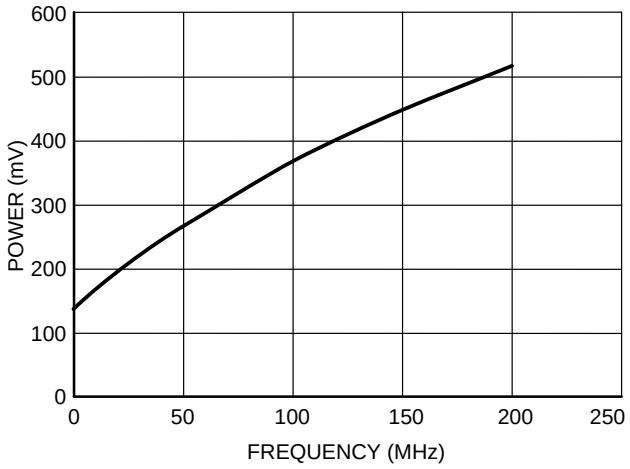

Figure 2. LVDS388

The driver must match the load for the signals to propagate cleanly. Strip lines and transmission lines typically have characteristic impedances of 50–100 Ω. Since the receiver is a comparator with 100 mV sensitivity, the transmitter needs to drive 250 mV or so to accommodate losses on the line. Indeed, the original notes[1] from National Semiconductor show a 3.5 mA driver and a 100 Ω termination. This implies that the power needed to be about 15 mW (from a 3.3 V supply) per driver. The 100 Ω case is valid for point–to–point applications. However, the BLVDS, or multipoint, case is quite different.

Cox, et al. [2], show that a multipoint system consists of a length of open transmission line with a large number of discrete capacitors spaced uniformly along the line. Since the driver is high impedance, a source termination is needed at the driver and a load termination is needed at the farthest end. This concept is the same whether the transmission line is balanced (differential) or single–ended. In this diagram, the 12 pf loads are the assumed loads of each receiver plus the capacitance of the bus and board. The loads are uniformly distributed along the length of the bus. Cox, et al., make a very reasonable assumption that the diagram can be represented by a uniformly distributed capacitance. They show that the characteristic impedance of a 50 Ω line reduces by a factor of 3. Since the receiver sensitivity remains the same, the receiver needs to see the same voltage at its input. With an open stripline impedance of 50 Ω, the new Zo is about 15Ω.

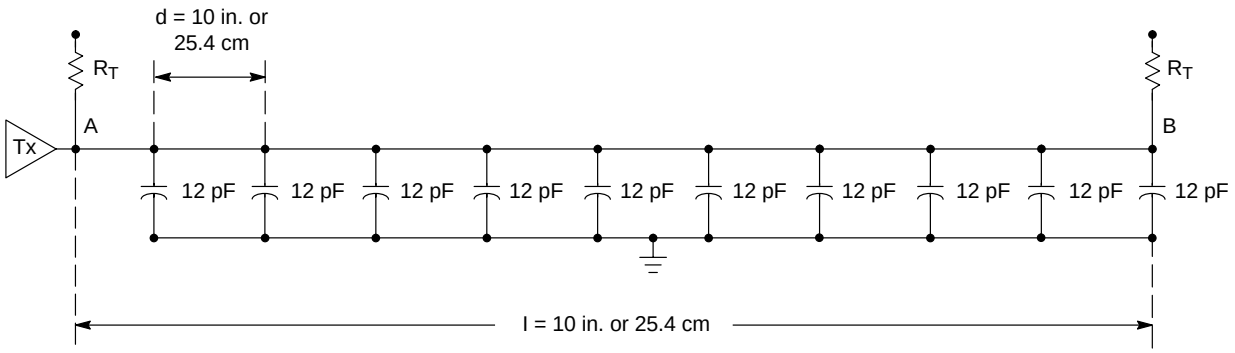

Figure 3.

It takes seven times the current to drive 15 W, compared to the nominal 100 Ω lines that were originally mentioned [2]. Each driver consumes 75 mW. A by–eight driver is, therefore, >500 mW, or 150 mA (at 3.3 V). The manufacturer's data sheet shows these values, as well.

A comparison of various devices from four manufacturers was performed. The devices were: MC100LVEP111 from ON Semiconductor, for ECL; 92CK16 (one of six clock buffers) and 92LV090A, a 9–channel bus transceiver from vendor "A," and LVDS388, an 8–bit bus transceiver from vendor "B" for BLVDS; and FCT3805, an 8–bit clock distribution device from vendor "C" for CMOS. Each specification comes from the original vendor's data sheet. The following table displays the results.

Table 1. Device Comparison

	100LVEP111	92LV090A	92CK16	LVDS388	FCT3805	Units
Part Type	Clock Distrib	Bus Trans	Clock Distrib	Line Recvr	Clock Distrib	
No. of Circuits	10	9	6	8	2 x 5	Outputs
No. of Pins	32	64	24	38	20	
Manufacturer	ON	Vendor "A"	Vendor "A"	Vendor "B"	Vendor "C"	
Technology	Bipolar	CMOS	CMOS	CMOS	CMOS	
Signaling Levels	ECL	BLVDS	BLVDS	BLVDS	LVTTL	
Inputs	Differential	Differential	Differential	Differential	Single–ended	
Signal Swing p to p	400	300	300	300	2200	mV
Power Supply	2.5, 3.3	3.3	3.3	3.3	3.3	Volts
Fmax	1500	50	125	200	100	MHz
Current Drain	100	170	100*	160 (Note 2.)	~100	mA
Power Disp	250 (Note 1.)	560	330	528	330	mW
Pin to Pin Skew	10	50	50	100	350 (Note 3.)	ps
Part to Part Skew	100	1600	2500	1000	500	ps
Prop Delay	400	2000	2800	2500	3500	ps

1. @ 2.5 Volts
2. 200 MHz, 3.3 Volts
3. 100 MHz, 30 pf

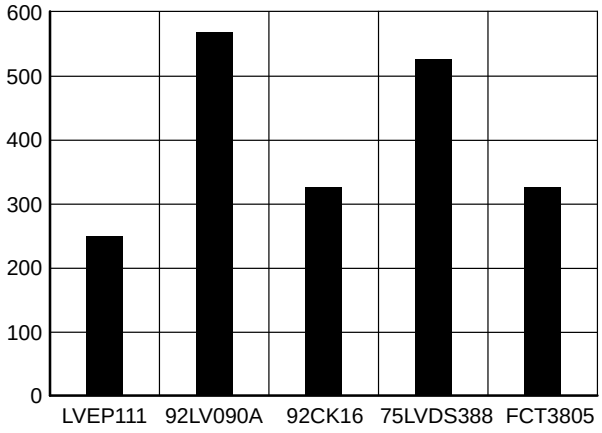

Figure 4. Power Consumption at Maximum Speed for Various Devices

Conclusion

BLVDS has high power consumption. The LVDS388 device runs at 200 MHz, but consumes over 500 mW. The doubly–terminated 27 Ω resistors cause much of the power consumption. This requires about 18 mA per driver to achieve a differential voltage high enough to meet the input requirements (~300 mV). With eight devices, this implies 144 mA, which is very close to the specifications shown on the data sheet. BLVDS has pin–for–pin skews that are two to four times worse than ECL. The part–to–part skew is five to ten times worse than ECL.

BLVDS has extended the range of CMOS operation from 100 MHz to as high as 250 MHz. The technology can be integrated onto ASICs and ASSPs, extending the range of these parts. It can be used to drive transmission lines 10 meters or more**.** Even for these applications, modern ECL drivers can drive low impedance cables, such as 75 Ω RG–6, beyond 1 GHz hundreds of meters. This compares to 250 MHz for LVDS.

ECL was always thought to be very high power. However, modern submicron geometry has brought ECL operating voltage down as low as 2.5 V and current drain down as low or lower than CMOS (either TTL or BLVDS). This is true, even though CMOS operates at one–fifth the speed. LVDS has borrowed some concepts, such as differential comparator input, from ECL and improved standard CMOS. However, the technology cannot compete in either speed or power skew with submicron ECL. Ohm's law still rules: if a device needs to drive a small resistor value, then large currents are needed. ECL is lower power in many applications and will operate at five to ten times the speed. Xilinx [3], the world's leading FPGA supplier, supports nearly all high–performance standards. The following is a quote from their Virtex™ product line description.

"LVPECL clocking becomes an essential requirement as FPGA system clock frequencies exceed 100 MHz. The Virtex–E device supports high–performance LVPECL clock inputs for global and local clocking with frequencies in excess of 300 MHz."

References:

1. LVDS Manual, National Semiconductor: Spring, 1997
2. "Basic Design Considerations for Backplanes", Application Note SZZA016, Texas Instruments, Cox, Ammar and Balsubramaniam: June, 1999
3. Xilinx website, description of I/O support: http://www.xilinx.com/products/virtex.htm

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