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Using PSPICE to Analyze Performance of Power MOSFETs in Step-Down, Switching Regulators Employing Synchronous Rectification

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APPLICATION NOTE

Prepared by: Rick Honda and Scott Deuty

INTRODUCTION

This paper will describe an easy method to analyze performance of various power MOSFETs in step down switching regulators using the PSPICE circuit analysis tool. A comparison will be made between circuit simulation results and the measured performance described in ON Semiconductor Application Note AN1520/D.

The utility of having a model which closely simulates switching performance is that different MOSFETs and diodes can be used in the model and comparisons can be made for proper performance vs. price, size, etc., prior to building breadboards. Actual hardware should always be used to verify performance, but a good simulation model gives the designer a means of trying various combinations of parts quickly to see how well they work in a particular circuit.

The ON Semiconductor website has SPICE, PSPICE, HSPICE, and Saber models available to download for numerous n−channel and p−channel MOSFETs along with several power rectifiers. Refer to Application Note AN1520/D which can be found at www.mot−sps.com/books/apnotes.

It should be noted that a full version of PSPICE is needed to run these simulations, the numerous demo versions do not support the complexity of the MOSFET models. A copy of the PSPICE circuit model listing is included for reference.

Circuit Description

The circuit described in AN1520/D is a 5 V to 3.3 V output buck regulator using synchronous rectifiers. The paper gives an overview on the operation of a buck regulator and the various waveforms through the power components. Also included in the application note are actual measurements of waveforms and power dissipations.

Figure 1 shows a block diagram of the circuit configuration. A schematic of the circuit is shown in Figure 2.

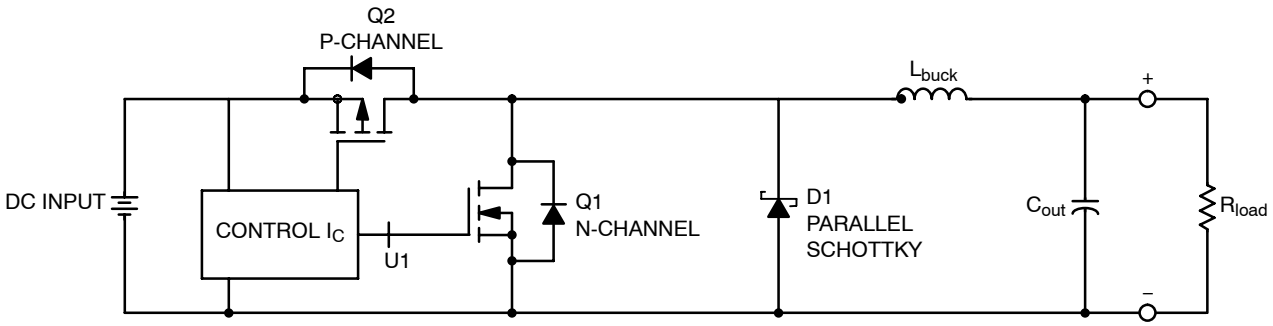

Figure 1. Typical Buck Regulator Employing a Synchronous Rectifier
(Source: ON Semiconductor Application Note AN1520/D)

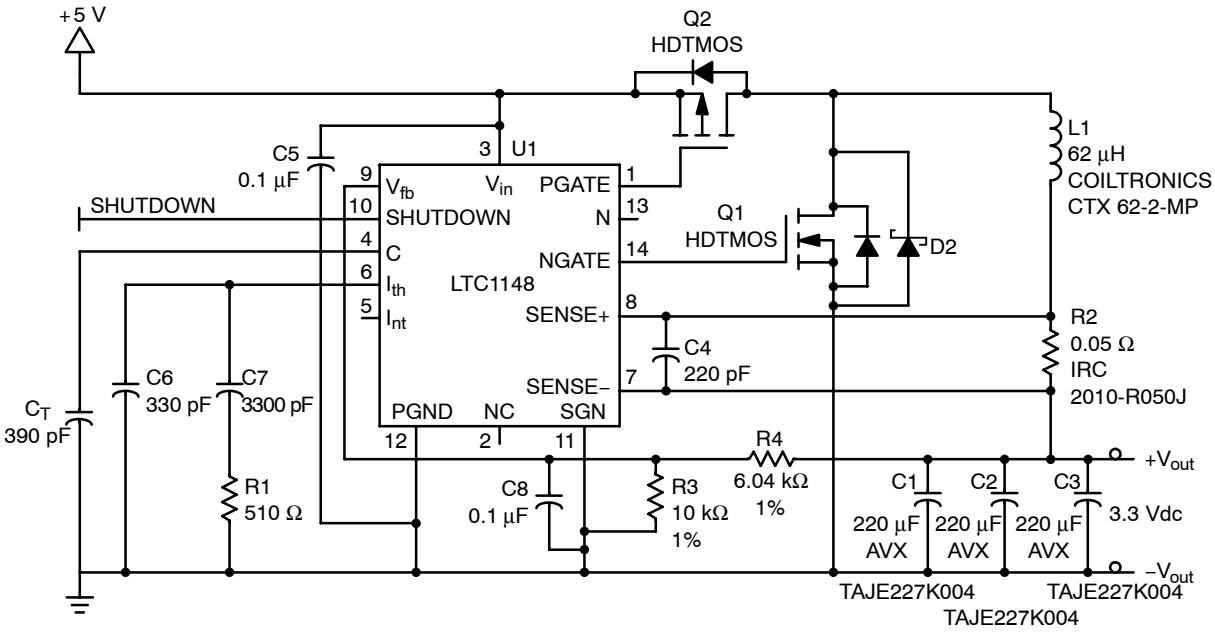

Figure 2. Physical Circuit Schematic of a 5 Vdc to 3.3 Vdc Buck Converter Employing a Synchronous Rectifier
(Source: ON Semiconductor Application Note AN1520)

The PSPICE model (Figure 3) follows the power stages of the circuit very closely. The model was set up to operate in an open loop configuration since the switching characteristics of the main switching transistor, synchronous rectifier, and flyback diode were of most interest. The duty cycle of the power switch ≈ Vout/Vin or 3.3 V/5 V = 66%. An L–C input filter was added for simulation purposes to smooth the input current to the regulator to facilitate measurements for efficiency calculations.

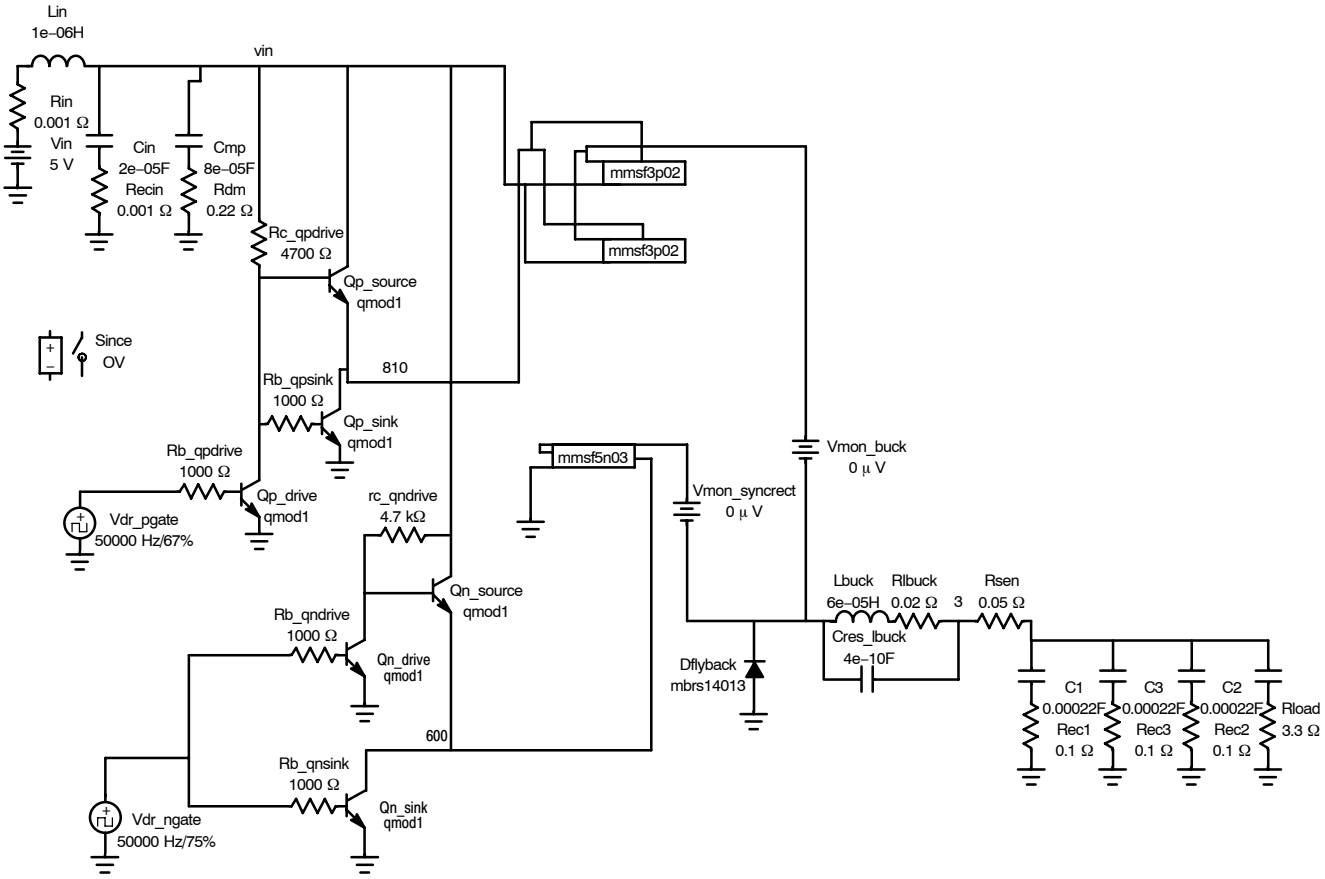

Figure 3. PSPICE Schematic of a 5 Vdc to 3.3 Vdc Buck Converter Employing a Synchronous Rectifier

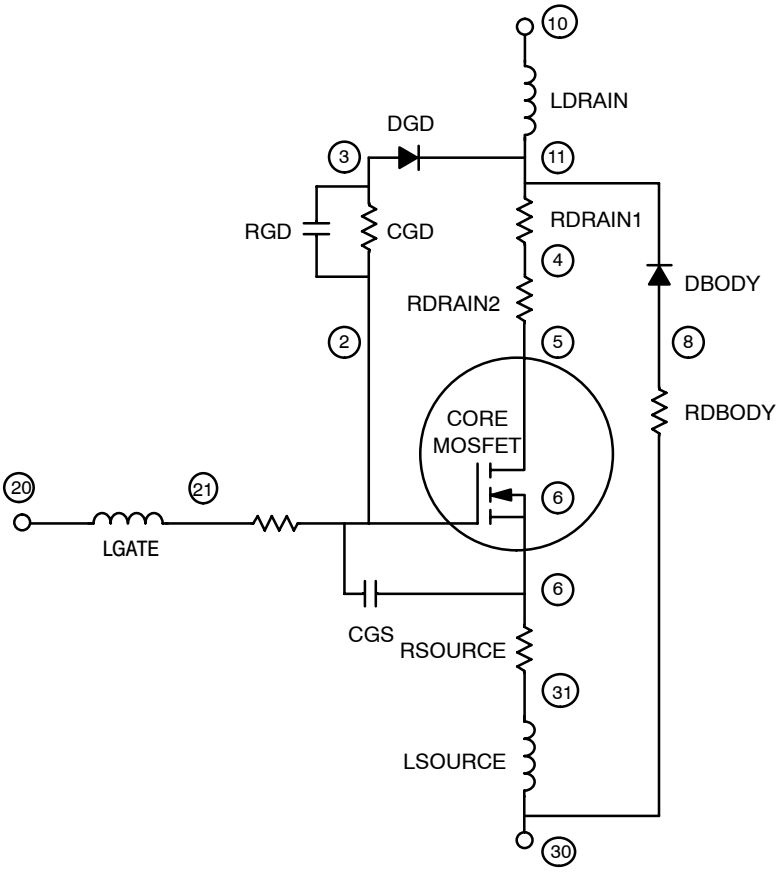

Figure 4. PSPICE Schematic of the N Channel MOSFET Model

A simple totem pole driver was included in the model to simulate the output driver stages of the LTC1148. The dead time of the switches was picked up from the measurements in the app. notes. For most pulse width modulators, the dead time can be calculated from the value of the timing capacitor.

Closed loop characteristics such as loop response and DC regulation can also be analyzed in PSPICE using the state−space models described in many other papers.

PSPICE Modeling Details

It is important to check any downloaded SPICE models for accuracy to the component data sheets. For diodes, a DC sweep of current through the diode vs. voltage drop should be run to verify that the model matches the data sheet. For MOSFETs, the switching time test set up can be copied from the data sheet and a simulation run to see if the switching time and on resistance matches the measured values. It is important to run any MOSFET models in a simple switching circuit before putting them into a more complex one. Some MOSFET models have convergence problems when running time domain analysis.

The model was run in the time domain for many cycles (800μS at a switching period of 20μS in 20nS steps). This was done to allow the transients to settle out. Options were set up in the transient analysis statement to bypass an initial DC operating point which PSPICE defaults to and instead use the specified initial conditions. The input voltage to the power switch was set to 5 V and the output voltage was set to 3.3 V. The initial condition on the output voltage puts an initial charge on the output capacitors. This greatly decreases the simulation time needed to reach a steady state condition since the capacitors do not have to charge up from 0 V. It is also important to use the ITL5 = 0 option which increases the number of iterations allowed during transient analysis. This is needed since many iterations are required during the switching transitions of the power devices.

Since the MOSFET models are set up as subcircuits containing numerous components, it can be difficult to see the total current into the drain or from the source. For modeling purposes, 0V voltage sources were placed in series with MOSFETs to monitor the current. In SPICE, voltage sources have zero resistance and thus do not affect circuit operation.

This model was also run using HSPICE (96.3.1) on a Unix workstation with simulation times on the order of 5 minutes. The results from PSPICE and HSPICE were very similar.

The particular version of PSPICE used did not have very good graphical capability to view the simulation results. The results from the simulations were loaded into excel, parsed, and graphed for inclusion into this document. More advanced versions of PSPICE have improved graphics, front end schematic entry, and various other useful features.

Excel was also used to calculate average values of input current and output voltage for efficiency calculations.

The components in the output L−C filter included extra components to account for non−ideal elements. The power inductor was composed of a series resistor with the inductor to account for winding resistance. A capacitor was placed in parallel with the series L−C to account for the inductor self resonance. The output capacitors included series resistors to simulate equivalent series resistance. These elements help the switching waveforms in the model to show non−ideal results such as current and voltage spikes.

The load current was set to 1A for the analyses showing the waveforms.

PSPICE Modeling Results

Figure 5 shows the current waveform of the main switching transistor as calculated by the circuit model. The various different MOSFETs used in application note AN1520 were all run in the model with similar results.

The MOSFETs used were:

P−Channel (Main power switch): MMSF3P02

N−Channel (Synchronous rectifier): MMS5N03HD, MMS3N03HD

Schottky Diode: MBR140

NOTE: No models were available for the MMDF2P02HD, MMDF2C02E, and MMDF2C02E MOSFETs also referenced in application note AN1520.

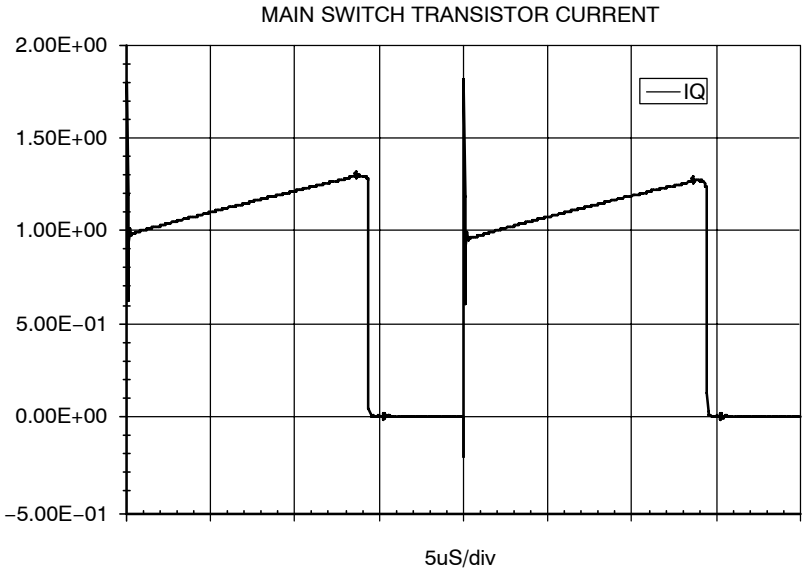

Figure 5. PSPICE Waveform of the Current through the Main, P Channel, Switching Transistors
(MMSF3P02 in Figure 2)

ANALYSIS OF THE WAVEFORMS

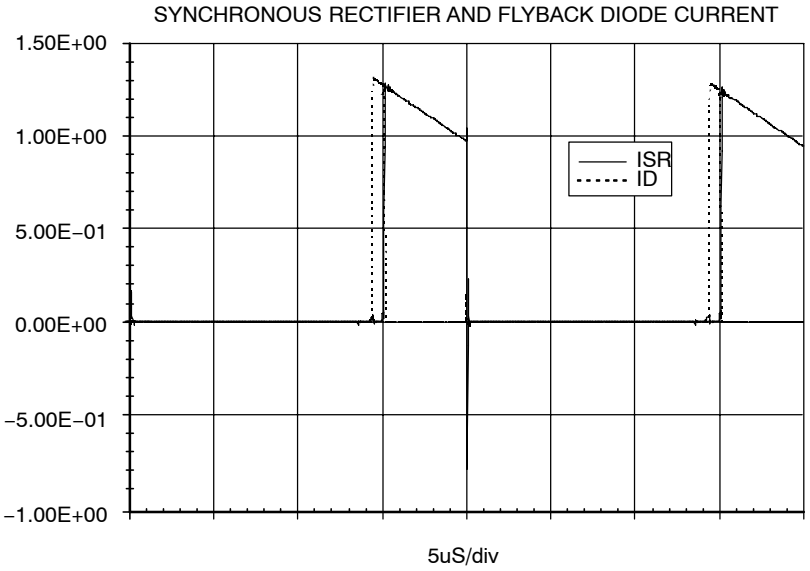

Figure 6. PSPICE Waveform of the Synchronous Rectifier Transistor and the Flyback Diode
(MMS5N03HD transistors and MBR140 Schottky diodes respectively in Figure 2)

Figure 7 shows an expanded view of the current in the synchronous rectifier leg and is very similar to Figure 8 that measured the performance of the physical circuit in the original application note.

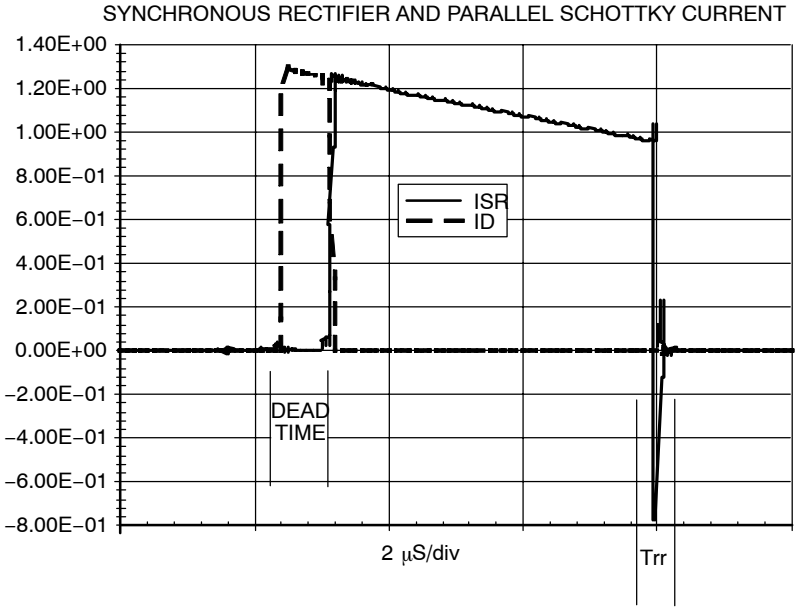

Figure 7. Shows an Expanded View of the SPICE Waveform
(Note the Similarity to the Physical Circuit)

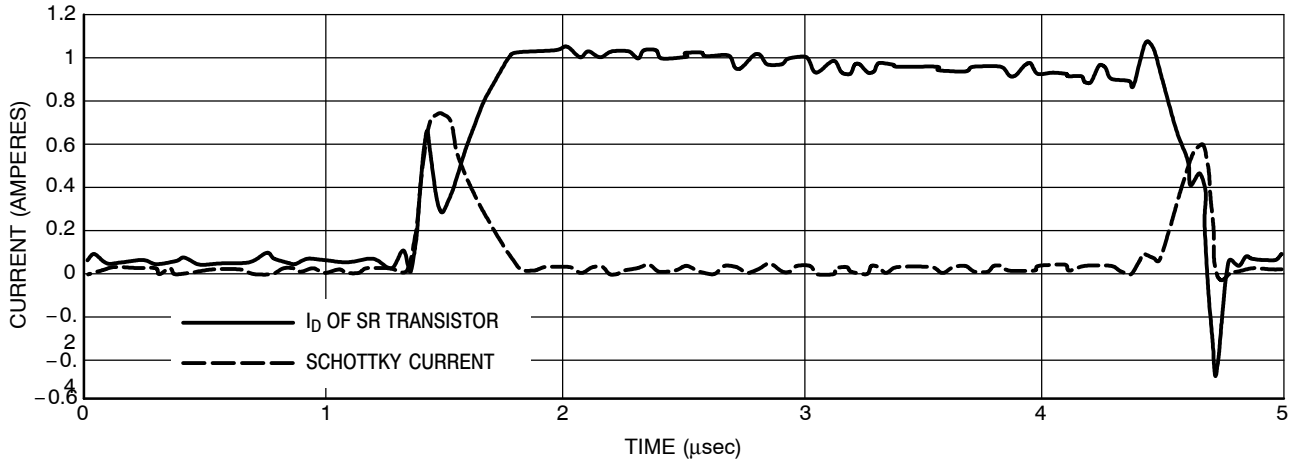

Figure 8. Waveforms of Synchronous Rectifier Transistor Drain Current and Parallel Schottky Current (I_{out} = 1 Amp) from the Physical Circuit

Figure 9 shows the expanded, leading edge of the current through the synchronous rectifier leg of the circuit. Notice that the Schottky takes the full current during the dead time and no body diode current is present. This is expected as the Schottky has a lower forward voltage drop. However, it was shown in the physical circuit of Figure 8 that the body diode does conduct current. Similarly, the trailing edge of this current in Figure 10 does not show any current in the Schottky. These findings indicate that the SPICE model is not matching the measurements from the physical circuit in terms of interaction of current interaction between synchronous rectifier transistor and parallel Schottky.

Expanded Leading Edge of Current in Sync Rec Transistor and Schottky

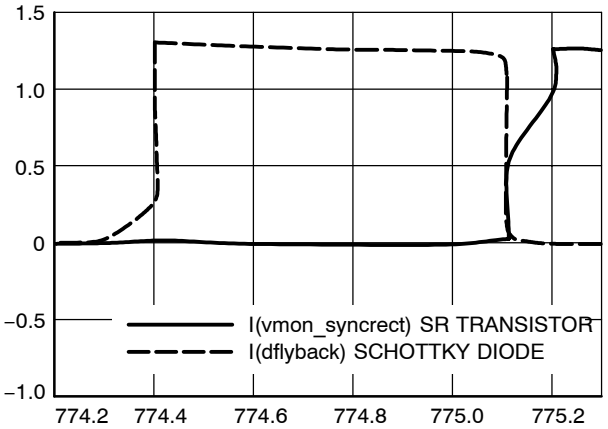

Figure 9. Expanded Leading Edge Current
(no inductance in Schottky path)

Expanded Trailing Edge of Current in Sync Rec Transistor and Schottky

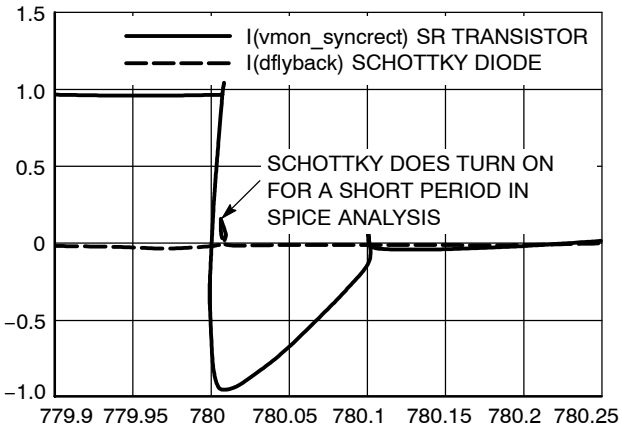

Figure 10. Expanded Trailing Edge Current
(no inductance in Schottky path)

A review of the SPICE model for the MBR140 diode reveals that no package inductance is listed. To account for the package and board inductance, an exaggerated value of 50 nH was inserted in series with the MBR140 Schottky and the model was run. The results of this test shown in Figure 11 show that the body diode now biases up for a short period on the leading edge of the current waveform.

Expanded Leading Edge Current in Sync Rec Transistor and Schottky with 50 nH of Inductance in Schottky Leg

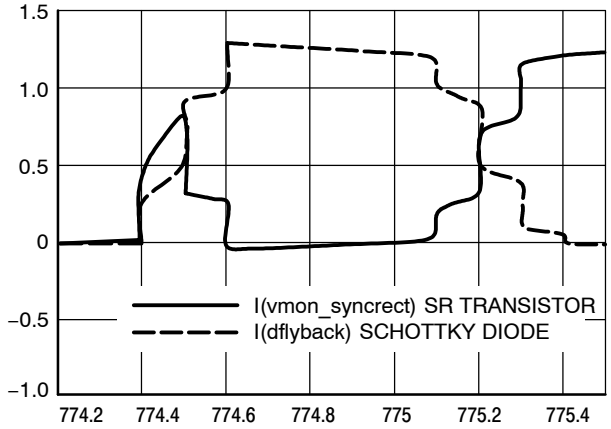

Figure 11. Expanded Leading Edge Current
(50 nH inductance in Schottky path)

Expanded Trailing Edge Current in Sync Rec Transistor and Schottky with 50 nH of Inductance in Schottky Leg

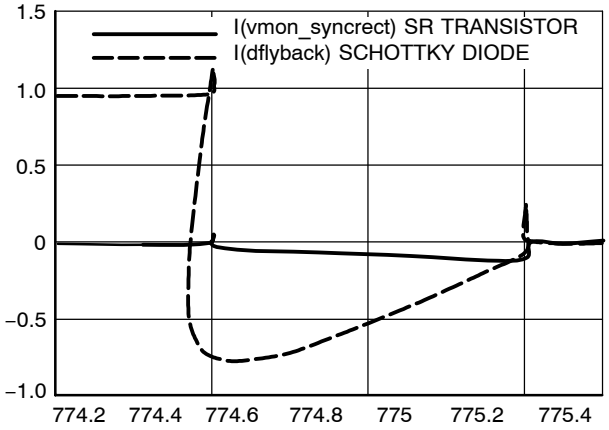

Figure 12. Expanded Trailing Edge Current
(50 nH inductance in Schottky path)

From the physical circuit and SPICE analysis it can be concluded that parasitics determine how the Schottky improves circuit performance. AN1520 argues the case for low RDS(on) and its effects on circuit efficiency. However, work remains to be done on the interaction between the body diode of the synchronous rectifier transistor and the parallel Schottky. The reverse recovery current of the body diode causes heating of the device and results in increased RDS(on). This in turn effects circuit performance. By understanding the interaction between the body diode and parallel Schottky, a more efficient design will result. The key is to design a system that uses the lower forward drop and faster recovery of the Schottky.

The power converter efficiency is simply Pout/Pin. This was calculated using Excel by finding the average value of the output voltage and the average value of the current through an input current sense resistor.

The efficiency is:

$$\text{Eff} = \frac{(\text{Vout}^2/\text{Rload})}{\left(\sqrt{\text{Pr in}/\text{Rin}}\right)(5\,\text{V})}$$

Newer versions of PSPICE may allow direct measurement of the currents which will greatly ease efficiency calculations. The version of HSPICE used had this feature.

Efficiency was calculated for two load conditions (0.5A and 1A) using two of the combinations listed in Figure 12 and Table 3 of the application note AN1520. The results are listed below:

P−Channel Part No.	N−Channel Part No.	Load Current	Efficiency
MMSF3P02HD	MMSF5N03HD	0.5 A	92.8%
MMSF3P02HD	MMSF5N03HD	1 A	86.4%
MMSF3P02HD	MMDF3N03HD	0.5 A	92.4%
MMSF3P02HD	MMDF3N03HD	1 A	86.0%

There is strong correlation of the efficiency values at 0.5A load, while the model indicates a slightly lower efficiency at a 1A load. The model does show the decrease in efficiency using the MMDF3N03HD MOSFET vs. the MMSF5N03HD MOSFET for the synchronous rectifier. The model can also be run without a synchronous rectifier and just the parallel Schottky diode with its corresponding decrease in efficiency. Thus, the designer can simulate performance effectively with modeling and optimize the system prior to performing any physical layout. This correlation is important to the choice of Schottky used.

Newer 5 to 3.3 V synchronous rectifier converters designed specifically for supplying Intel processors have resulted in a new synchronous rectifier controller, the MC33470 from ON Semiconductor, and a new HDTMOS III technology the MMSF3300 N Channel MOSFET. This design (Figure 13) is highly optimized to achieve high efficiency at 300 kHz (Figure 14). No SPICE models were available at time of print however they are needed to understand the board. It has proven very difficult to breakout paths to measure the current in the synchronous rectifier leg and modeling could be a solution for further performance optimization.

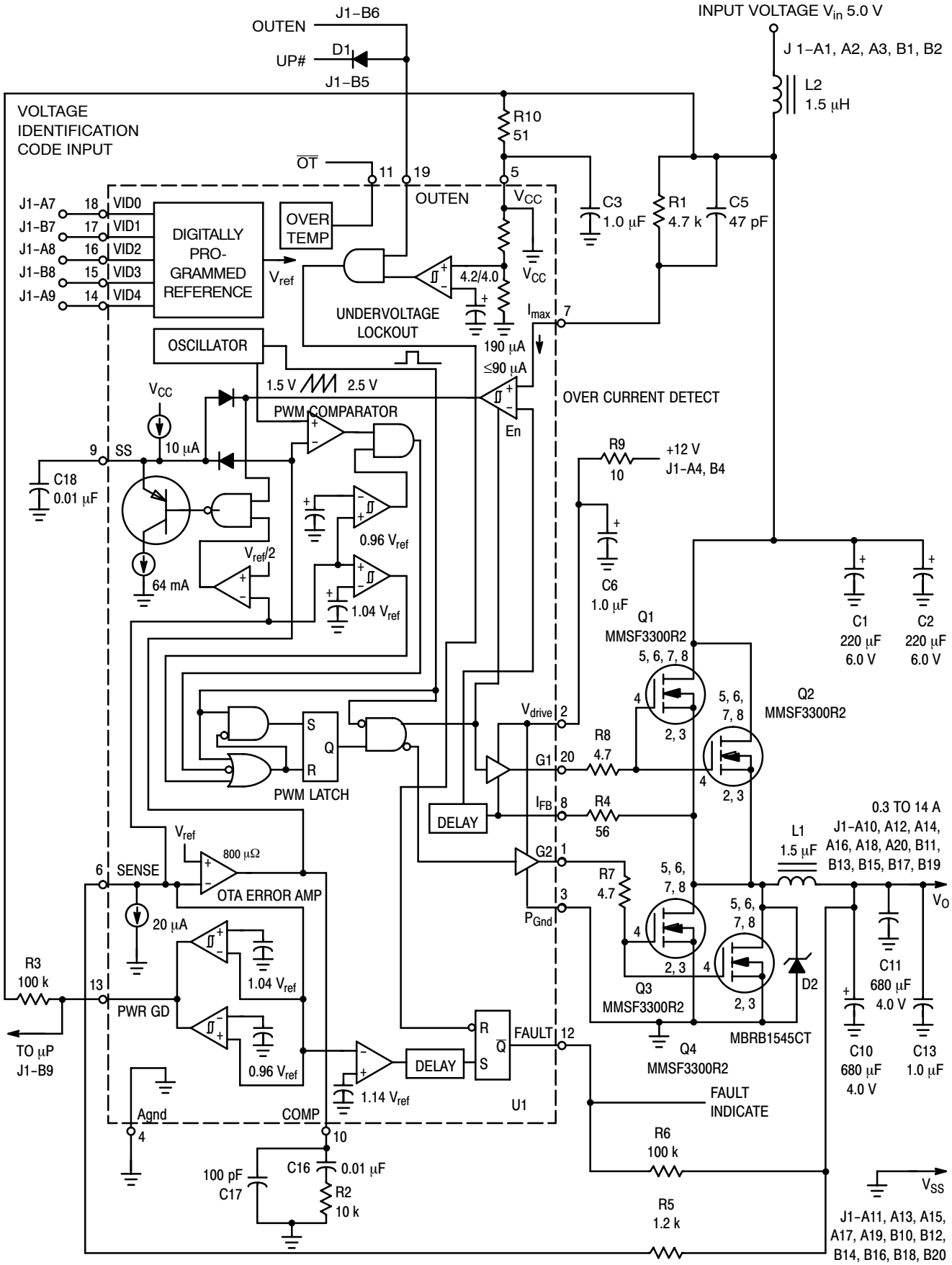

Figure 13. The MC33470 Based Pentium™ Design Schematic

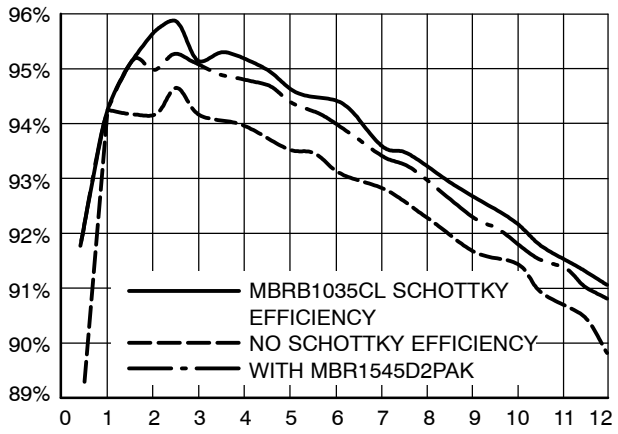

Figure 14. The MC33470 Based Pentium™ Design Efficiency

Summary

The PSPICE and HSPICE circuit simulators are powerful tools which enable the designer to assess the effects of different devices in a power converter circuit using time domain analysis. This paper showed that the waveforms of a measured breadboard can be modeled with strong correlation using a relatively simple circuit model along with available component models.

Some gaps in modeling were shown to exist. These gaps need to be overcome as more demand is placed on synchronous rectifier circuits to provide even lower logic level voltages reliably.

REFERENCES

"HDTMOS Power MOSFETs Excel in Synchronous Rectifier Applications,'' Deuty, ON Semiconductor Application Note AN1520/D.

PSPICE Program Listing:

```
******* 07/08/97 ******* PSpice 4.01 - Jan 1989 ******* 19:45:07 *******
 motorola 5v-3.3v buck regulator model
 ****   CIRCUIT DESCRIPTION
******************************************************************************
* Input Voltage
vin vin1 0 dc 5.0v
rin vin1 vin4 .001
*
* Input Filter (used to smooth out input current waveform)
lin vin4 vin 1uh
cin vin vin2 20uf
recin vin2 0 .001
cmp vin vin3 80uf
rdm vin3 0 .22
****************************************
* Flyback Diode model (Schottky diode)
.model mbrs140t3 d is= 4.41547e-06 rs= 0.103922 n= 1.03751 tt= 1e-12 cjo= 1.598e-10 vj= 0.4934
+ m= 0.4258 eg= 0.6 xti= 3.29768 fc= 0.5 bv= 48 ibv= 0.01 kf= 0 af= 1
****************************************
* Synchronous recitifer model (N-Channel MOSFET)
***** MICROSIM PSPICE(tm) SIMULATORS **********************
************************* INSTANTIATION ******************
.subckt mmsf5n03hdP 10 20 30
*
* 10 = Drain 20 = Gate 30 = Source
*
************************************************************
*
*------------------------ EXTERNAL PARASITICS --------------------------------
* PACKAGE INDUCTANCE
*
LDRAIN 10 11 7.5e-09
LGATE  20 21 4.5e-09
LSOURCE 30 31 4.5e-09
*
* RESISTANCES
*
RDRAIN1  4 11 RDRAIN 0.02556
RDRAIN2  4  5 RDRAIN 0.001
RSOURCE  31  6 RSOURCE 0.01518
RDBODY   8 30 RDBODY 0.03772
*
RGATE   21  2 5
*
*------------------------------------------------------------------------------
*
*---------------- CAPACITANCES AND BODY DIODE -----------------------------
*
DBODY    8 11 DBODY
DGD     3 11 DGD
CGDMAX   2  3 2.3e-09
RGDMAX   2  3 1e+08
CGS     2  6 1.182e-09
*
*------------------------------------------------------------------------------
*
*------------------------ CORE MOSFET -----------------------------------------
*
M1    5 2 6 6 MAIN
*
*------------------------------------------------------------------------------
*
.MODEL RDRAIN RES (TC1  = 0.01064 TC2  = -6.14682e-06)
*
.MODEL RSOURCE RES (TC1  = -0.009967 TC2  = 2.36438e-05)
*
.MODEL RDBODY RES (TC1  = 0.001953 TC2  = -6.62384e-06)
*
*
.MODEL MAIN NMOS ( LEVEL = 3 VTO = 2.359 KP = 22.07 GAMMA = 1.5 PHI = 0.6
+LAMBDA = 0.001 RD = 0 RS = 0 CBD= 0 CBS= 0 IS = 1e-14 PB = 0.8 CGSO = 0
+CGDO = 0 CGBO = 0 RSH = 0 CJ = 0 MJ= 0.5 CJSW= 0 MJSW = 0.33 JS= 1e-14
+TOX = 1e-07 NSUB = 1e+15 NSS = 0 NFS = 2e+11 TPG = 1 XJ = 0 LD = 0 UO = 600
+UCRIT = 0 UEXP = 0 UTRA = 0 VMAX = 0 NEFF = 1 KF= 0 AF = 1 FC = 0.5 DELTA = 0
+THETA = 0 ETA = 0 KAPPA = 0.2)
*
```

```
*---------------------------------------------------------------------------
*
.MODEL DGD D ( IS = 1e-15 RS = 0 N = 1000 TT = 0 CJO= 8.633e-10 VJ = 0.1 M = 0.487
+EG = 1.11 XTI = 3 KF = 0 AF = 1 FC = 0.5 BV = 10000 IBV = 0.001)
*
*---------------------------------------------------------------------------
*
.MODEL DBODY D ( IS = 1.668e-12 RS = 0 N= 1.018 TT = 5e-09 CJO = 1.2e-09 VJ = 0.5302
+M = 0.3689 EG = 1.11 XTI = 4 KF = 0 AF = 1 FC = 0.5 BV = 45.91 IBV = 0.00025)
.ENDS
*
********************************************************************
* Power Switch model (P-Channel MOSFET)
.subckt mmsf3p02hdP 10 20 30
*
* 10 = Drain 20 = Gate 30 = Source
*
********************************************************************
*
*------------------------ EXTERNAL PARASITICS -------------------------------
* PACKAGE INDUCTANCE
*
LDRAIN 10 11 7.5e-09
LGATE  20 21 4.5e-09
LSOURCE 30 31 4.5e-09
*
* RESISTANCES
*
RDRAIN1  4 11 RDRAIN 0.04938
RDRAIN2  4  5 RDRAIN 0.001
RSOURCE  31  6 RSOURCE 0.01649
RDBODY   8 30 RDBODY 0.166
*
RGATE   21  2 5
*
*---------------------------------------------------------------------------
*
*--------------- CAPACITANCES AND BODY DIODE -------------------------------
*
DBODY    11 8 DBODY
DGD     11 3 DGD
CGDMAX   2  3 4.5e-09
RGDMAX   2  3 1e+08
CGS     2  6 9e-10
*
*---------------------------------------------------------------------------
*
*----------------------- CORE MOSFET ---------------------------------------
*
M1    5 2 6 6 MAIN
*
*---------------------------------------------------------------------------
*
.MODEL RDRAIN RES ( TC1 = -0.003993 TC2 = 4.21478e-05)
*
.MODEL RSOURCE RES ( TC1 = -0.0055 TC2  = -1.73763e-05)
*
.MODEL RDBODY RES ( TC1 = 0.01634 TC2= 0.00019925)
*
.MODEL MAIN PMOS ( LEVEL = 3 VTO = -2.194 KP = 14.71 GAMMA = 0.8 PHI = 0.6
+LAMBDA = 0.001 RD = 0 RS= 0 CBD = 0 CBS= 0 IS= 1e-14 PB = 0.8 CGSO= 0
+CGDO = 0 CGBO = 0 RSH = 0 CJ = 0 MJ = 0.5 CJSW = 0 MJSW = 0.33 JS= 1e-14
+TOX = 1e-07 NSUB = 1e+15 NSS = 0 NFS = 2.5e+11 TPG = 1 XJ = 0 LD = 0 UO = 600
+UCRIT = 0 UEXP = 0 UTRA = 0 VMAX = 0 NEFF = 1 KF = 0 AF = 1 FC = 0.5 DELTA = 0
+THETA = 0 ETA = 5000 KAPPA = 0.2)
*
*---------------------------------------------------------------------------
*
.MODEL DGD D ( IS = 1e-15 RS = 0 N = 1000 TT = 0 CJO= 1.891e-09 VJ= 0.3367
+M = 0.4348 EG = 1.11 XTI = 3 KF = 0 AF = 1 FC = 0.5 BV = 10000 IBV   = 0.001)
*
*---------------------------------------------------------------------------
*
.MODEL DBODY D ( IS = 1.533e-12 RS = 0 N = 1.029 TT = 1e-12 CJO = 1.571e-09
+VJ = 0.7699 M = 0.3859 EG = 1.11 XTI = 4 KF = 0 AF = 1 FC = 0.5 BV = 28.91
+IBV   = 0.00025)
.ENDS
```

```
************************************************
*
* buck switch (p-channel), parallel transistors in same package
* subcircuit call
xbuck_sw1 11 810 vin mmsf3p02hdP
xbuck_sw2 11 810 vin mmsf3p02hdP
*
* 0V voltage source used to monitor currents through both switches
vmon_buck 11 1 dc 0v
************************************************
* synchronous rectifier (n-channel)
* subcircuit call
xsync_rect 10 600 0 mmsf5n03hdP
*
* 0V voltage source used to monitor current through synchronous rectifier
vmon_syncrect 10 1 dc 0v
*
************************************************
* Driver circuit for MOSFETs
* power switch gate driver
qp_source vin 100 810 qmod1
.model qmod1 npn bf=100
qp_sink 810 101 0 qmod1
qp_drive 100 102 0 qmod1
rc_qpdrive 100 vin 4.7k
rb_qpdrive 102 103 1k
rb_qpsink 101 103 1k
*
* drive to power switch: 50kHz, 67% duty cycle, and dead time
vdr_pgate 103 0 pulse(0v 5 0 .02us .02us 13.5us 20us)
*
*
* synchronous rectifier gate driver
qn_source vin 200 600 qmod1
qn_sink 600 201 0 qmod1
qn_drive 200 202 0 qmod1
rc_qndrive 200 vin 4.7k
rb_qndrive 202 203 1k
rb_qnsink 201 203 1k
*
* drive to synchcronous rectifier: 50kHz, 25% duty cycle, and dead time
vdr_ngate 203 0 pulse(0 5 0us .01us .01us 15.0us 20us)
* set vdr_ngate to 5v dc to operate without synchronous restifier
*
************************************************
* flyback diode
dflyback 0 1 mbrs140t3
*
************************************************
* output filter
*
* output inductor and parasitics
lbuck 1 2 60uh
rlbuck 2 3 .02
cres_lbuck 1 3 400pf
*
* current sense resistor
rsen 3 500 .05
*
* output capacitors and ESR
c1 500 4 220uf
rec1 4 0 .1
c2 500 5 220uf
rec2 5 0 .1
c3 500 6 220uf
rec3 6 0 .1
*
* load resistor
* node 500 is the output voltage
rload 500 0 3.3
*
```

```
*******************************************
* PSPICE option statements
* itl5=0 allows unlimited number of iterations at each point in transient analysis
.option nomod itl5=0
*
* probe statements allow the points to be viewed graphically
.probe i(vmon_buck)
*.probe v(600)
*.probe v(810)
.probe i(vmon_syncrect)
*.probe i(dflyback)
.probe v(500)
.probe i(rin)
*.probe v(103)
*.probe v(203)
*
* Transient analysis control statement:
* perform analysis out to 800us in 20ns steps, print out results starting at 760us
* use initial conditions, do not calculate initial DC operating point
.tran 20ns 800us 760us uic
*
* initial condition statements: sets output voltage to 3.3v and input to power switch to 5v
.ic v(500)=3.3 v(vin)=5
*
* print statements cause voltage, currents data points to be printed out
* .print tran v(1)
* .print tran i(lbuck)
 .print tran i(vmon_syncrect)
 .print tran i(vmon_buck)
 .print tran i(rin)
 .print tran i(dflyback)
.end
```

Notes

PUBLICATION ORDERING INFORMATION

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