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# AN-9736

# Design Guideline of AC-DC Converter Using FL6961 & FL6300A for 70W LED Lighting

## Summary

This application note describes a design strategy for a Power Factor Correction (PFC) circuit and higher-power conversion efficiency using FL6961 and FL6300A. Based on this design guideline and several functions of each controller for LED lighting applications, a design example with detailed parameters demonstrates the performance.

## Introduction

Figure 1 shows the typical application circuit, with the BCM PFC converter in the front end and the Quasi-resonant (QR) flyback converter in the back end. FL6961 and FL6300A achieve high efficiency with relatively low cost for 75~200W applications where BCM and QR operation with a single switch shows best performance. BCM boost PFC converter can achieve better efficiency with lower cost than Continuous Conduction Mode (CCM) boost PFC converter. These benefits result from the elimination of the reverse-recovery losses of the boost diode and zero-voltage switching (ZVS) or near-ZVS (also called valley switching) of boost switch. The QR flyback converter for the DC-DC conversion achieves higher efficiency than the conventional hard-switching converter with valley switching.

The FL6961 provides a controlled on-time to regulate the output DC voltage and achieves natural power factor correction. The maximum on-time of the switch is programmable to ensure safe operation during AC brownouts. The FL6300A ensures thepower system operates in quasi-resonant operation in wide range line voltage and reduces switching loss to minimize switching voltage in drain of the power MOSFET. To minimize standby power consumption and improve light-load efficiency, a proprietary Green-Mode provides off-time modulation to decrease switching frequency and perform extended valley voltage switching to keep to a minimum switching voltage.
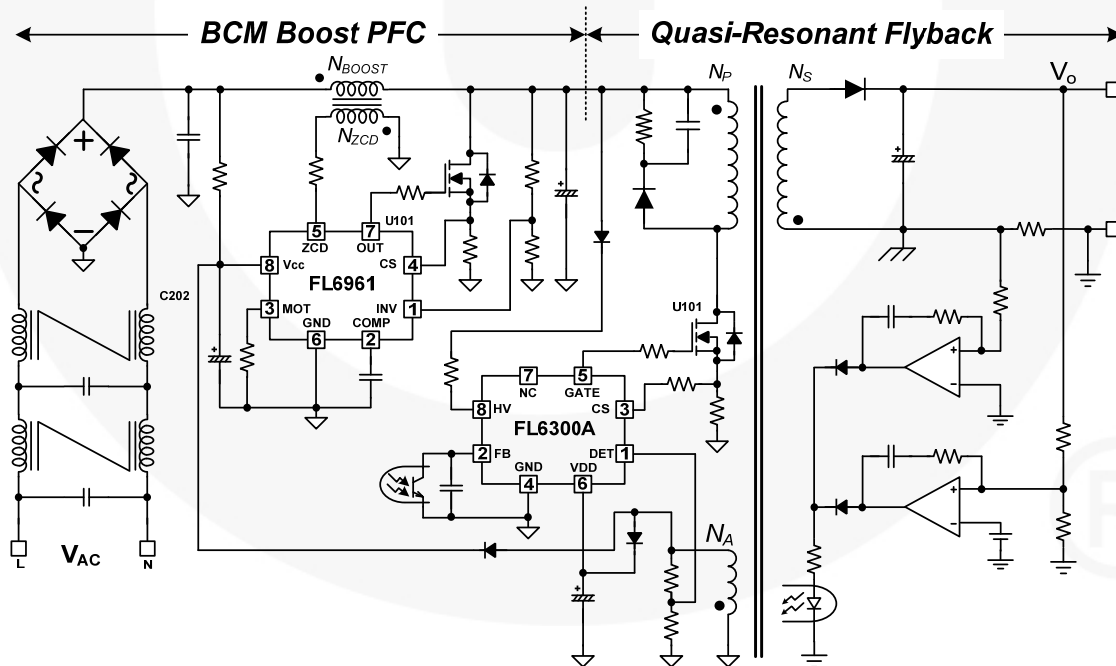


**Figure 1. Typical Application Circuit**

# 1. Basin Operation of BCM Boost PFC Converter

The typical boost converter and its operational waveforms are shown in Figure 2, Figure 3, and Figure 4.
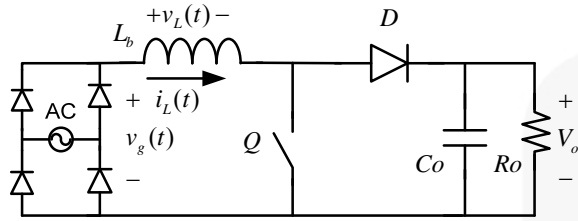


**Figure 2. Boost Converter**



**(a) Switch Q is ON**        **(b) Switch Q is OFF**
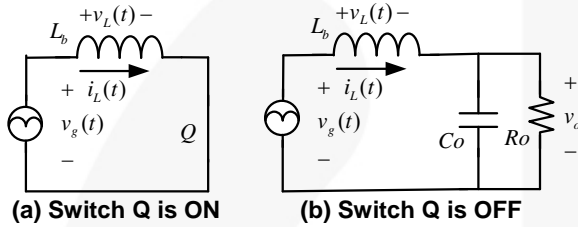
**Figure 3. Switching Sequences of the Boost Converter**
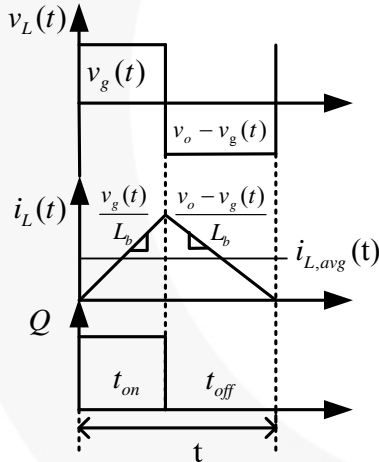


**Figure 4. One-Cycle Waveform of the Boost Converter**

## 1.1. Operation Principle

When Q turns on, the rectifier diode D is reverse-biased and output capacitor $C_O$ supplies load current. The rectified AC line input voltage $V_g(t)$ is applied to the inductor $L_b$ so that inductor current $I_L$ ramps up linearly and can be expressed as:

$$I_L(t_{on}) = \frac{V_g(t)}{L_b} \qquad (1)$$

When Q turns off, the voltage $V_O - V_g(t)$ is applied to inductor $L_b$ and the polarity on the inductor Lb is reversed. The diode D is forward-biased in this stage. The energy stored in the inductor $L_b$ is delivered to supply load current

and output capacitor $C_O$. The inductor current $I_L$ can be expressed as:

$$I_L(t_{off}) = \frac{V_o - V_g(t)}{L_b} \qquad (2)$$

The on-time of the power MOSFET Q is determined by the output of the error amplifier that monitors the pre-regulator output voltage. With a low-bandwidth error amplifier, the feedback signal is almost constant during a half AC cycle, resulting a fixed on-time of the power MOSFET at a specific AC voltage and some certain output power level. Therefore, the peak inductor current $I_{Lpk}$ automatically follows the input voltage $V_{g(t)}$, achieving a natural power factor correction mechanism. Figure 5 shows the typical inductor current waveform during a half AC cycle.
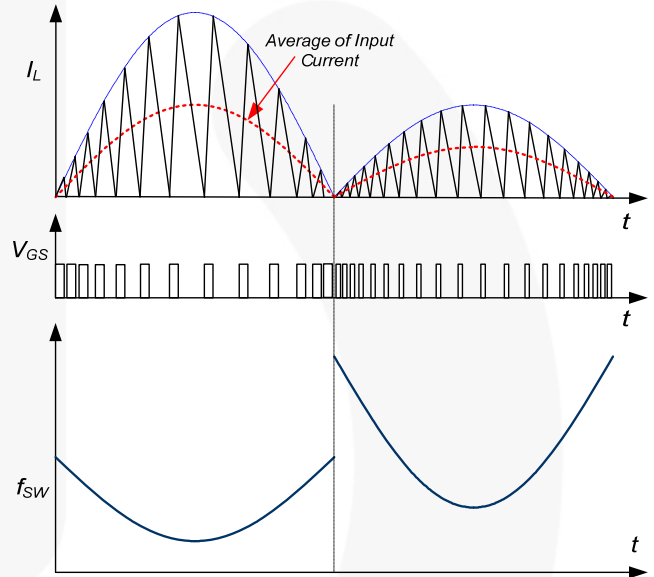


**Figure 5. Controlled On-Time Inductor Current Waveform**

Referring to Figure 4, considering one switching period the average inductor current, $I_{L,ave}(t)$ can be calculated by the average area of triangle waveform of inductor current:

$$I_{L,avg}(t) = \left[ V_g(t) + \frac{V_g(t)^2}{V_o - V_g(t)} \right] \times \frac{\left[ \frac{t_{on}}{T_s} \right]^2}{2 \cdot L_b} \cdot T_s \qquad (3)$$

# 2. Operation Principle of Quasi-Resonant Flyback Converter

QR flyback converter topology can be derived from a conventional square wave, Pulse-Width Modulated (PWM), flyback converter without additional components. Figure 6 and Figure 7 show the simplified circuit diagram of a quasi-resonant flyback converter and its typical waveforms.
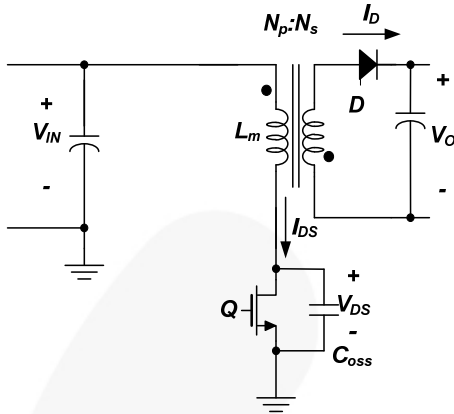
**Figure 6.  Schematic of QR Flyback Converter**

## 2.1.  Operation Principle

- During the MOSFET on time ($t_{ON}$), input voltage ($V_{IN}$) is applied across the primary-side inductor ($L_m$). MOSFET current ($I_{DS}$) increases linearly from zero to the peak value ($I_{pk}$). During this time, the energy is drawn from the input and stored in the inductor.

- When the MOSFET is turned off, the energy stored in the inductor forces the rectifier diode (D) to turn on. During the diode ON time ($t_D$), the output voltage (Vo) is applied across the secondary-side inductor and the diode current ($I_D$) decreases linearly from the peak value to zero. At the end of $t_D$, all the energy stored in the inductor has been delivered to the output. During this period, the output voltage is reflected to the primary side as $V_O \times N_P/N_S$. Then, the sum of input voltage ($V_{IN}$) and the reflected output voltage ($Vo \times N_P/N_S$) is imposed across the MOSFET.

- When the diode current reaches zero, the drain-to-source voltage ($V_{DS}$) begins to oscillate by the resonance between the primary-side inductor ($L_m$) and the MOSFET output capacitor ($C_{OSS}$) with an amplitude of $V_O \times N_P/N_S$ on the offset of $V_{IN}$, as depicted in Figure 7. Quasi-resonant switching is achieved by turning on the MOSFET when $V_{DS}$ reaches its minimum value. This reduces the MOSFET turn-on switching loss caused by the capacitance loading between the drain and source of the MOSFET.
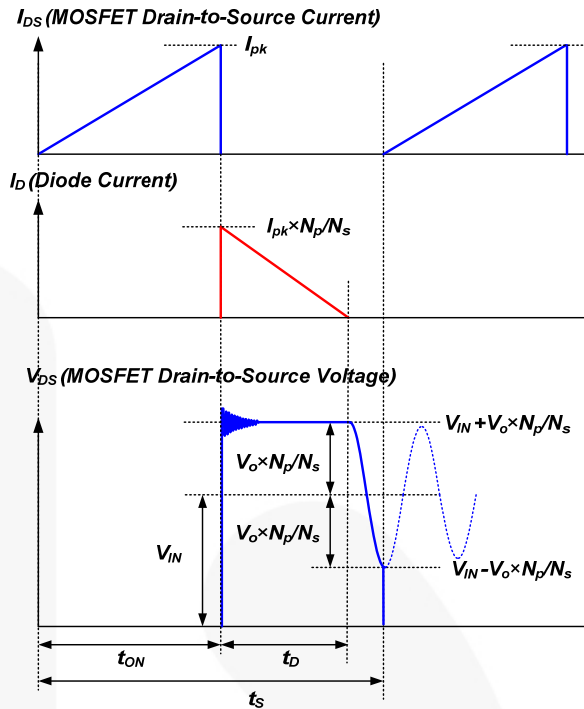
**Figure 7.  Typical Waveforms of QR Flyback Converter**

# 3. Design Considerations

This design procedure uses the schematic in Figure 1 as a reference. A 70W PFC application with universal input range is selected as a design example. The design specifications are:

- Line Voltage Range: 90~277$V_{AC}$ (60Hz)
- Output of DC-DC Converter: 24V/2.9A (70W)
- PFC Output Voltage for Line Voltage: 420V
- Minimum PFC Switching Frequency: > 58kHz
- Minimum QR flyback Switching Frequency: > 50kHz
- Overall Efficiency: 90% (PFC: 95%, QR: 95%)

## 3.1.  PFC Section

### 3.1.1. Boost Inductor Design

The boost inductor value is determined by the output power and the minimum switching frequency. The voltage-second balance equation for the inductor is:

$$V_{IN}(t) \cdot t_{ON} = (V_{O.PFC} - V_{IN}(t)) \cdot t_{OFF} \tag{4}$$

$$f_{SW,\ MIN} = \frac{1}{t_{ON} + t_{OFF}} = \frac{1}{t_{ON}} \cdot \frac{V_{O.PFC} - \sqrt{2}V_{LINE}}{V_{O.PFC}} \tag{5}$$

where $V_{IN}(t)$ is the rectified line voltage.
$V_{LINE}$ is RMS line voltage;
$t_{ON}$ is the MOSFET conduction time; and
$V_{O.PFC}$ is the PFC output voltage.

The MOSFET conduction time with a given line voltage at a nominal output power is given as:

$$t_{ON} = \frac{2 \cdot P_{OUT} \cdot L}{\eta \cdot V_{LINE}{}^2} \tag{6}$$

where:

$\eta$ is the overall efficiency;

L is the boost inductance; and

$P_{OUT}$ is the nominal output power.

Using Equation 5, the minimum switching frequency of Equation 6 can be expressed as:

$$f_{SW.\ MIN} = \frac{\eta \cdot V_{LINE}{}^2}{2 \cdot P_{OUT} \cdot L} \cdot \frac{V_{O.PFC} - \sqrt{2}V_{LINE}}{V_{O.PFC}} \tag{7}$$

As shown in Figure 5, considering one AC line voltage cycle, the minimum switching frequency occurs at peak of the AC line voltage. Also, the minimum switching frequency may occur in AC maximum or minimum input voltage, depending on the output voltage. Therefore, calculate both the maximum and the minimum input voltage and choose the lower inductance value. Once the output voltage and minimum switching frequency are set, the inductor value is given as:

$$L = \frac{\eta \cdot V_{LINE\ MAX}{}^2}{2 \cdot P_{OUT} \cdot f_{SW.\ MIN}} \cdot \frac{V_{O.PFC} - \sqrt{2}V_{LINE\ MAX}}{V_{O.PFC}} \tag{8}$$

where $V_{LINE,MAX}$ is the maximum line voltage.

As the minimum frequency decreases, the switching loss is reduced, while the inductor size and line filter size increase. Thus, the minimum switching frequency should be determined by the trade-off between efficiency and the size of magnetic components. The minimum switching frequency must be above 20kHz to prevent audible noise.

Once the inductance value is decided, the maximum peak inductor current at the nominal output power is obtained at low-line condition as:

$$I_{L.PK} = \frac{2\sqrt{2} \cdot P_{OUT}}{\eta \cdot V_{LINE.MIN}} \tag{9}$$

where $V_{LINE,MIN}$ is the minimum line voltage.

Since the maximum on time is internally limited at 25μs, it should be smaller than 25μs, as calculated by:

$$t_{ON}{}^{MAX} = \frac{2 \cdot P_{OUT} \cdot L}{\eta \cdot V_{LINE\ MIN}{}^2} < 20\mu s \tag{10}$$

The number of turns of the boost inductor should be determined considering the core saturation. The minimum number is given as:

$$N_{BOOST} \geq \frac{I_{L.PK} \cdot L}{A_e \cdot \Delta B} \tag{11}$$

where is Ae is the cross-sectional area of core and $\Delta B$ is the maximum flux swing of the core in Tesla. $\Delta B$ should be set below the saturation flux density.

(**Design Example**) Since the output voltage is 420V for line voltage, the minimum frequency occurs at high-line ($277V_{AC}$) and full-load condition. Assuming the overall efficiency is 90% and selecting the minimum frequency as 58kHz, the inductor value is obtained as:

$$L = \frac{\eta \cdot V_{LINE\ MAX}{}^2}{2 \cdot P_{OUT} \cdot f_{SW.\ MIN}} \cdot \frac{V_{O.PFC} - \sqrt{2}V_{LINE\ MAX}}{V_{O.PFC}}$$

$$\frac{0.9 \cdot 277^2}{2 \cdot 70 \cdot 58 \times 10^3} \cdot \frac{420 - \sqrt{2 \cdot 277}}{420} = 570\mu H$$

The maximum peak inductor current at nominal output power is calculated as:

$$I_{L.PK} = \frac{2\sqrt{2} \cdot P_{OUT}}{\eta \cdot V_{LINE.MIN}} = \frac{2\sqrt{2} \cdot 70}{0.9 \times 90} = 2.44\ A$$

$$t_{ON}{}^{MAX} = \frac{2 \cdot P_{OUT} \cdot L}{\eta \cdot V_{LINE\ MIN}{}^2} = \frac{2 \cdot 70 \cdot 570 \times 10^{-6}}{0.9 \times 90^2}$$

$$= 10.9\mu s < 20\mu s$$

Assuming RM10 core (PC40, $A_e$=85mm$^2$) is used and setting $\Delta B$ as 0.25T, the primary winding should be:

$$N_{BOOST} \geq \frac{I_{L.PK} \cdot L}{A_e \cdot \Delta B} = \frac{2.44 \cdot 570 \times 10^{-6}}{85 \times 10^{-6} \times 0.25} = 65.8\ turns$$

Thus, the number of turns ($N_{BOOST}$) of boost inductor is determined as 65.

### 3.1.2. Auxiliary Winding Design

Figure 9 shows the internal block for Zero-Current Detection (ZCD) for the PFC. FL6961 indirectly detects the inductor zero-current instant using an auxiliary winding of the boost inductor. The auxiliary winding should be designed such that the voltage of the ZCD pin rises above 2.1V when the boost switch is turned off to trigger internal comparator as:

$$\frac{N_{ZCD}}{N_{BOOST}}(V_{O.PFC} - \sqrt{2}V_{LINE.MAX}) > 2.1V \tag{12}$$

The ZCD pin has upper voltage clamping and lower voltage clamping at 10V and 0.3V, respectively. When the ZCD pin voltage is clamped at 0.3V, the maximum sourcing current is 1.5mA and, therefore, the resistor $R_{ZCD}$ should be properly designed to limit the current of the ZCD pin below 1.5mA in the worst case as:

$$R_{ZCD} > \frac{V_{IN}}{1.5mA} \cdot \frac{N_{AUX}}{N_{BOOST}} = \frac{\sqrt{2}V_{LINE.MAX}}{1.5mA} \cdot \frac{N_{AUX}}{N_{BOOST}} \tag{13}$$
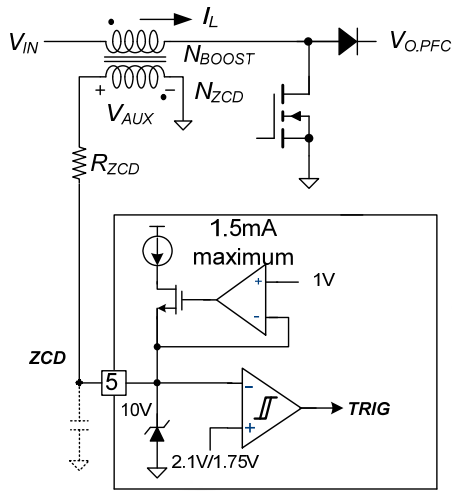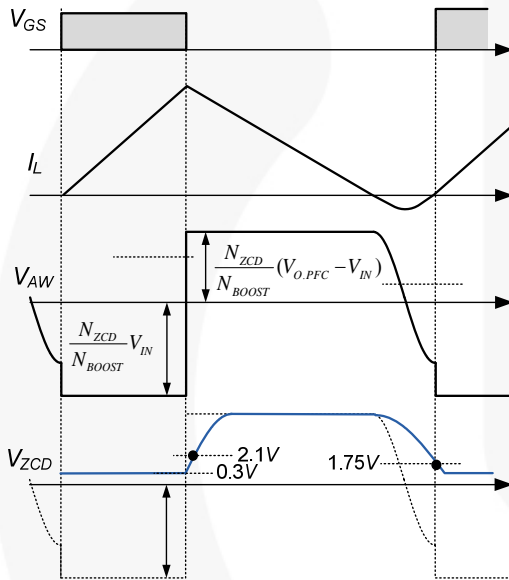
**Figure 8.  Internal Block for ZCD**



**Figure 9.  ZCD Waveforms**

(**Design Example**) The number of turns for the auxiliary ZCD winding is obtained as:

$$N_{ZCD} > \frac{2.1 N_{BOOST}}{(V_{O.PFC} - \sqrt{2}V_{LINE.MAX})} = 4.83 \text{ turn}$$

With a margin, $N_{AUX}$ is determined as 6 turns.

$R_{ZCD}$ is selected from:

$$R_{ZCD} > \frac{\sqrt{2}V_{LINE.MAX}}{1.5mA} \cdot \frac{N_{AUX}}{N_{BOOST}} = \frac{\sqrt{2} \cdot 277}{1.5 \times 10^{-3}} \cdot \frac{6}{65} = 24 k\Omega$$

as $30 k\Omega$.

### 3.1.3. Current-Sensing Resistor for PFC

FL6961 has pulse-by-pulse current limit function. It is typical to set the pulse-by-current limit level at 20~30% higher than the maximum inductor current:

$$R_{CS1} = \frac{0.82}{I_{L.PK}(1 + K_{MARGIN})} \tag{14}$$

where $K_{MARGIN}$ is the margin factor and 0.85V is the pulse-by-pulse current limit threshold.

(**Design Example**) Choosing the margin factor as 35%, the sensing resistor is selected as:

$$R_{CS1} = \frac{0.85}{I_{L.PK}(1 + K_{MARGIN})} = \frac{0.82}{2.44(1 + 0.35)} = 0.25\Omega$$

### 3.1.4. Output Capacitor Selection

For a given minimum PFC output voltage during the hold-up time, the PFC output capacitor is obtained as:

$$C_{O.PFC} > \frac{2P_{OUT} \cdot t_{HOLD}}{V_{O.PFC}{}^2 - V_{O.PFC.HLD}{}^2} \tag{15}$$

where:
$P_{OUT}$ is total nominal output power;
$t_{HOLD}$ is the required holdup time; and
$V_{O.PFC,HLD}$ is the allowable minimum output voltage during the hold-up time.

For PFC output capacitor, it is typical to use 0.5~1µF per 1W output power for 420V PFC output. Meanwhile, it is reasonable to use about 1µF per 1W output power for variable output PFC due to the larger voltage drop during the hold-up time than 420V output.

(**Design Example**) Assuming the minimum allowable PFC output voltage during the hold-up time is 160V, the capacitor should be:

$$C_{O.PFC} > \frac{2P_{OUT} \cdot t_{HOLD}}{V_{O.PFC}{}^2 - V_{O.PFC.HLD}{}^2} = \frac{2 \cdot 80 \cdot 20 \times 10^{-3}}{420^2 - 350^2}$$

$$= 60\mu F$$

A 68µF capacitor is selected for the output capacitor.

### 3.1.5. Design Compensation Network

The feedback loop bandwidth must be lower than 20Hz for the PFC application. If the bandwidth is higher than 20Hz, the control loop may try to reduce the 120Hz ripple of the output voltage and the line current is distorted, decreasing power factor. A capacitor is connected between COMP and GND to attenuate the line frequency ripple voltage by 40dB. If a capacitor is connected between the output of the error amplifier and the GND, the error amplifier works as an integrator and the error amplifier compensation capacitor can be calculated by:

$$C_{COMP} > \frac{100 \cdot g_M}{2\pi \cdot 2f_{LINE}} \cdot \frac{25}{V_{O.PFC}} \tag{16}$$

To improve the power factor, $C_{COMP}$ must be higher than the calculated value. However, if the value is too high, the output voltage control loop may become slow.

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**(Design Example)**

$$C_{COMP} > \frac{100 \cdot g_M}{2\pi \cdot 2f_{LINE}} \cdot \frac{2.5}{V_{O.PFC}}$$

$$= \frac{100 \cdot 125 \times 10^{-6}}{2\pi \cdot 2 \cdot 60} \cdot \frac{2.5}{420} = 100nF.$$

470nF is selected for better power factor.

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## 3.2.  DC-DC Section

### 3.2.1. Determine the Reflected Output Voltage ($V_{RO}$)

Figure 10 shows the typical operation waveforms of a quasi-resonant flyback converter. When the MOSFET is turned off, the input voltage (PFC output voltage), together with the output voltage reflected to the primary ($V_{RO}$), is imposed on the MOSFET. When the MOSFET is turned on, the sum of input voltage reflected to the secondary side and the output voltage is applied across the diode. Thus, the maximum nominal voltage across the MOSFET ($V_{DS.nom}$) and diode are given as:

$$V_{DS}{}^{nom} = V_{O.PFC} + n(V_O + V_F) = V_{O.PFC} + V_{RO} \quad (17)$$

where:

$$n = \frac{V_{RO}}{V_O + V_F} \quad (18)$$

$$V_D{}^{nom} = V_O + \frac{V_{O.PFC}}{n} = V_O + \frac{V_{O.PFC}}{V_{RO}}(V_O + V_F) \quad (19)$$

By increasing $V_{RO}$ (i.e. the turns ratio, *n*), the capacitive switching loss and conduction loss of the MOSFET are reduced. This also reduces the voltage stress of the secondary-side rectifier diode. However, this increases the voltage stress on the MOSFET. Therefore, $V_{RO}$ should be determined by a trade-off between the voltage stresses of the MOSFET and diode. It is typical to set $V_{RO}$ such that $V_{DS.nom}$ and $V_{D.nom}$ are 75~85% of their voltage ratings.
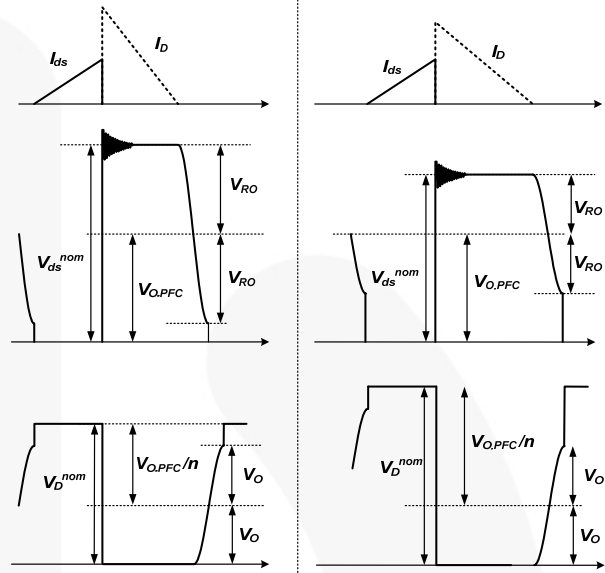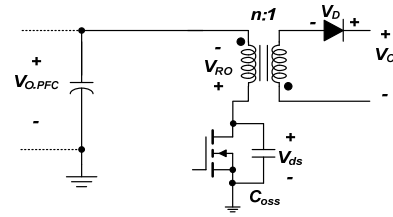


**Figure 10. Typical Waveforms of QR Flyback Converter**

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**(Design Example)** Assuming 650V MOSFET and 150V Diode are used for primary side and secondary side, respectively, with 18% voltage margin:

$$0.82 \cdot 650V > V_{DS}{}^{nom} = V_{O.PFC} + V_{RO}$$

$$\therefore V_{RO} < 0.82 \cdot 650 - V_{O.PFC} = 133V$$

$$0.82 \cdot 150 > V_{DS}{}^{nom} = V_O + \frac{V_{O.PFC}}{V_{RO}}(V_O + V_F)$$

$$\therefore V_{RO} > V_{DS}{}^{nom} = \frac{V_{O.PFC}}{0.82 \cdot 150 - V_O}(V_O + V_F) = 106V$$

$V_{RO}$ is determined as 130V.

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### 3.2.2. Transformer Design

Figure 11 shows the typical switching timing of a quasi-resonant converter. The sum of MOSFET conduction time ($t_{ON}$), diode conduction time ($t_D$), and drain voltage falling time ($t_F$) is the switching period ($t_S$). To determine the primary-side inductance ($L_m$), the following parameters should be determined first.

#### Minimum Switching Frequency ($f_{S.QRmin}$)

The minimum switching frequency occurs at the minimum input voltage and full-load condition, which should be higher than 20kHz to avoid audible noise. By increasing $f_{S.QRmin}$, the transformer size can be reduced. However, this results in increased switching losses. Determine $f_{S.QRmin}$ by a trade-off between switching losses and transformer size. Typically $f_{S.QRmin}$ is set to around 50kHz.

## Falling Time of the MOSFET Drain Voltage (t$_F$)

As shown in Figure 11, the MOSFET drain voltage fall time is half of the resonant period of the MOSFET's effective output capacitance and primary-side inductance. The typical value for t$_F$ is 0.6~1.2μs.

## Non-Conduction Time of the MOSFET (t$_{OFF}$)

FL6300A has a minimum non-conduction time of MOSFET (8μs), during which turning on the MOSFET is prohibited. To maximize the efficiency, it is necessary to turn on the MOSFET at the first valley of MOSFET drain-to-source voltage at heavy-load condition. Therefore, the MOSFET non-conduction time at heavy load condition should be larger than 8μs.

Although QR flyback is operated in PFC end for normal operation; when D$_{max}$ is calculated to meet all input conditions, it should take into account the minimum input voltage of V$_{LINE}$ due to the start sequence between PFC and QR flyback at startup.

After determining $f_{S.QR}^{min}$ and t$_F$, the maximum duty cycle is calculated as:

$$D_{max} = \frac{V_{RO}}{V_{LINE} + V_{RO}} \left(1 - f_{S.QR}^{min} \cdot t_F\right) \qquad (20)$$

The primary-side inductance is obtained as:

$$L_m = \frac{\eta_{QR} \cdot (V_{LINE} \cdot D_{max})^2}{2 \cdot f_{S.QR}^{min} \cdot P_{OUT}} \qquad (21)$$

Once L$_m$ is determined, the maximum peak current and RMS current of the MOSFET in normal operation are obtained as:

$$I_{DS}^{PK} = \frac{V_{LINE} \cdot D_{max}}{L_m \cdot f_{S.QR}^{min}} \qquad (22)$$

$$I_{DS}^{RMS} = I_{DS}^{PK} \sqrt{\frac{D_{max}}{3}} \qquad (23)$$

The MOSFET non-conduction time at heavy load is obtained as:

$$t_{OFF} = \frac{(1 - D_{max})}{f_{S.QR}^{min}} \qquad (24)$$

To guarantee the first valley switching at heavy-load condition, *t$_{OFF}$* should be larger than 8μ*s*.
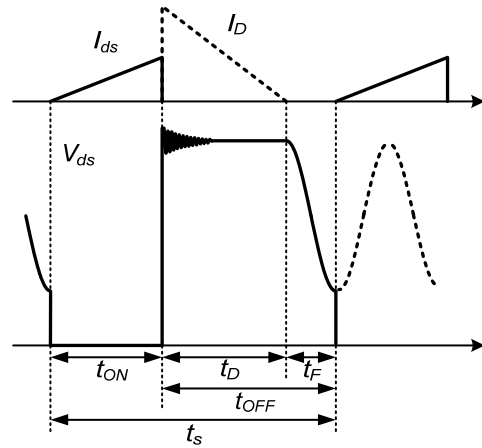


**Figure 11. Switching Timing of QR Flyback Converter**

When designing the transformer, the maximum flux density (B) swing in normal operation as well as the maximum flux density (Bmax) in transient should be considered. The maximum flux density swing in normal operation is related to the hysteresis loss in the core, while the maximum flux density in transient is related to the core saturation.

The minimum number of turns for the transformer primary side to avoid over temperature in the core is given by:

$$N_P^{min} = \frac{L_m \cdot I_{DS}^{PK}}{A_e \cdot \Delta B} \qquad (25)$$

where *B* is the maximum flux density swing in Tesla. If there is no reference data, use B =0.25~0.30T.

Once the minimum number of turns for the primary side is determined, calculate the proper integer for N$_S$ so that the resulting N$_P$ is larger than $N_P^{min}$ as:

$$N_P = n \cdot N_S > N_P^{min} \qquad (26)$$

The number of turns of the auxiliary winding for V$_{DD}$ is given as:

$$N_{AUX} = \frac{V_{DD}^{nom} + V_{FA}}{(V_O + V_F)} \cdot N_S \qquad (27)$$

where $V_{DD}^{nom}$ is the nominal V$_{DD}$ voltage, typically 18V, and V$_{FA}$ is forward-voltage drop of V$_{DD}$ diode.

Once the number of turns of the primary winding is determined, the maximum flux density when the drain current reaches its pulse-by-pulse current limit level should be checked to guarantee the transformer is not saturated during transient or fault condition.

The maximum flux density (B$_{max}$) when drain current reaches I$_{DS}$$^{PK}$ is given as:

$$B_{max} = \frac{L_m \cdot I_{DS}^{PK}}{A_e \cdot N_P} < B_{sat} \qquad (28)$$

B$_{max}$ should be smaller than the saturation flux density. If there is no reference data, use B$_{sat}$ =0.35~0.40T.

**(Design Example)** Setting the minimum frequency is 50kHz and the falling time is 0.8µs:

$$D_{max} = \frac{V_{RO}}{V_{LINE} + V_{RO}}\left(1 - f_{S.QR}{}^{min} \cdot t_F\right)$$

$$= \frac{130}{127 + 130}\left(1 - 50 \times 10^3 \cdot 0.8 \times 10^{-6}\right) = 0.48$$

$$L_m = \frac{\eta_{QR} \cdot (V_{LINE} \cdot D_{max})^2}{2 \cdot f_{S.QR}{}^{min} \cdot P_{OUT}}$$

$$= \frac{0.95 \cdot (127 \cdot 0.48)^2}{2 \cdot 50 \times 10^3 \cdot 70} = 500\mu F$$

$$I_{DS}{}^{PK} = \frac{127 \cdot 0.48}{500 \times 10^{-6} \cdot 50 \times 10^3} = 2.52A$$

$$t_{OFF} = \frac{(1 - D_{max})}{f_{S.QR}{}^{min}} = \frac{1 - 0.48}{50 \times 10^3} = 10\mu s$$

Assuming EER3124 (Ae=102mm2) core is used and the flux swing is 0.29T

$$N_P{}^{min} = \frac{L_m \cdot I_{DS}{}^{PK}}{A_e \cdot \Delta B} = \frac{500 \times 10^{-6} \cdot 2.52}{102 \times 10^{-6} \cdot 0.29} = 41.8$$

$$N_P = n \cdot N_S = 5.3 \cdot 8 = 42.4 > N_P{}^{min}$$

$$N_{AUX} = \frac{V_{DD}{}^{nom} + V_{FA}}{(V_O + V_F)} \cdot N_S = \frac{18 + 1.2}{24.5} \cdot 8 = 6.3$$

Assuming the pulse-by-pulse current limit for PFC output voltage is 120% of peak drain current at heavy load:

$$B_{max} = \frac{L_m \cdot I_{DS}{}^{PK}}{A_e \cdot N_P} = \frac{500 \cdot 2.52 \cdot 1.2}{102 \cdot 42} = 0.34T$$

### 3.2.3. Design the Valley Detection Circuit

Figure 12 shows the DET pin circuitry. The DET pin is connected to an auxiliary winding by $R_{DET}$ and $R_A$. The voltage divider is used for the following purposes:

- Detect the valley voltage of the switching waveform for valley voltage switching. This ensures QR operation, minimizes switching losses, and reduces EMI.

- Produce an offset to compensate the threshold voltage of the peak current limit to provide a constant power limit. The offset is generated in accordance with the input voltage with the PWM signal enabled.

- A voltage comparator and a 2.5V reference voltage provide output OVP. The ratio of the divider determines the output voltage level to stop the gate.
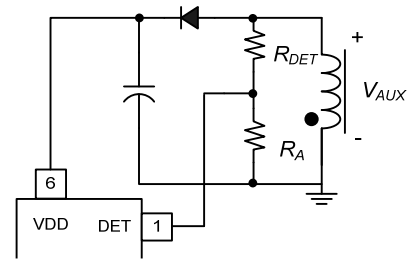


**Figure 12. Detection Pin Section**

First, determine the ratio of the voltage divider resisters. The ratio of the divider determines what output voltage level to stop gate. In Figure 13, the sampling voltage $V_S$ is:

$$V_S = \frac{N_A}{N_S} \cdot V_O \cdot \frac{R_A}{R_{DET} + R_A} < 2.5V \qquad (29)$$

where $N_A$ is the number of turns for the auxiliary winding and $N_S$ is the number of turns for the secondary winding.

Figure 14 shows the internal valley detection block and the output voltage OVP detection block of FL6300A using auxiliary winding to detect $V_O$. The internal timer (minimum $t_{OFF}$ time) prevents the system frequency from being too high. First valley switching is activated after minimum $t_{OFF}$ time of 8µs.

The nominal voltage of $V_S$ is designed around 80% of the reference voltage 2.5V; thus, the recommended value for $V_S$ is 1.9V~2.1V. The output over-voltage protection works by the sampling voltage after the switching-off sequence. A 4µs blanking time ignores the leakage inductance ringing. If the DET pin OVP is triggered, the power system enters latch mode until AC power is removed.
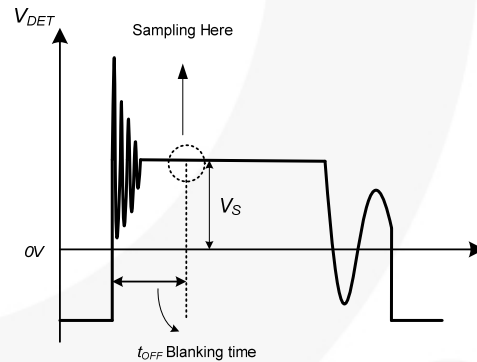


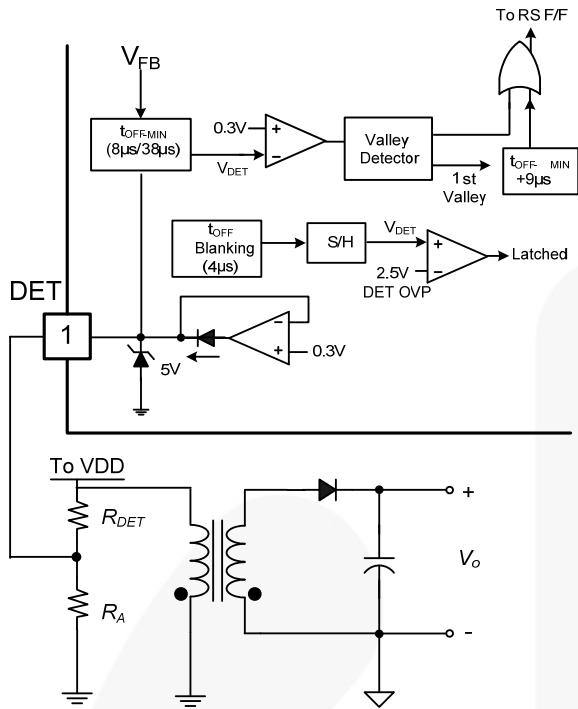**Figure 13. Voltage Sampled After 4µs Blanking Time After Switch-Off Sequence**

**Figure 14. Output Voltage Detection Block**

Once the secondary-side switching current discharges to zero, a valley signal is generated on the DET pin. It detects the valley voltage of the switching waveform to achieve the valley voltage switching. When the voltage of auxiliary winding $V_{AUX}$ is negative (as defined in Figure 12), the DET pin voltage is clamped to 0.3V. $R_{DET}$ is recommended as 150kΩ to 220kΩ to achieve valley voltage switching. After the platform voltage $V_S$ in Figure 13 is determined, $R_A$ can be calculated by Equation 14.

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**(Design Example)** Setting $R_{DET}$ is 200kΩ and $V_S$ is around 80% of the reference voltage 2.5V:

$$V_S = \frac{N_A}{N_S} \cdot V_O \cdot \frac{R_A}{R_{DET} + R_A} = 2.1V$$

$$R_A = \frac{2.1 \times R_{DET}}{\dfrac{N_A}{N_S} \times V_O - 2.1} = 26.4k\Omega$$

---

### 3.2.4. Current-Sensing Resistor for PFC
FL6300A has pulse-by-pulse current limit function. It is typical to set the pulse-by-current limit level at 20~30% higher than the maximum inductor current:

$$R_{CS1} = \frac{0.8}{I_{DS}^{PK}(1 + K_{MARGIN})} \tag{30}$$

where $K_{MARGIN}$ is the margin factor and 0.8V is the cycle-by-cycle current limit threshold.

**(Design Example)** Choosing the margin factor as 35%, the sensing resistor is selected as:

$$R_{CS1} = \frac{0.8}{I_{DS}^{PK}(1 + K_{MARGIN})} = \frac{0.8}{2.52(1 + 0.35)} = 0.23\Omega$$

### 3.2.5. Design the Feedback Circuit
Figure 15 is a typical feedback circuit mainly consisting of a op-amp and a photo-coupler. $R_H$ and $R_L$ form a voltage divider for output voltage regulation. $R_F$ and $C_F$ are adjusted for control-loop compensation. A small-value RC filter (e.g. $R_{FB} = 100$, $C_{FB} = 1nF$) placed from the FB pin to GND can increase stability substantially. The maximum source current of the FB pin is about 1.2mA. The phototransistor must be capable of sinking this current to pull the FB level down at no load. The value of the biasing resistor, $R_{BIAS}$, is determined as:

$$\frac{V_{OP} - V_{OPD}}{R_{BIAS}} \cdot CTR > 1.2 \times 10^{-3} \tag{31}$$

where $V_{OPD}$ is the drop voltage of photodiode, about 1.2V; $V_{OP}$ is the output voltage of operational amplifier (assuming about 2.5V); and CTR is the current transfer rate of the opto-coupler.
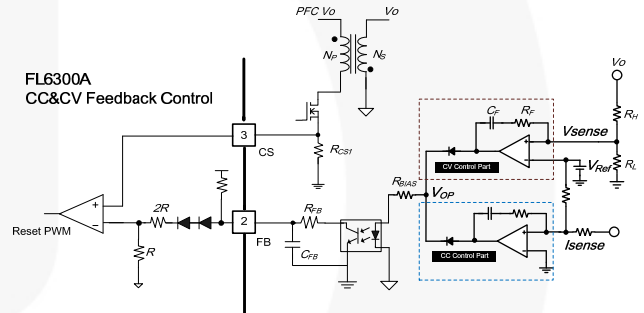


**Figure 15. Feedback Circuit**

The constant voltage and current output is adapted by measuring the actual output voltage and current with some external passive components and op-amp in the reference board. Because the output load, the High Bright LED (HB LED), and some passive components effect the ambient temperature, use the feedback path for stable operation.
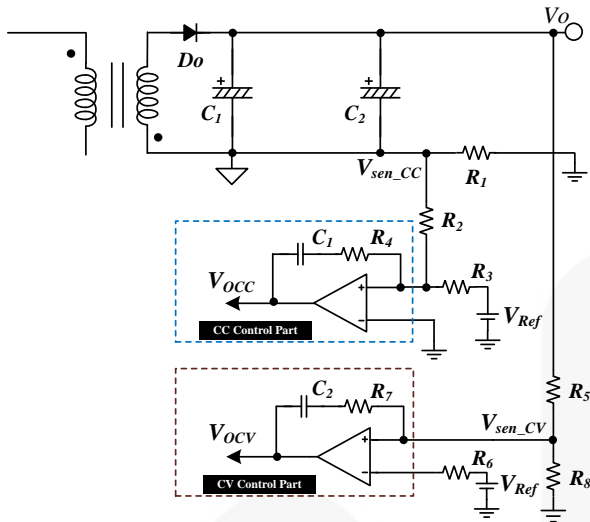
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**Figure 16.    Feedback Circuit for CC/CV
Operation**

$$V_{OCV} = V_{sen\_CV} + \frac{R_7}{R_6}(V_{sen\_CV} - V_{ref}) + \frac{1}{C_2}\frac{1}{R_6}\int(V_{sen\_CV} - V_{ref})\,dt \qquad (32)$$

where the $V_{sen\_CV}$ means the sensing output voltage from the output stage and is divided by $R_4$ and $R_8$ resistor.

Sensing resistor $R_4$ and its value directly effect the CC control block output.

Normally, the CC block is more dominate than the CV block in steady state and the CV block acts as the Over-Voltage Protection (OVP) at transient or abnormal mode, such as no load condition.

The output signal of *CC* block is determined as:

$$V_{OCC} = R_4(\frac{V_{sen\_CC}}{R_2} - \frac{V_{ref}}{R_3}) + \frac{1}{C_1}\int(\frac{V_{sen\_CC}}{R_2} - \frac{V_{ref}}{R_3})\,dt \qquad (33)$$

## 3.3. Schematic of the Evaluation Board
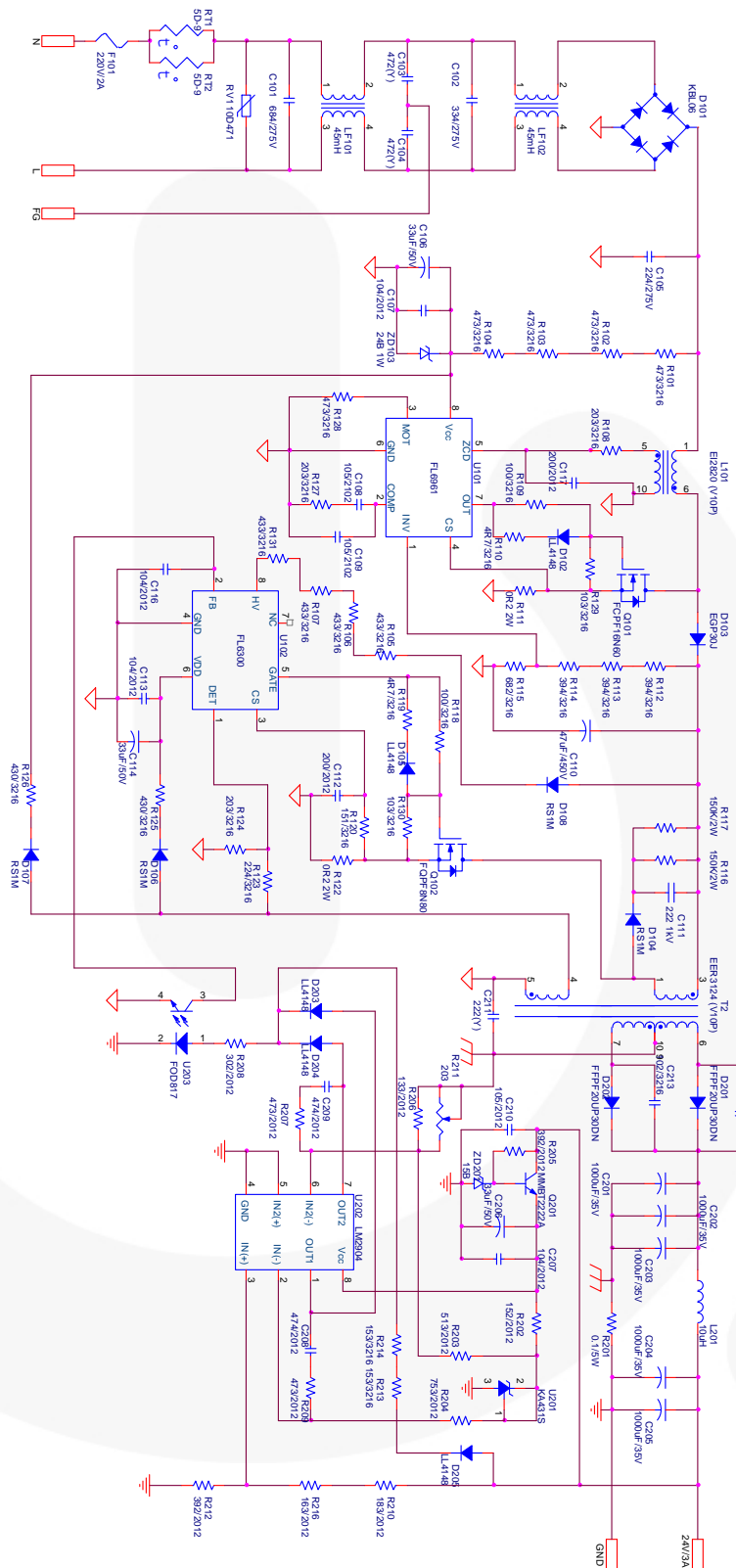


**Figure 17.    Evaluation Board Schematic**

## 3.4. Bill of Materials

| Item No. | Part Reference | Value | Qty. | Description (Manufacturer) |
|---|---|---|---|---|
| 1 | U101 | FL6961 | 1 | CRM PFC Controller (Fairchild Semiconductor) |
| 2 | U102 | FL6300A | 1 | QR PWM Controller (Fairchild Semiconductor) |
| 3 | Q101 | FCPF20N60 | 1 | 600V/20A MOSFET (Fairchild Semiconductor) |
| 4 | Q102 | FQPF8N80 | 1 | 800V/8A MOSFET (Fairchild Semiconductor) |
| 5 | D201,D202 | FFPF20UP30DN | 2 | Ultra-Fast Recovery Power Rectifier (Fairchild Semiconductor t) |
| 6 | D103 | EGP30J | 1 | 600V/3A Ultra-Fast Recovery Diode (Fairchild Semiconductor) |
| 7 | D104,D106,D107,D108 | RS1M | 4 | 1000V/1A Ultra-Fast Recovery Diode (Fairchild Semiconductor) |
| 8 | D101 | KBL06 | 1 | Bridge Diode (Fairchild Product) |
| 9 | Q201 | MMBT2222A | 1 | General-Purpose Transistor (Fairchild Semiconductor) |
| 10 | U202 | LM2904 | 1 | Dual Op Amp (Fairchild Semiconductor) |
| 11 | U203 | FOD817 | 1 | Opto-Coupler (Fairchild Semiconductor) |
| 12 | U201 | KA431S | 1 | Shunt Rregulator (Fairchild Semiconductor) |
| 13 | ZD103 | 24B 1W | 1 | Zener Diode (Fairchild Semiconductor) |
| 14 | ZD201 | 15B | 1 | Zener Diode (Fairchild Semiconductor) |
| 15 | D102,D105,D203,D204, D205 | LL4148 | 5 | General-Purpose Diode (Fairchild Semiconductor) |
| 16 | C101 | 684/275V | 1 | X – Capacitor |
| 17 | C102 | 334/275V | 1 | X – Capacitor |
| 18 | C105 | 224/275V | 1 | X – Capacitor |
| 19 | C103,C104 | 472(Y) | 2 | Y – Capacitor |
| 20 | C211 | 222(Y) | 1 | Y – Capacitor |
| 21 | C106,C114,C206 | 33µF/50V | 3 | Electrolytic Capacitor, 105°C |
| 22 | C107,C113,C116,C207 | 104/2012 | 4 | SMD Capacitor 2012 |
| 23 | C108,C109, C210 | 105/2102 | 3 | SMD Capacitor 2012 |
| 24 | C110 | 68µF/450V | 1 | Electrolytic Capacitor, 105°C |
| 25 | C111 | 222 1kV | 1 | Ceramic-Capacitor |
| 26 | C112,C117 | 200/2012 | 2 | SMD Capacitor 2012 |
| 27 | C201,C202,C203,C204, C205 | 1000µF/35V | 5 | Electrolytic Capacitor, 105°C |
| 28 | C208,C209 | 474/2012 | 2 | SMD Capacitor 2012 |
| 29 | C212,C213 | 102/3216 | 2 | SMD Capacitor 3216 |
| 30 | F101 | 220V/2A | 1 | Fuse |
| 31 | L101 | EI2820 | 1 | PFC Inductor (V10P), 450µH |
| 32 | L201 | 10µH | 1 | Stick Inductor |
| 33 | LF101,LF102 | 45mH | 2 | Line Filter |
| 34 | R101,R102,R103,R104 | 104/3216 | 4 | SMD Resistor 3216 |
| 35 | R128 | 393/3216 | 1 | SMD Resistor 3216 |
| 36 | R105,R106,R107,R131 | 433/3216 | 4 | SMD Resistor 3216 |
| 37 | R108,R124,R127 | 203/3216 | 3 | SMD Resistor 3216 |
| 38 | R109,R118 | 100/3216 | 2 | SMD Resistor 3216 |
| 39 | R110,R119 | 4R7/3216 | 2 | SMD Resistor 3216 |
| 40 | R111,R122 | 0R2 2W | 2 | Metal Film Resistor 2W |
| 41 | R112,R113,R114 | 394/3216 | 3 | SMD Resistor 3216 |
| 42 | R115 | 682/3216 | 1 | SMD Resistor 3216 |
| 43 | R213,R214 | 153/3216 | 2 | SMD Resistor 3216 |
| 44 | R116,R117 | 150KΩ/2W | 2 | Metal Oxide Film Resistor 2W |

## Bill Of Materials (Continued)

| Item No. | Part Reference | Value | Qty. | Description (Manufacturer) |
|----------|----------------|-------|------|----------------------------|
| 45 | R120 | 151/3216 | 1 | SMD Resistor 3216 |
| 46 | R123 | 224/3216 | 1 | SMD Resistor 3216 |
| 47 | R125,R126 | 430/3216 | 2 | SMD Resistor 3216 |
| 48 | R129,R130 | 103/3216 | 2 | SMD Resistor 3216 |
| 49 | R201 | 0.1/5W | 1 | MPR Resistor 5W |
| 50 | R202 | 152/2012 | 1 | SMD Resistor 2012 |
| 51 | R203 | 513/2012 | 1 | SMD Resistor 2012 |
| 52 | R204 | 753/2012 | 1 | SMD Resistor 2012 |
| 53 | R205 | 392/2012 | 1 | SMD Resistor 2012 |
| 54 | R206 | 133/2012 | 1 | SMD Resistor 2012 |
| 55 | R207,R209 | 473/2012 | 2 | SMD Resistor 2012 |
| 56 | R208 | 302/2012 | 1 | SMD Resistor 2012 |
| 57 | R212 | 432/2012 | 1 | SMD Resistor 2012 |
| 58 | R210 | 153/2012 | 1 | SMD Resistor 2012 |
| 59 | R216 | 223/2012 | 1 | SMD Resistor 2012 |
| 60 | R211 | 20kΩ | 1 | Variable Resistor |
| 61 | RT1,RT2 | 5D-9 | 2 | NTC |
| 62 | T2 | EER3124 | 1 | QR Transformer(V10P), 500µH |
| 63 | RV1 | 10D471 | 1 | VARISTOR |

## 4.0 Related Datasheets

FL6961 - *Single Stage Flyback and Boundary Mode PFC Controller for Lighting* –

FL6300A -*Quasi-Resonant Current Mode PWM Controller for Lighting*

*Application Note -* AN-6300 FAN6300/A/H - Highly Integrated Quasi-Resonant PWM Controller

*Application Note -* AN-6961- Critical Conduction Mode PFC Controller

## PUBLICATION ORDERING INFORMATION