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Application Note AN-9041

PFC SPM® Design Guide with Analog PFC IC

Written by:

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FAIRCHILD SEMICONDUCTOR

Contents

NOTE:

In this and other Fairchild documentation and collateral, the following terms are interchangeable: DIP = SPM2, Mini-DIP = SPM3, Tiny-DIP = SPM5, µMini-DIP = SPM45H, PFCM = PFC SPM®.

1. System Configurations

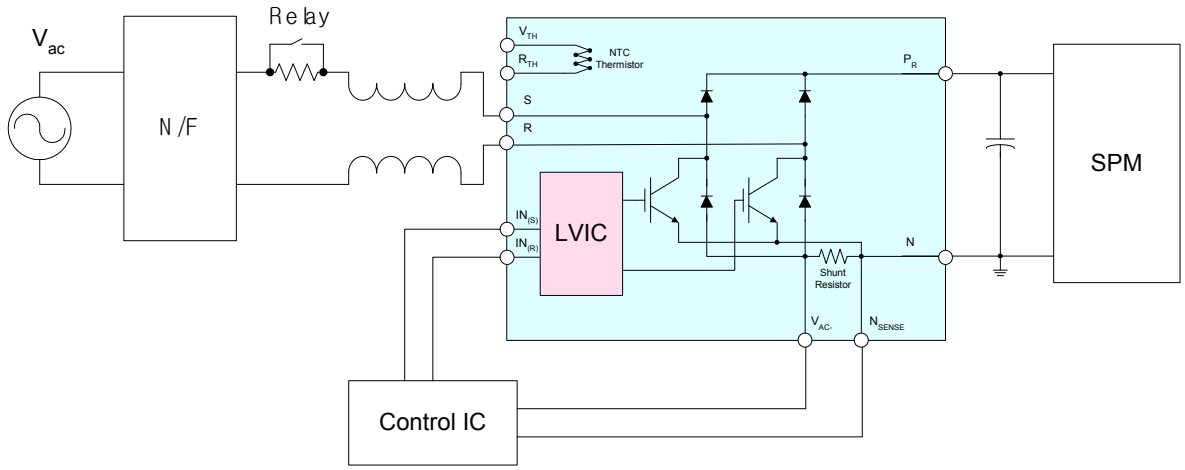


Fig.1 Typical block diagram of PFC SPM® system

An inrush-current prevention circuit is required due to the large DC link capacitance as shown in Fig. 1. The relay of the circuit should be closed after DC link capacitor is charged far enough. PFC SPM®, mini-SPM and control IC can share single GND stage. Usually, this GND and the N_{SENSE} terminal of PFC SPM should have the same potential. Large surge voltage is easily produced between P and N terminals by large current switching. To reduce surge voltage it is important to shorten the DC link bus wiring between PFC SPM and DC link capacitor. In addition, good high frequency characteristic capacitor, such as polypropylene film capacitor should be mounted near to P and N terminals as a snubber.

2. Protection Circuits

Following Fig. 2 shows the timing chart of protection function. There are two kind of protection level for both OCP and OVP. Generally, PFC control ICs have its own OCP and OVP function. Also, user can make the PFC SPM® stop and output the FO signal under preset OC, OV condition using its Csc input.

Over Current Protection (OCP)

[OCP Level1 –PFC SPM®] PFC SPM can protect from over current situation. When OC(over current) situation happens, the PFC SPM stops operating and generates fault out signal during fault-out duration time(set by C_{FOD}). And then after the duration, it works again according to the input command. Its total propagation delay time may depend on outer op-amp speed. We recommend using a low cost slow op-amp solution with fast protection. It is the OCP level2 protection described in next paragraph.

[OCP Level2 (SCP) –PFC control IC] By the peak current limit function of PFC control IC, the system is protected from SC(Short Circuit) situation. The recommended current limit of OCP level 2 is higher than that of OCP level 1. It doesn't generate the fault out signal but its response is very fast. It will protect the system from short circuit situation during the propagation delay time of OCP level1.

Over Voltage Protection

OV (Over Voltage) protection can be also implemented by dual protection. The DC-link voltage changes slowly because of its large capacitance. So OVP does not need fast response. Therefore it is optional to activate the OVP of PFC controller.

[OVP Level 1 - PFC controller] OVP level 1 suppresses voltage overshoot in transient situation. It doesn't generate fault out signal.

[OVP Level 2 – PFC SPM®] The voltage level of OVP level 2 is higher than that of OVP level 1. When OV situation happens, the PFC SPM stops operating and generates fault out signal during fault-out duration time(set by C_{FOD}). And then it works again.

Under Voltage Protection

IGBT gate will be interrupted when control voltage drops below UV trip level, and the protection will be realeased automatically if the control voltage recovers to the UV reset level.

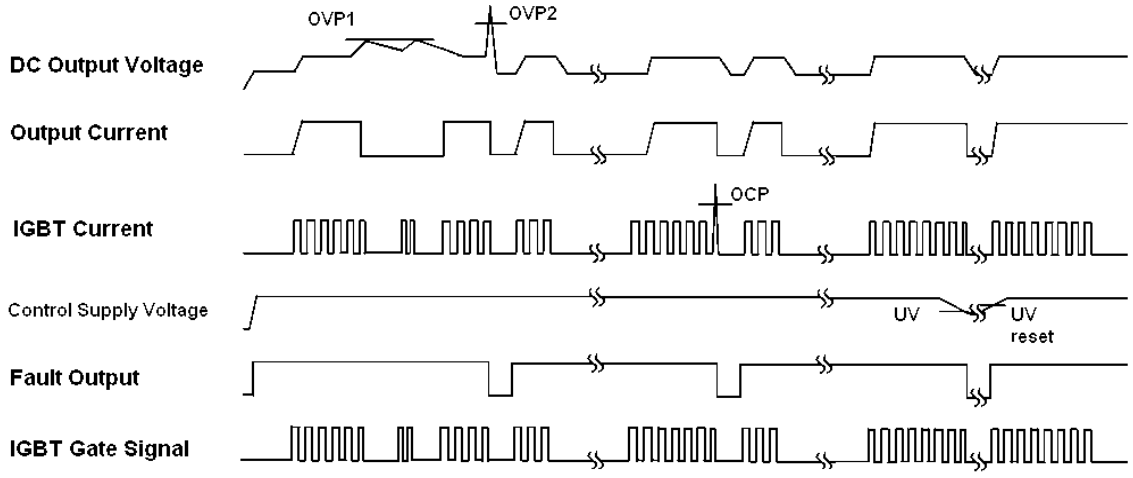


Fig.2 Timing chart of protection function

3. Design Example (PFC SPM® DEMO BOARD)

A general PFC example is implemented for 5[kW] air-conditioning applications whose input voltage is 187~276[V].

Operating conditions of PFC SPM® demo board:

Table 1. The operating conditions.

	Item	Symbol	Value	Unit
1	Switching Frequency	Fsw	40	KHz
2	Minimum Input Voltage	Vimin	176	Vac
3	Nominal Input Voltage	Vinom	220	Vac
4	Maximum Input Voltage	Vimax	264	Vac
5	Output Max. Power	Po	5000	W
6	Minimum Output Voltage	Vomin	350	Vdc
7	Nominal Output Voltage	Vonom	380	Vdc
8	OVP level 1	V_{OV1}	420	V
9	OVP level 2	V_{OV2}	440	V
10	Peak Ripple Current	Iripple	5	A
11	OCP Level1	Iocp1	40	A
12	OCP Level2 (SCP)	Iocp2	50	A
13	Shunt Resistor	Rsh	2	MOhm
14	DC Capacitor	Cout	940	uF

Output capacitance and Inductance design

Output Voltage Ripple & Output Capacitance

$$|V_{OUTRIPPLE}|_{PEAK} = I_{OUTDC}\sqrt{\left(\frac{1}{4\pi f_L \times C_{OUT}}\right)^2 + ESR^2}$$

where:

f_L = line frequency.

ESR = the ESR of the output capacitor.

Voltage ripple of V_{DC} can be reduced by employing large C_{OUT}. In demo board, C_{OUT} is set to 940[μF] (470[μF] x 2)

Inductance & Input Current Ripple

$$\Delta I_{L_{p-p}} = \frac{V_{IN}(V_{OUTDC} - V_{IN})}{fLV_{OUTDC}}$$

where: ΔI_{Lp-p} : Peak to peak current of PFC inductor

V_{IN} : Input AC voltage

V_{OUTDC} : DC link Voltage

f : Switching frequency

L : Inductance of PFC inductor

$$\Delta I_{L_{p-p}} = \frac{V_{IN}(V_{OUTDC} - V_{IN})}{fLV_{OUTDC}}$$

$$\therefore (\Delta I_{L_{p-p}})_{MAX} = \frac{V_{OUTDC}}{4fL} \quad (\because V_{IN} = \frac{1}{2}V_{OUTDC})$$

$$(\Delta I_{L_{p-p}})_{MAX} = 5A \rightarrow L = \frac{V_{OUTDC}}{20f} = \frac{380}{20 \cdot 40000} = 475[\mu H] \text{ (fs=40kHz)}$$

Current ripple is decided by switching frequency and inductance. To reduce current ripple, high switching frequency and large inductance value is required. It means that employing higher switching frequency can reduce inductor size. But the power losses will increase and it requires more efficient heat sink structure.

Open Loop Response

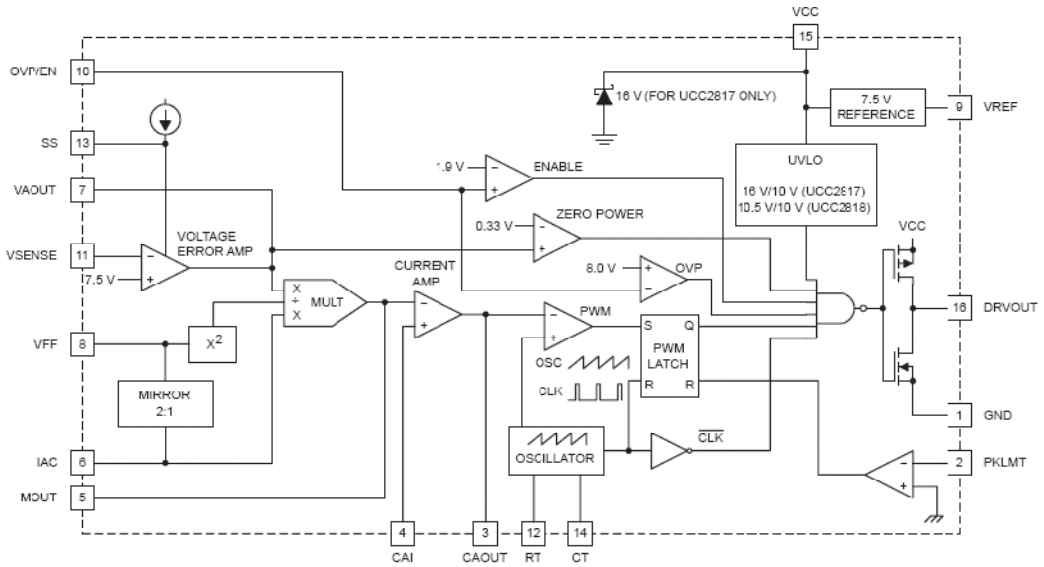


Fig.3 Block diagram of PFC control IC

The following is the block diagram of PFC controller ucc3818. The average current mode control is composed of two types of loops- voltage loop and current loop. The voltage loop controls the output DC-Link voltage. It regulates the output voltage. There is a 120[Hz] ripple voltage in the output DC-Link, which is caused by the 60[Hz] ac input current. Hence, the voltage loop must be designed to be slow enough to reject the 120[Hz] ripple voltage.

In general CCM (Continuous Current Mode) PFC IC, there is a multiplier. It multiplies V_{EA}(the output of voltage loop) by I_{AC}(reference of input ac current shape) and then divides it by V_{RMS}(reference of rms input voltage). The output($I_{MO} = K \cdot \frac{V_{EA} \cdot I_{AC}}{V_{RMS}^2}$) of a multiplier is the reference of the PFC's input current(I_{AC}).

The difference between the voltage of I_{MO} pin(output of the multiplier) and the voltage of the current sensing resister is amplified by the current loop. The V_{EA}(output of the current loop) is the reference voltage to the comparameter that generates the gating signal. Current loop should be fast enough to catch up with the 120[Hz] input ac current. But too fast speed can distort the current shape due to the switching noise. Therefore, the current loop must be designed to be fast enough to catch up with the 120[Hz] rectified input current, but not too fast for switching noise immunity.

Current Loop Amplifier

Eq. 1 shows the open loop response of power stage. (Refer to UCC3818 datasheet)

$$G_{PST} = \frac{V_S(s)}{V_{IAOUT}(s)} = \frac{V_{DC} R_{SH}}{4sL} \quad \text{(UCC3818)} \qquad \text{(Eq.1)}$$

where: V_S : Voltage of shunt resistor

V_{IAOUT} : Voltage of R_{MO}

V_{DC} : DC link Voltage

R_{SH} : Shunt resistance for current sensing (2mohm)

L : PFC inductance

s : $j\omega (= j \cdot 2\pi f)$

Voltage Loop Amplifier

Eq. 2 shows the open loop response of power stage. (Refer to UCC3818 datasheet)

$$G_{V.O.L.} = \frac{P_{IN}}{sC_{OUT} V_{OUTDC} \Delta V_{EAOUT}} \quad \text{(UCC3818)} \qquad \text{(Eq.2)}$$

where: P_{IN} : Input power

C_{OUT} : DC link capacitance

V_{OUTDC} : DC link voltage

ΔV_{EAOUT} : Error amplifier output difference (≈5V)

s : $j\omega(= j\cdot 2\pi f)$

Control Loop Implementation

Current Loop

[Step 1] Crossover frequency

Theoretical crossover frequency is given by following equation.

$$f_C = \frac{f_S}{6} \Rightarrow 6.7kHz \qquad \text{(Eq.3)}$$

[Step 2] Fz and Fp decision

$$f_Z = \frac{f_C}{2} = 3.3kHz, \quad f_P = 6 f_Z = 20kHz$$

[Step 3] Rz, Cp, Cz decision

R_i is same to R_{MO}. (Refer to "other parameters" in page 10)

R_i = 470[Ω],

In Eq.1, $G_{PST}\Big|_{f_C=6.6kHz} = \frac{V_{DC}R_{SH}}{4sL} = \frac{V_{DC}R_{SH}}{4(2\pi f_C)L} = 0.0103 = -39.8dB$

Therefore it requires 40dB boosting at fc(=6.6kHz).

R_z is given by Eq.7.

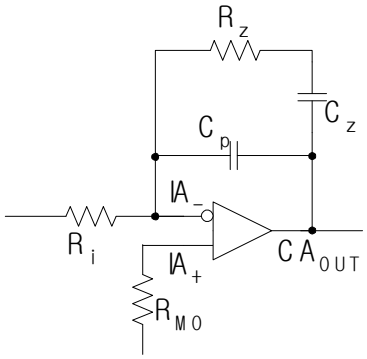
$|G|_{dB} = 20\log\frac{R_z}{R_i} = 40dB$ → R_z = 47[kΩ],

From Eq.4 ,Eq.5, Cp and Cz is given.

C_p = 180[pF], C_z = 1[nF]

$$f_z = \frac{1}{2\pi R_z C_z} \qquad \text{(Eq.4)}$$

$$f_p = \frac{C_z + C_p}{2\pi R_z C_z C_p} \qquad \text{(Eq.5)}$$



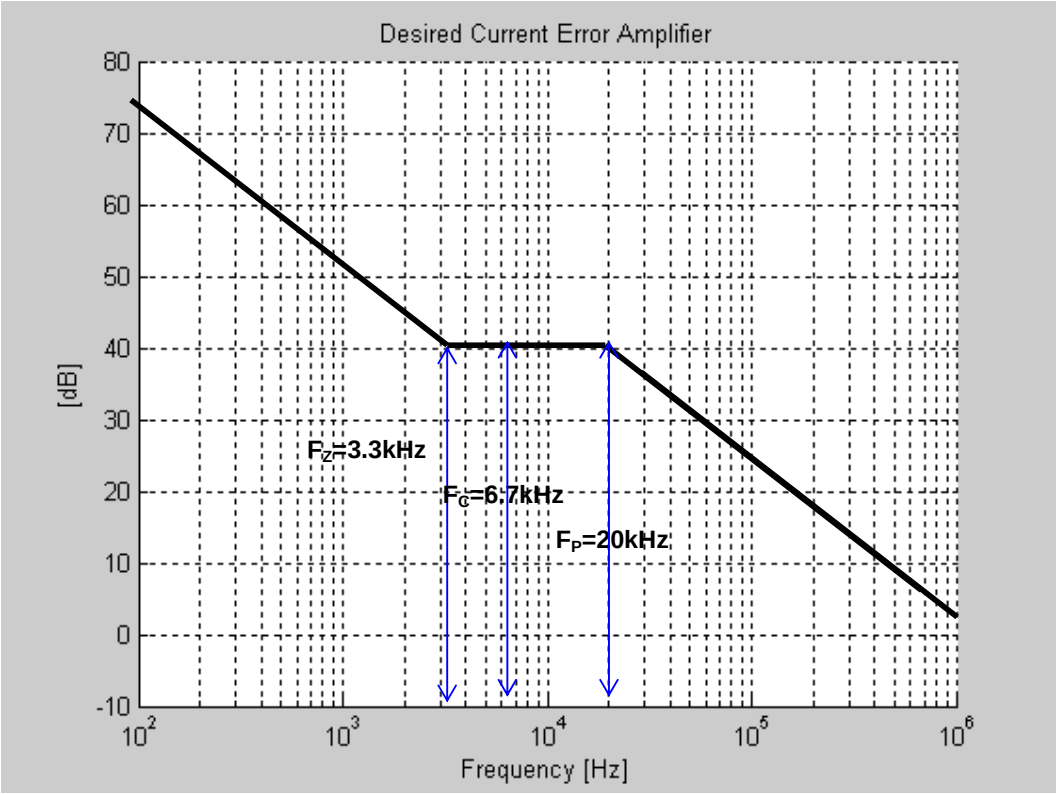


Fig.4 Current loop circuit

Fig.5 Desired current error amplifier response

[1] $$|G|_{dB} = 20\log\frac{1}{2\pi f R_i C_z} \quad \text{(Eq.6)}$$

[2] $$|G|_{dB} = 20\log\frac{R_z}{R_i} \quad \text{(Eq.7)}$$

[3] $$|G|_{dB} = 20\log\frac{1}{2\pi f R_i C_p} \quad \text{(Eq.8)}$$

Voltage Loop

$$G_{V.O.L.}\Big| = \frac{P_{IN}}{sC_{OUT}V_{OUTDC}\Delta V_{EAOUT}} = \frac{5000}{2\pi f \cdot 0.001 \cdot 380 \cdot 5} = \frac{419}{f}$$

A resistor(R_{VD}) is added between E/A input and sensing resistor. By virtue of large R_{VD}, C_{VF} can be replaced by small SMD type capacitor.

→ $R_{VD} = 120k\Omega$ (>R_{VS})

$R_{VF} = 8 \cdot R_{VD} \approx 1M\Omega$ (>R_{VD})

$f_{CV} = \frac{1}{2\pi R_{VD} C_{VF}} << 120$ → C_{VF}=1uF $\left(f_{CV} = 1.3Hz\right)$

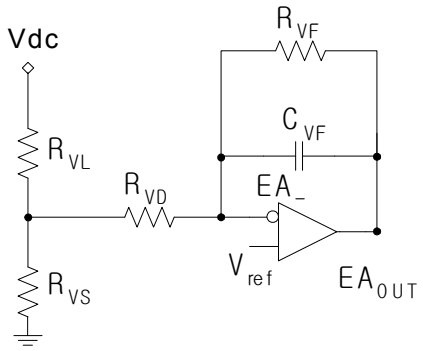


Fig.6 Voltage loop circuit

Other Parameters

R_T, C_T: Switching frequency decision

$$f = \frac{0.6}{R_T C_T}$$

R_T = 15[kΩ]

C_T = 1[nF]

➔ F_s = 40[kHz]

R_{MO}: (Refer to fig.4)

$$R_{MO} = \frac{I_{AC\_peak} \cdot R_{sense}}{I_{GMMAX}} = \frac{50\sqrt{2} \cdot 0.002}{300 \times 10^{-6}} = 471 \approx 470[\Omega]$$

(Assuming the input current is $50A_{RMS}$ @ $V_{AC} = 100V_{RMS}$)

➔ $R_{MO} = 470[\Omega]$

$R_{sense} = 0.002[\Omega]$(small resistance can cause distortions at low level current)

R_{AC} & Optocoupler circuit:

Optocuopler: TLP180

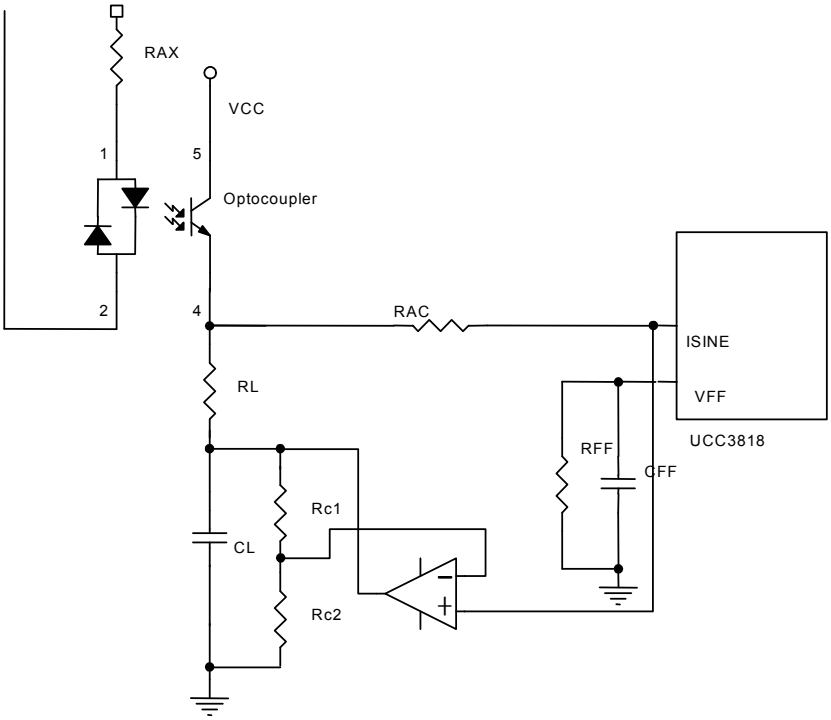


Fig.7 Input AC voltage sensing circuit

R_{AX} and R_L depend on optocoupler :

$$R_{AX} = \frac{V_{RMS\_\max} \cdot \sqrt{2}}{I_{LINEAR\_\max}} = \frac{270 \cdot \sqrt{2}}{6 \times 10^{-3}} = 64[k\Omega]$$

→ $18 + 18 + 18 + 18[k\Omega](0.5 \times 4 = 2W)$

$$R_{AC} = \frac{V_{RL\_PEAK}}{I_{AC\_\max}} = \frac{9}{0.5 \times 10^{-3}} = 18[k\Omega]$$

$$R_L = 390[\Omega]$$

R_{C1} , R_{C2} , C_L, and an op-amp→ I_{SINE} off-set compensation

$C_L = 1[uF]$, $R_{C1} = 0[\Omega]$, $R_{C2} = 150[\Omega]$,

V_{FF}:

$V_{FF} = 1.4[V]$ (when, input voltage V_{AC} = 90[V_{AC}])

R_{FF} = 33[kΩ], C_{FF} = 100[uF]

Over Current Protection

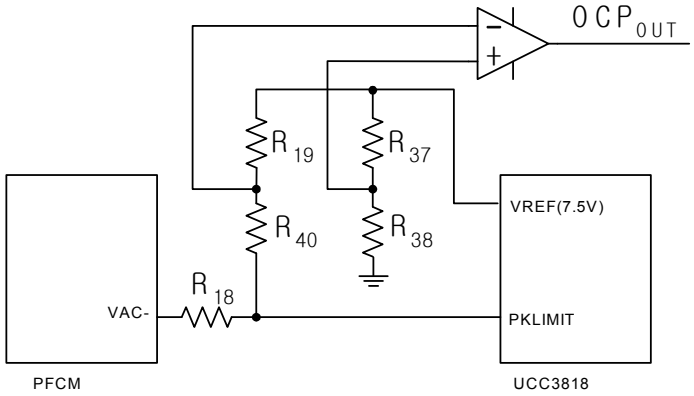


Fig.8 Over current protection circuit

The actual protection level can be slightly different from the calculated value. It depends on PCB layout pattern. About demo board, the designed values are:

R_{18} = R_{40} = 1.2[kΩ], R_{19} = R_{37} = 82[kΩ], R_{38} = 1.5[kΩ]

And the expected OC levels are:

1) OCP level 1

$$\frac{R_{38}}{R_{37}}V_{REF} = \frac{(R_{18}+R_{40})V_{REF} - R_{SH}I_{PK}R_{19}}{R_{18}+R_{19}+R_{40}} \Rightarrow I_{PK} = \frac{V_{REF}}{R_{SH}R_{19}}\left(R_{18}+R_{40}-\frac{R_{38}}{R_{37}}(R_{18}+R_{19}+R_{40})\right)$$

$$\therefore I_{PK} \approx 40[A]$$

2) OCP level 2

$$\frac{R_{19}+R_{40}}{R_{18}} = \frac{V_{REF}}{R_{SH}I_{PK}} \Rightarrow I_{PK} = \frac{R_{18}V_{REF}}{R_{SH}(R_{19}+R_{40})}$$

$$\therefore I_{PK} \approx 50[A]$$

Over Voltage Protection

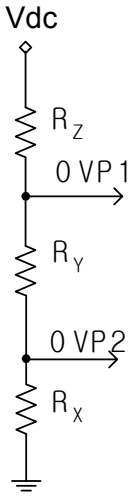


Fig.9 Over voltage protection circuit

About demo board, the designed values are:

R_X = 15 [kΩ], R_Y = 1.8 [kΩ], R_Z = 870 (270+270+330) [kΩ]

And the expected OC levels are:

1) OVP level 1

$$\frac{R_X + R_Y}{R_X + R_Y + R_Z} = \frac{V_{REF\_OV}}{V_{DC\_PK}} \Rightarrow V_{DC\_PK} = \frac{R_X + R_Y + R_Z}{R_X + R_Y} V_{REF\_OV} = \frac{886.8}{16.8} \cdot 8 = 422[V]$$

2) OVP level 2

$$\frac{R_X}{R_X + R_Y + R_Z} = \frac{V_{REF}}{V_{DC\_PK}} \Rightarrow V_{DC\_PK} = \frac{R_X + R_Y + R_Z}{R_X} V_{REF} = \frac{886.8}{15} \cdot 7.5 = 443[V]$$

DC-link Voltage Control

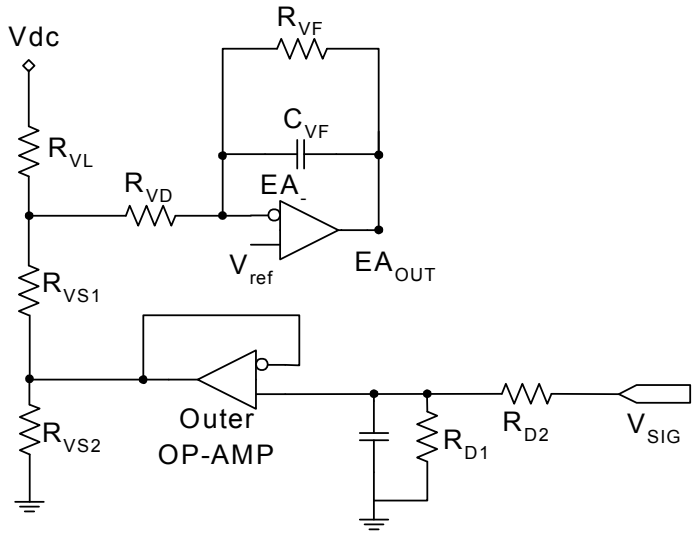


Fig.10 DC link voltage control circuit

The relation between V_{DC} and parameters is:

$$V_{DC} = 7.5\left(R_{VL}\left(\frac{R_{VD}}{R_{VF}R_{VS1}} + \frac{1}{R_{VF}} + \frac{1}{R_{VS1}} \right) + \frac{R_{VD}}{R_{VF}} + 1 \right) - \frac{1}{R_{VF}}\left(R_{VD} + R_{VL} + \frac{R_{VL}R_{VD}}{R_{VS1}} \right) V_{EA} - \frac{R_{VL}}{R_{VS1}}\left(\frac{R_{D1}}{R_{D1} + R_{D2}} \right) V_{SIG}$$

The variable V_{DC} voltage is available by just changing V_{SIG} voltage. V_{EA}, the output of voltage error amplifier changes from 0 to 5.5V as its load current. In no load condition, V_{EA} value is almost zero. And the voltage of V_{DC} will be the highest value. The next graph shows V_{SIG} and V_{DC} voltage. The voltage of V_{DC} in low load condition is higher than that of max. load condition.

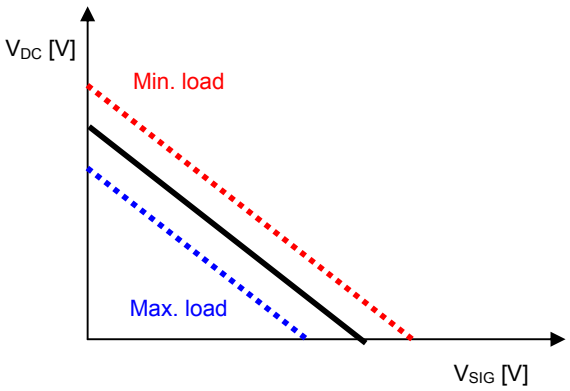


Fig.11. DC link voltage vs. control voltage

4. Experimental Results

Fig. 12 shows the overall schematics of implemented PFC converter. Table 2 shows the components that are used for the implemented hardware. Fig. 13 shows the input ac current and DC-link voltage waveforms. These figures' details are shown in table 3.

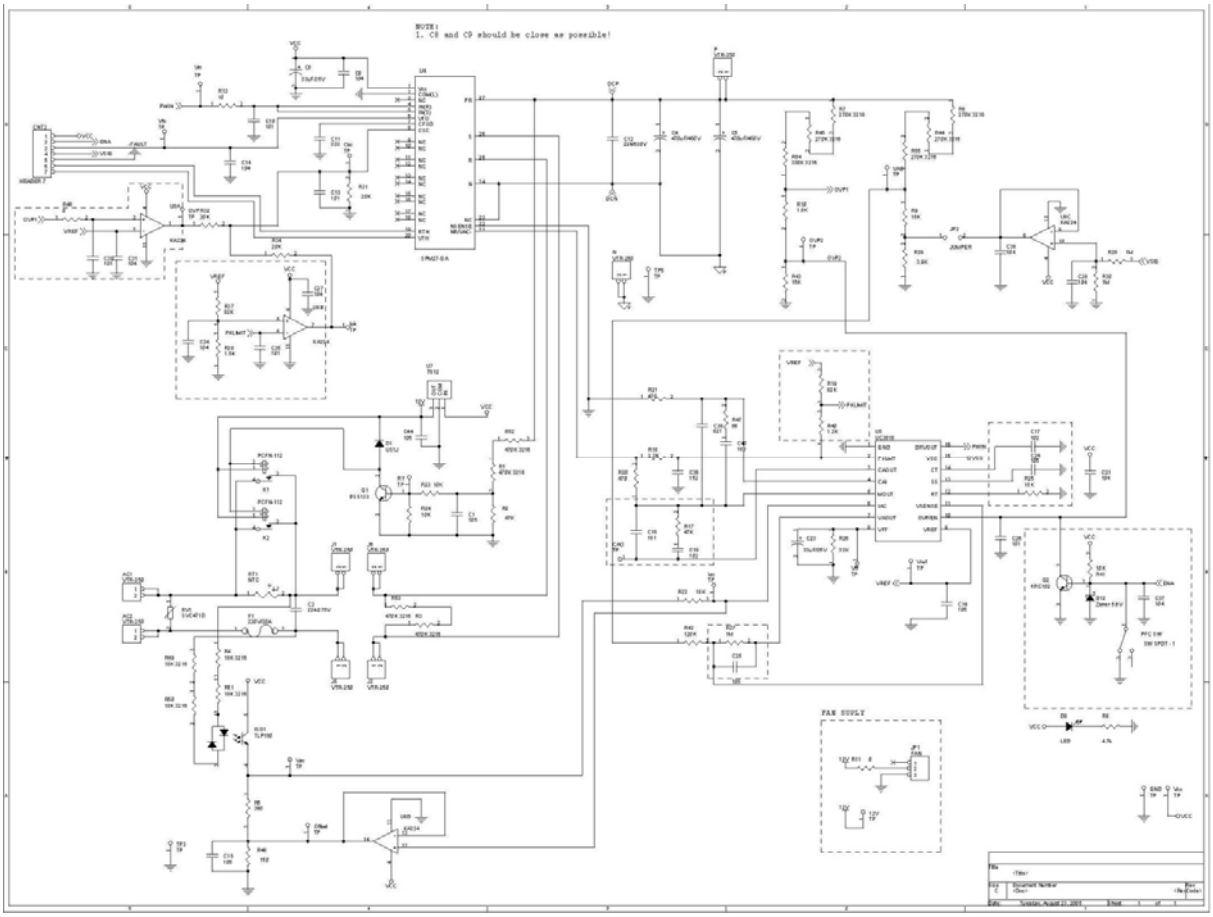


Fig.12. Schematic diagram of the implemented PFC converter.

Table 2. BOM of PFC SPM® demo board.

Item	Part	Reference	Quantity
1	C-Ceramic : 101 2012	C10,C13,C26,C30,C35	5
2	C-Ceramic : 102 2012	C17,C18	2
3	C-Ceramic : 104 2012	SC2,SC4,C9,C14,C21,C27,C29,C31,C34,C37,C38	11
4	C-Ceramic : 105 2012	C1,C15,C19,C24,C25,C44,SC6	7
5	C-Ceramic : 152 2012	C36	1
6	C-Ceramic : 183 2012	C40	1
7	C-Ceramic : 221 2012	C16	1
8	C-Ceramic : 333 2012	C11,SC7	2
9	C-Ceramic : 821 2012	C39	1
10	C-Elec : 220uF 35V	SC5	1
11	C-ELEC : 33uF 35V	C8,C23	2
12	C-ELEC : 470uF 450V	C4,C5	2
13	C-Elec : 47uF 35V	SC3	1
14	C-FILM : 105 630V	C12	1
15	C-FILM : 220nF AC275V	C2	1
16	Connector : 7-pin, 2.54mm pitch	CNT2	1
17	DIODE : US1J	D1,SD2,SD3,SD4	4
18	FAN connector : 3-pin, 2.54mm pitch	JP1	1
19	FPS : KA5M02659RN	U10	1
20	Fuse : 220V/20A	F1	1
21	JUMPER : 2-pin, 2.54mm pitch	JP2	1
22	LED	D8	1
23	Main Relay : PCFN-112	K1,K2	2
24	Mosfet : BSS138	Q1	1
25	NTC : 6D-22	RT1	1
26	Op-Amp : KA224	U8	1
27	Opto-coupler : TLP180	ISO1	1
28	Opto-coupler : TLP181	ISO2	1
29	PFC IC : UC3818	U5	1
30	PFCM : FPDB30PH60	U4	1
31	R-Chip : 0ohm, 1/8W, J, 2012	R11,R46	2
32	R-Chip : 1.2Kohm, 1/8W, J, 2012	R40,R18	2
33	R-Chip : 1.5Kohm, 1/8W, J, 2012	R38	1
34	R-Chip : 1.8kohm, 1/8W, F, 2012	SR6,R10	2
35	R-Chip : 1.8kohm, 1/8W, J, 2012	SR2	1
36	R-Chip : 100kohm, 1/2W, J, 5025	SR7,SR8	2
37	R-Chip : 10Kohm, 1/8W, J, 2012	SR4,R23,R24,R41	4
38	R-Chip : 10ohm, 1/8W, J, 2012	R13	1
39	R-Chip : 10ohm, 1/8W, J, 2012	SR1	1
40	R-Chip : 120Kohm, 1/8W, J, 2012	R42	1
41	R-Chip : 150ohm, 1/8W, J, 2012	R48	1
42	R-Chip : 15Kohm, 1/8W, J, 2012	R9,R25,R43	3
43	R-Chip : 18Kohm, 1/4W, J, 3216	R4,R49,R50,R51	4
44	R-Chip : 18Kohm, 1/8W, J, 2012	R22	1
45	R-Chip : 1Mohm, 1/8W, J, 2012	R27,R28,R30	3
46	R-Chip : 20Kohm, 1/8W, J, 2012	R31,R32,R34	3
47	R-Chip : 270Kohm, 1/4W, F, 3216	R6,R7,R44,R45,R55	5
48	R-Chip : 3.3kohm, 1/8W, J, 2012	SR3	1
49	R-Chip : 3.9Kohm, 1/8W, J, 2012	R29	1
50	R-Chip : 33Kohm, 1/8W, J, 2012	R26	1
51	R-Chip : 330Kohm, 1/4W, F, 3216	R54	1
52	R-Chip : 390ohm, 1/8W, J, 2012	R5	1
53	R-Chip : 4.7Kohm, 1/8W, J, 2012	R8	1
54	R-Chip : 470Kohm, 1/4W, F, 3216	R1,R3,R52,R53	4
55	R-Chip : 470ohm, 1/8W, J, 2012	R20,R21	2
56	R-Chip : 47Kohm, 1/8W, J, 2012	R2,R17	2
57	R-Chip : 56ohm, 1/8W, J, 2012	R47	1
58	R-Chip : 82Kohm, 1/8W, J, 2012	R19,R37	2
59	R-Chip : 9kohm, 1/8W, F, 2012	SR5	1
60	Regulator : KA78M12	U7	1
61	Switch : SW SPDT - 1	PFC SW	1
62	Terminal : VTR-250	J1,J2,J5,J6,AC1,AC2,P,N	8
63	TR : KRC102	Q2	1
64	Transformer : EI-1916	T1	1
65	TVS : SMBJ170	SD1	1
66	Varistor : SVC471D	RV1	1
67	Voltage detector : KA431A	SD5	1
68	Zener Diode : 1N4734A, 5.6V	D12	1

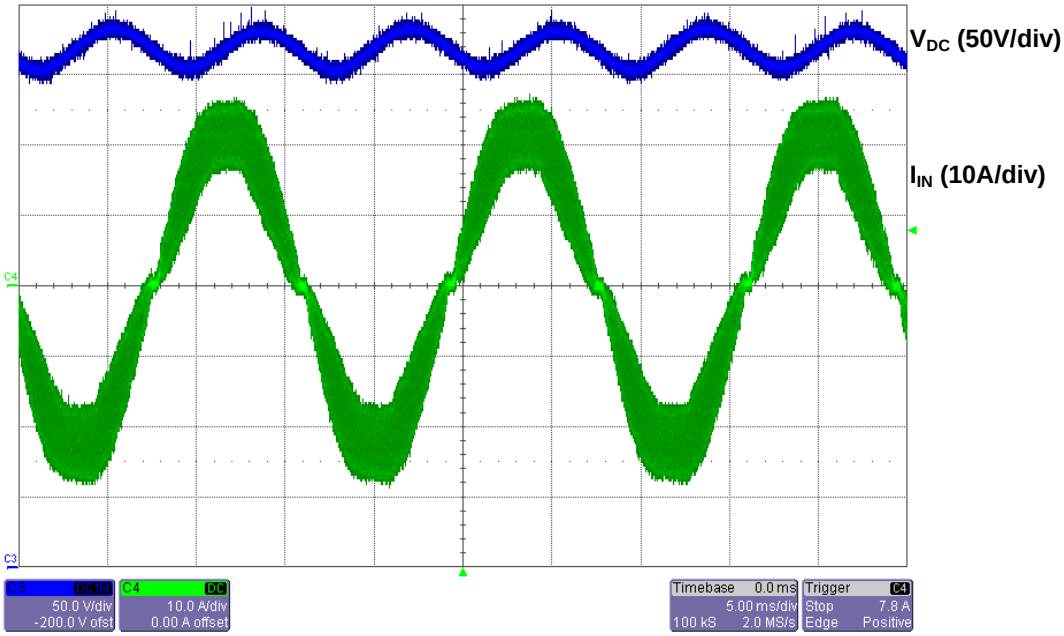


Fig. 13. Full load test results (I_{IN} = 16A_{RMS})

Table 3. Power factor and input power measurement.

	V_{AC} [V]	I_{AC} [A]	Power [kW]	Power Factor [%]
Fig.13	220	16	3.5	99

**** V_{AC} and I_{AC} are RMS values***

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