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# AN-4176

## 1 kV SenseFET Integrated Power Switch

### 1. Abstract

Some industrial equipment that are supplied from a three-phase AC power source such as industrial drives and energy meters often need an auxiliary power supply stage that can provide a regulated low-power DC source for analog and digital circuitry.

This power supply stage requests special specifications such as;

- Wide AC input voltage: 45 V<sub>AC</sub> to 460 V<sub>AC</sub>
- Robust system against high line surge
- Protection against magnetic contact test
- Large output capacitance to keep long hold-up time after power-off

Designing this power supply is a challenge because high voltage MOSFET increases total cost.

FSL4110LR has a 1 kV avalanche rugged SenseFET and a PWM controller in order to design optimized auxiliary power supply stage in industrial equipments.

### 2. Introduction

The FSL4110LR is an integrated Pulse Width Modulation (PWM) controller and 1000 V avalanche rugged SenseFET specifically designed for high input voltage offline Switching Mode Power Supplies (SMPS) with minimal external components. V<sub>CC</sub> can be supplied through integrated high-voltage power regulator without auxiliary bias winding.

The integrated PWM controller includes a fixed-frequency oscillator, Under-Voltage Lockout (UVLO), Leading-Edge Blanking (LEB), optimized gate driver, soft-start, temperature-compensated precise current sources for loop-compensation, and variable protection circuitry.

Compared with a discrete MOSFET and PWM controller solution, the FSL4110LR can reduce total cost, component count, PCB size, and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform for cost-effective design of a flyback converter.

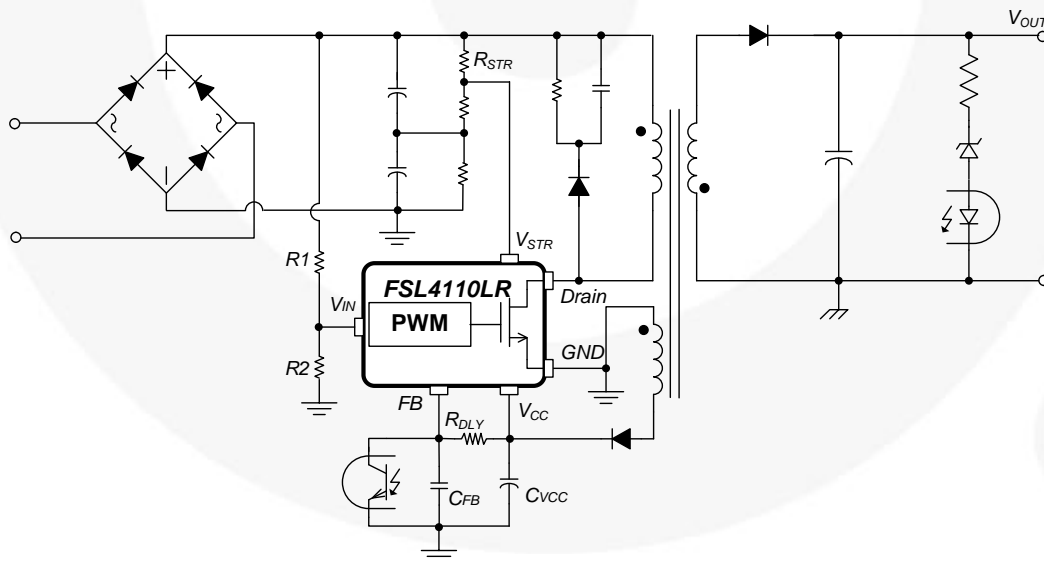


Figure 1. Typical Application

## 3. Functional Description

### 3.1. Startup and High-Voltage Regulator

During startup, an internal high-voltage current source ( $I_{CH}$ ) of the high-voltage regulator ( $HV_{REG}$ ) supplies the internal bias current ( $I_{START}$ ) and charges the external capacitor ( $C_{VCC}$ ) connected to  $V_{CC}$  pin, as shown in Figure 2. This internal high-voltage current source is enabled until  $V_{CC}$  reaches  $V_{START}$  (12 V). During steady-state operation, this internal high-voltage regulator ( $HV_{REG}$ ) maintains the  $V_{CC}$  with 10 V and provides operating switching current ( $I_{OPS}$ ) for all internal circuits. Therefore, FSL4110LR needs no external bias circuit. The high-voltage regulator is disabled when  $V_{CC}$  supplied by the external bias is higher than 10 V. However in the case of self-biasing, power consumption is increased.

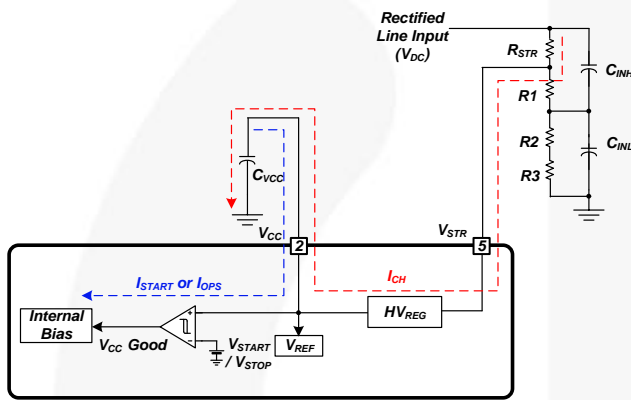


Figure 2. Startup and  $HV_{REG}$  Block

### 3.2. Feedback Control

FSL4110LR employs current-mode control scheme. An opto-coupler (such as FOD817) and shunt regulator (such as KA431) in secondary-side are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across  $R_{SENSE}$  resistor makes it possible to control the switching duty cycle. When the input voltage is increased or the output load is decreased, reference input voltage of shunt regulator is increased. If this voltage exceeds internal reference voltage of shunt regulator, optodiode's current of the opto-coupler increases, pulling down the feedback voltage and reducing drain current.

#### 3.2.1. Pulse-by-Pulse Current Limit

Because current-mode control is employed, the peak current flowing through the SenseFET is limited by the inverting input of PWM comparator, as shown in Figure 3. Assuming that 100  $\mu$ A current source ( $I_{FB}$ ) flows only through the internal resistors ( $3R + R = 24$  k $\Omega$ ), the cathode voltage of diode D2 is about 2.4 V. Since D1 is blocked when feedback voltage ( $V_{FB}$ ) exceeds 2.4 V, the maximum voltage of the cathode of D2 is clamped at this voltage. Therefore, the peak value of the current of the SenseFET is limited at:

$$\frac{2.4V}{R_{SENSE}} \times \text{Sense Ratio} \quad (1)$$

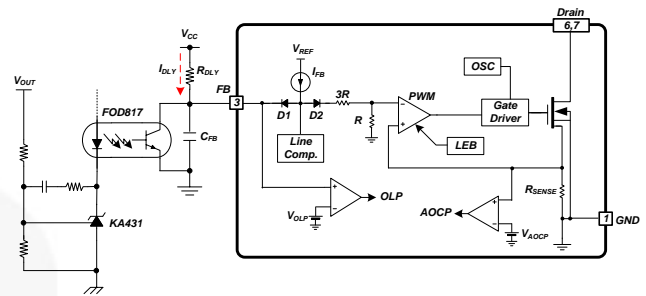


Figure 3. Pulse-Width Modulation (PWM) Circuit

#### 3.2.2. Leading-Edge Blanking (LEB)

At the instant, the internal SenseFET is turned on, a high-current spike usually occurs through the SenseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the  $R_{SENSE}$  resistor leads to incorrect feedback operation in the current-mode PWM control. To counter this effect, FSL4110LR employs a leading-edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for  $t_{LEB}$  (250 ns) after the SenseFET is turned on.

### 3.3. Protection Circuits

The protective functions include Overload Protection (OLP), Over-Voltage Protection (OVP), Under-Voltage Lockout (UVLO), Abnormal Over-Current Protection (AOCP), and Thermal Shutdown (TSD). All of the protections operate in auto-restart mode as shown in Figure 4. Since these protection circuits are fully integrated inside the IC without external components, reliability is improved without increasing cost and PCB space. If a fault condition occurs, switching is terminated and the SenseFET remains off. At the same time, internal protection timing control is activated to decrease power consumption and stress on passive and active components during auto-restart. When internal protection timing control is activated,  $V_{CC}$  is regulated with 10 V through the internal high-voltage regulator while switching is terminated. This internal protection timing control continues until restart time (1.6 s) duration is finished. After counting to 1.6 s, the internal high-voltage regulator is disabled and  $V_{CC}$  is decreased. When  $V_{CC}$  reaches the UVLO stop voltage,  $V_{STOP}$  (8 V), the protection is reset and the internal high-voltage current source charges the  $V_{CC}$  capacitor via the high voltage startup pin ( $V_{STR}$ ) again. When  $V_{CC}$  reaches the UVLO start voltage,  $V_{START}$  (12 V), the FSL4110LR resumes normal operation. In this manner, auto-restart function can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated.

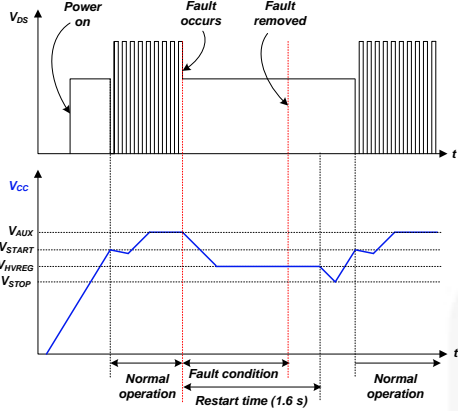


Figure 4. Auto-Restart Protection Waveforms

3.3.1. Overload Protection (OLP)

Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in normal operation, the overload protection circuit can be triggered during load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current-limit capability, the maximum peak current through the SenseFET is limited. If the output consumes more than this maximum power, the output voltage decreases below the set voltage. This reduces the current through the opto-diode, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage ( $V_{FB}$ ). If  $V_{FB}$  exceeds 2.4 V, internal diode D1 is blocked and the current ( $I_{DLY}$ ) by  $R_{DLY}$  starts to charge  $C_{FB}$ . If feedback voltage reaches 4.4 V, internal fixed delay time ( $t_{DELAY}$ ) starts counting. If feedback voltage maintains over 4.4 V after  $t_{DELAY}$  (100 ms), the switching operation is terminated (see Figure 5). The internal OLP circuit is shown in Figure 6.

Recommend the  $R_{DLY}$  value does not exceed 5 MΩ in self-biasing.

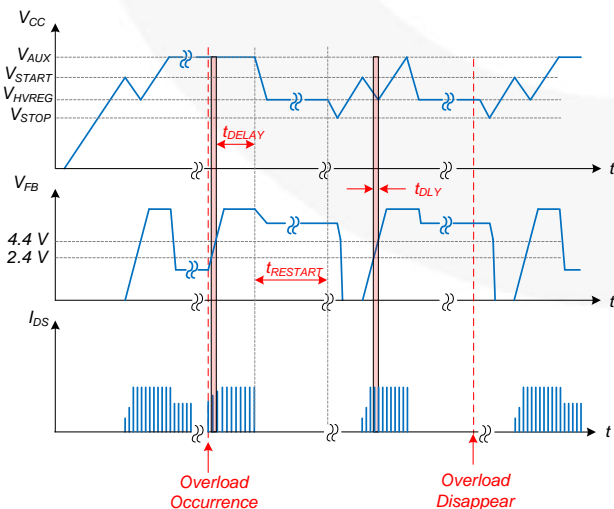


Figure 5. OLP Waveforms

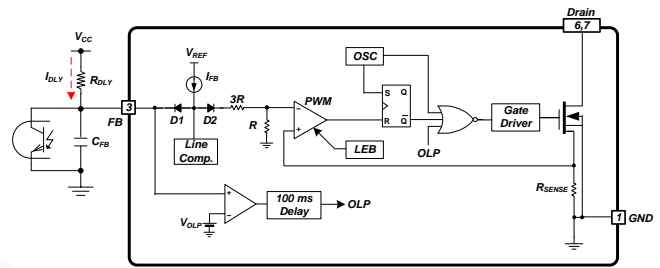


Figure 6. OLP Circuit

3.3.2. Abnormal Over-Current Protection (AOCP)

When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SenseFET during the minimum turn-on time. Overload protection is not enough to protect the FSL4110LR in that abnormal case (see Figure 7); since severe current stress is imposed on the SenseFET until OLP is triggered. The internal AOCP circuit is shown in Figure 8. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing-resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the high signal is applied to input of the NOR gate, resulting in the shutdown of the SMPS.

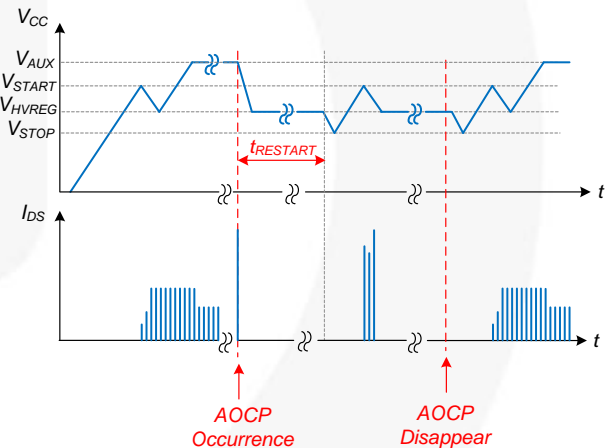


Figure 7. AOCP Waveforms

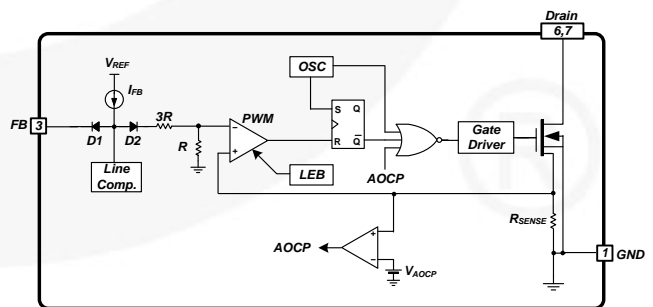


Figure 8. AOCP Circuit

3.3.3. Over-Voltage Protection (OVP)

If the secondary-side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes almost

zero. Then  $V_{FB}$  climbs up in a similar manner to the overload situation, forcing the preset maximum drain current to flow until the overload protection is triggered. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection is triggered, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In general, the  $V_{CC}$  is proportional to the output voltage when the bias-winding is used and the FSL4110LR uses  $V_{CC}$  instead of directly monitoring the output voltage. If  $V_{CC}$  exceeds 24.5 V, an OVP circuit is triggered, resulting in the termination of the switching operation. To avoid undesired activation of OVP during normal operation,  $V_{CC}$  should be designed to be below 24.5 V in the normal conditions. The internal OVP circuit is shown in Figure 9.

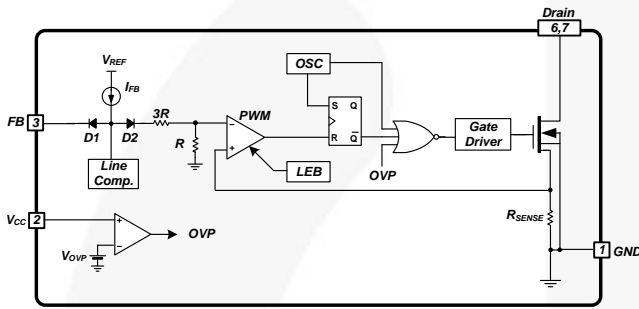


Figure 9. OVP Circuit

3.3.4. Thermal Shutdown (TSD)

The SenseFET and control IC integrated on the same package makes it easier to detect the temperature of the SenseFET. When the junction temperature exceeds 140°C, thermal shutdown is activated. The FSL4110LR is restarted when the temperature decreases by 60°C within  $t_{RESTART}$  (1.6 s).

3.3.5. Line Over-Voltage Protection (LOVP)

If the line input voltage is increased to an undesirable level, high line input voltage creates high-voltage stress on the entire system. To protect the SMPS from this abnormal condition, LOVP is included. It is comprised of detecting  $V_{IN}$  voltage by using divided resistors. When voltage of  $V_{IN}$  is higher than 2.0 V, this condition is recognized as an abnormal error and PWM switching shuts down until voltage of  $V_{IN}$  decreases to around 1.9 V within  $t_{RESTART}$  (see Figure 10). The LOVP circuit is shown in Figure 11

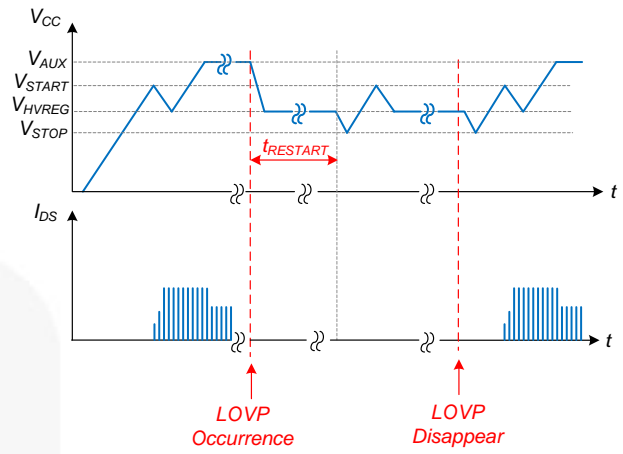


Figure 10. LOVP Waveforms

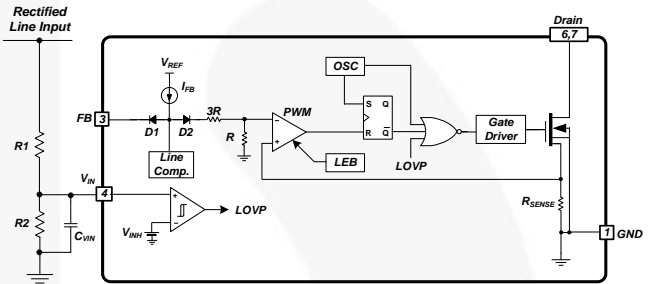


Figure 11. LOVP Circuit

3.4. Oscillator Block

The oscillator frequency is set internally and the FSL4110LR has a random frequency fluctuation function as shown in Figure 12. Fluctuation of the switching frequency can reduce EMI by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. The range of frequency variation is fixed internally; however, its selection is randomly chosen by the combination of an external feedback voltage and an internal free-running oscillator. This randomly chosen switching frequency effectively spreads the EMI noise near switching frequency and allows the use of a cost-effective inductor instead of an AC input line filter to satisfy world-wide EMI requirements.

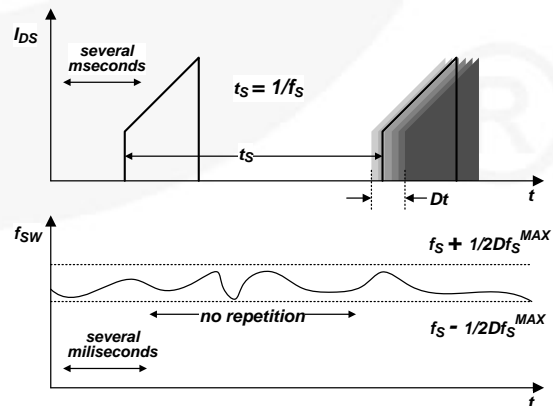


Figure 12. Frequency Fluctuation Waveform

### 3.5. Soft-Start

The internal soft-start circuit slowly increases the SenseFET current after it starts. The typical soft-start time is 20 ms, as shown in Figure 13, where progressive increments of the SenseFET current are allowed during startup. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is gradually increased to smoothly establish the required output voltage. Soft-start also helps to prevent transformer saturation and reduces stress on the secondary diode.

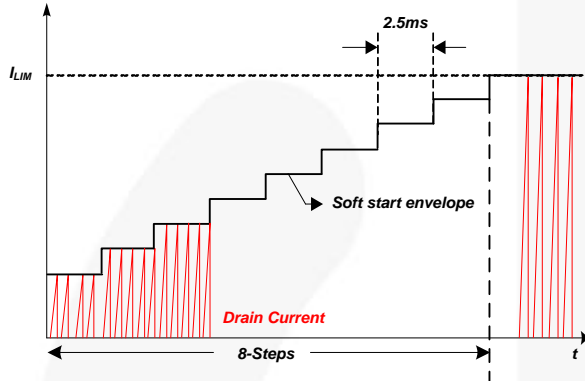


Figure 13. Internal Soft-Start

### 3.6. Burst Mode Operation

To minimize power dissipation in standby mode, the FSL4110LR enters burst mode. As the load decreases, the feedback voltage decreases. The device automatically enters burst mode when the feedback voltage drops below  $V_{BURL}$  (400 mV), as shown in Figure 14. At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes  $V_{BURH}$  (500 mV), switching resumes. Feedback voltage then falls and the process repeats. Burst Mode alternately enables and disables switching of the SenseFET, reducing switching loss in standby mode. Additionally to reduce the audible noise soft-burst is implemented.

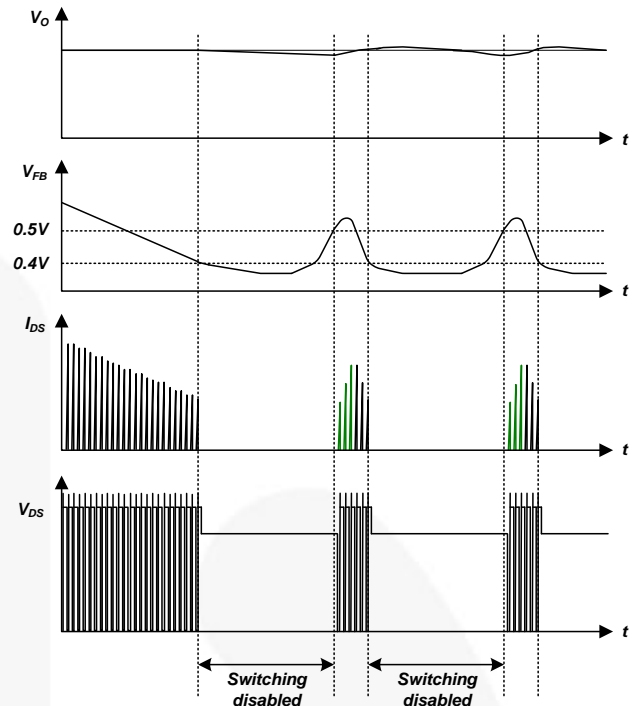


Figure 14. Burst Mode Operation

### 3.7. Line Compensation

All of switching devices have their own inherent propagation delays. This propagation delay will cause a current limit delay defined as  $t_{CLD}$ . Because there is a current limit delay,  $t_{CLD}$ , there is a difference in the current peak between low and high input voltage. The variance in the current peak is related to the difference between the input voltages, a wider gap in input voltage results in a greater variance of the current peak.

In order to have a constant current peak regardless of the input voltage; line compensation is required. FSL4110LR has line compensation, the real peak value of high input voltage is similar to that of low input voltage.  $t_{CLD}$  effect could be neglected as showed Figure 15.

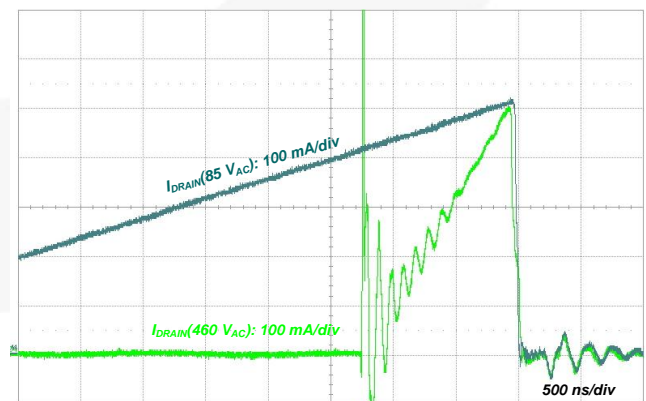


Figure 15.  $I_{LIMIT}$  Waveforms (85  $V_{AC}$  vs. 460  $V_{AC}$ )

## 4. Design Example

The following is a design example for 6 W flyback converter accompanying 85 V<sub>AC</sub> ~ 460 V<sub>AC</sub> input voltage for e-metering system.

### 4.1. Determine System Specifications

1. Define the system specifications				
Minimum Line voltage ( $V_{line}^{min}$ )	85 V.rms			
Maximum Line voltage ( $V_{line}^{max}$ )	460 V.rms			
Line frequency ( $f_L$ )	60 Hz			
	$V_{O(n)}$	$I_{O(n)}$	$P_{O(n)}$	$K_{L(n)}$
1st output for feedback	20 V	0.30 A	6 W	100 %
Full load output power ( $P_O$ ) =	6.0 W			
Estimated efficiency ( $\eta$ )	80 %			
Full load input power ( $P_{in}$ ) =	7.5 W			

Figure 16. System Specification

- Output Power ( $P_O$ ) = 6.0 W (20 V / 0.3 A)
- V<sub>AC</sub> input range = 85 to 460 V<sub>AC</sub>
- Line frequency ( $f_L$ ) = 60 Hz
- Estimated Efficiency ( $\eta$ ) > 80%.

Estimated efficiency is required to estimate the power conversion efficiency to calculate the maximum input power. If no reference data is available, set  $\eta = 0.7\sim 0.75$  for low voltage output applications and  $\eta = 0.8\sim 0.85$  for high voltage output applications.

For multiple output SMPS, the load occupying factor for each output is defined as:

$$K_{L(n)} = \frac{P_{O(n)}}{P_O} \quad (2)$$

where  $P_{O(n)}$  is the maximum output power for the n-th output. For single output SMPS,  $K_{L(1)}=1$ .

This application is single output, therefore  $K_{L(n)}$  value is 1.

### 4.2. Determine DC Link Capacitor ( $C_{DC}$ ), DC Link Voltage Range and Startup Resistor ( $R_{STR}$ )

2. Determine DC link capacitor, DC link voltage range & startup resistor ( $R_{STR}$ )	
DC link capacitor ( $C_{DC}$ )	22 $\mu$ F
Bulk capacitor charging duty ratio ( $D_{CH}$ )	0.2
Minimum DC link voltage ( $V_{DC}^{min}$ ) =	100 V
Maximum DC link voltage ( $V_{DC}^{max}$ ) =	651 V
Startup charging current ( $I_{CH}$ )	1 mA
Recommended startup resistor ( $R_{STR}$ ) =	88 K $\Omega$
Determine startup resistor ( $R_{STR}$ )	100 K $\Omega$
Power loss in startup resistor ( $P_{RSTR}$ ) =	400.0 mW

Figure 17. Determination of  $C_{DC}$  and  $R_{STR}$

It is typical to select the DC link capacitor as 2~3  $\mu$ F per watt of input power for the universal input range (85~460 V<sub>AC</sub>) and 1  $\mu$ F per watt of input power for the European input range (195~460 V<sub>AC</sub>). Figure 18 shows the corrected input voltage waveform. The blue line shows ripple voltage on the DC link capacitor and the minimum

and maximum voltage on the DC link capacitor are expressed in equations (3) and (4).

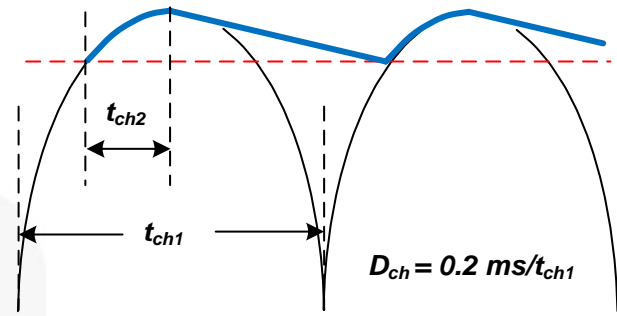


Figure 18. Bridge Rectifier and Bulk Capacitor Voltage Waveforms

$$V_{DC}^{min} = \sqrt{2 \times (V_{line}^{min})^2 - \frac{(P_O)/\eta \times (1-D_{ch})}{C_{DC} \times f_L}} \quad (3)$$

$$= \sqrt{2 \times (85V_{AC})^2 - \frac{6W/0.8 \times (1-0.2)}{22\mu F \times 60Hz}}$$

$$= 100V$$

$$V_{DC}^{max} = \sqrt{2} \times V_{line}^{max} = \sqrt{2} \times 460V = 651V \quad (4)$$

where,  $D_{ch}$  is DC link capacitor charging duty ratio as shown in Figure 18, which is typically about 0.2.

Output power is 6 W, so the  $C_{DC}$  capacitor is 12  $\mu$ F ~ 18  $\mu$ F. Select the nearest standard value of 22  $\mu$ F for  $C_{DC}$  and substitute it above. Therefore; from equation (3) and (4), the  $V_{DC}^{min}$  is 100 V and  $V_{DC}^{max}$  is 651 V.

High input voltage applications need a high-voltage rated bulk capacitor, but it increases size and price. Series-connected bulk capacitors with relatively low-voltage rating can be a solution. The case of series-connected capacitors needs a balancing resistor to achieve good voltage equalization. Small resistance can bring relatively large stand-by power consumption at light-load condition. To avoid this situation, a several M $\Omega$  resistor is recommended. HV<sub>REG</sub> is supplied from the line voltage through the balancing resistor. If HV<sub>REG</sub> is supplied from the center point of series-connected bulk capacitor, the voltage unbalance of bulk capacitors may happen, and startup time may be too long when line voltage is low. So HV<sub>REG</sub> is recommended to be supplied as shown in Figure 19 between  $R_{STR}$  and R1. Startup charging current ( $I_{CH}$ ) is supplied from  $R_{STR}$  and R1. But  $I_{CH2}$  which is supplied from R1 is very smaller than  $I_{CH1}$  which is supplied from  $R_{STR}$ , so  $I_{CH1}$  is assumed that it can be similar  $I_{CH}$ .  $I_{CH}$  should be over 1 mA to start FSL4110LR.



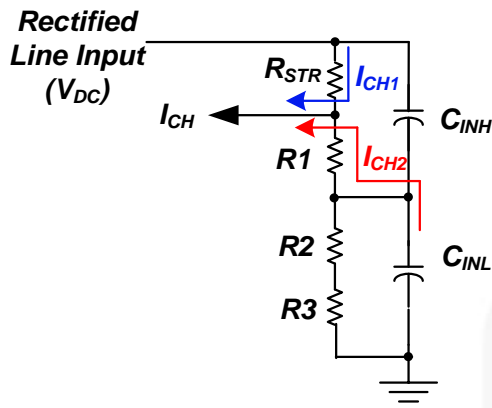


Figure 19. Balancing Resistors

The startup resistor ( $R_{STR}$ ) can be calculated by equation (5).

$$R_{STR} \leq \frac{V_{DC}^{min} - V_{START}}{I_{CH}} = \frac{100V - 12V}{1mA} = 88k\Omega \quad (5)$$

where,  $R_{STR} + R1 = R2 + R3$ ,  $I_{CH} = 1 \text{ mA}$

Choose 100 k $\Omega$  for  $R_{STR}$  in this application notes.

### 4.3. Determine Reflected Output Voltage ( $V_{RO}$ ), Maximum Duty ( $D^{MAX}$ ) & Turn Ratio

3. Determine Maximum duty ratio (Dmax)		
Output voltage reflected to primary ( $V_{RO}$ )	80 V	
Maximum duty ratio at full loading ( $D_{max}$ )	0.33	--->DCM operation
Max nominal MOSFET voltage ( $V_{ds}^{nom}$ ) =	731 V	

Figure 20. Determination of Max. Duty Ratio

A Flyback converter has two kinds of operation modes; Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). CCM and DCM have their own advantages and disadvantages, respectively. In general, DCM provides better switching conditions for the rectifier diodes, since the diodes are operating at zero current just before becoming reverse biased. The transformer size can be reduced using DCM because the average energy storage is low compared to CCM. However, DCM inherently causes high RMS current, which increases the conduction loss of the MOSFET and the current stress on the output capacitors. Therefore DCM is usually recommended for high voltage and low current output applications such as smart metering power. So  $D_{max}$  is selected 0.33, which is DCM operation.

When the SenseFET in the FSL4110LR is turned off, the input voltage ( $V_{DC}$ ) together with the output voltage reflected to the primary ( $V_{RO}$ ) are imposed on the MOSFET, as shown in Figure 21. After determining  $D_{max}$ ,  $V_{RO}$  and the maximum nominal MOSFET voltage ( $V_{ds}^{nom}$ ) are obtained as:

$$V_{ds}^{nom} = V_{DC}^{max} + V_{RO} = 651V + 80V = 731V \quad (6)$$

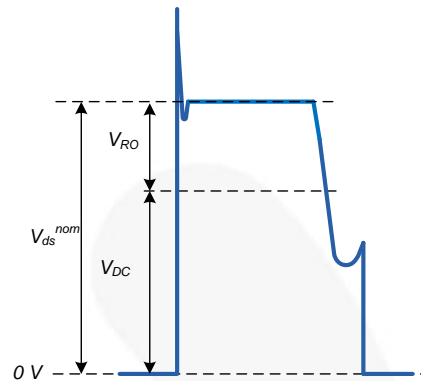
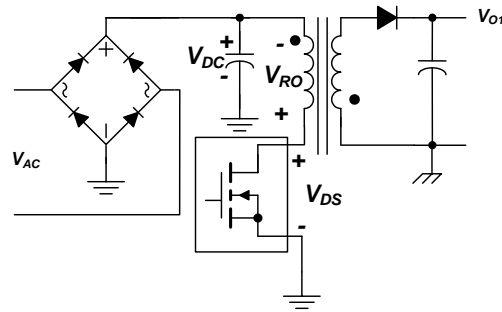


Figure 21. Output Voltage Reflected to the Primary

$V_{ds}^{nom}$  would be 65~75% of the MOSFET voltage rating considering the voltage spike caused by the leakage inductance.

### 4.4. Determine Transformer Primary-Side Inductance ( $L_m$ ) & Choose Current Limit

4. Determine transformer primary inductance ( $L_m$ )			
Switching frequency of FPS ( $f_s$ )	50 kHz		
Ripple factor ( $K_{RF}$ )	1	--->OK	
Primary side inductance ( $L_m$ ) =	1438 $\mu$ H		
Maximum peak drain current ( $I_{ds}^{peak}$ ) =	0.46 A		
RMS drain current ( $I_{ds}^{rms}$ ) =	0.15 A		

5. Choose the proper FPS considering the input power and current limit			
Typical current limit of FPS ( $I_{LM}$ )	0.52 A		
Minimum $I_{LM}$ considering tolerance of 12%	0.46 A	>	0.46 A
		--->OK	

Figure 22. Determination of Transformer Primary-Side Inductance & Current Limit

The operation changes between CCM and DCM as the load condition and input voltage vary. For both operation modes, the worst case in designing the inductance of the transformer primary side ( $L_m$ ) is full load and minimum input voltage condition. Therefore,  $L_m$  is obtained in this condition as:

$$L_m = \frac{(V_{DC}^{min} \times D_{max})^2}{2 \times P_{in} \times f_s \times K_{RF}} = \frac{(100V \times 0.33)^2}{2 \times 7.5W \times 50kHz \times 1} \approx 1.4mH \quad (7)$$

where,  $f_s$  is the switching frequency and  $K_{RF}$  is the ripple factor in full load and minimum input voltage condition.  $K_{RF} = 1$ .

$K_{RF}$  is defined as shown in Figure 23. For DCM operation,  $K_{RF} = 1$  and for CCM operation  $K_{RF} < 1$ . The ripple factor is

closely related with the transformer size and the RMS value of the MOSFET current. Even though the conduction loss in the MOSFET can be reduced through reducing the ripple factor, too small a ripple factor forces an increase in transformer size. When designing the flyback converter to operate in CCM, it is reasonable to set  $K_{RF} = 0.25 \sim 0.5$  for the universal input range and  $K_{RF} = 0.4 \sim 0.8$  for the European input range.

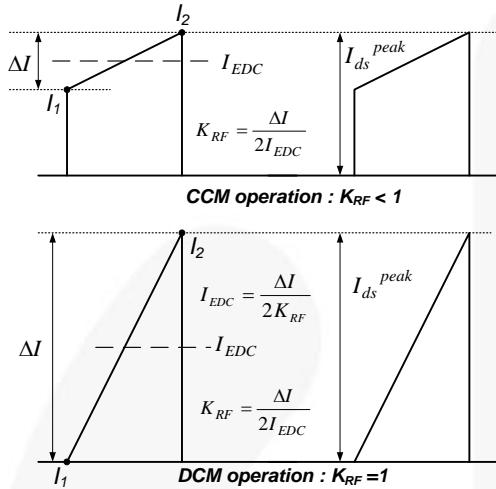


Figure 23. MOSFET Drain Current and  $K_{RF}$

Once  $L_m$  is determined, the maximum peak current and RMS current of the MOSFET in normal operation are obtained as;

$$I_{ds}^{peak} = \sqrt{\frac{2 \times P_{IN}}{L_m \times f_s}} = \sqrt{\frac{2 \times 7.5W}{1.4mH \times 50kHz}} \quad (8)$$

$$\cong 0.46A$$

With the resulting maximum peak drain current of the SenseFET ( $I_{ds}^{peak}$ ) from equation (8). The pulse-by-pulse current limit level ( $I_{LIM}$ ) is higher than  $I_{ds}^{peak}$ . Since FSL4110LR has  $\pm 12\%$  tolerance of  $I_{LIM}$ . Therefore  $I_{ds}^{peak}$  should be lower than 88% of  $I_{LIM}$ , which is 0.46 A.

And rms current of drain can be obtained by,

$$I_{ds}^{rms} = \sqrt{3 \times (I_{EDC})^2 + \left(\frac{\Delta I}{2}\right)^2} \times \frac{D_{MAX}}{3}$$

$$\cong \sqrt{3 \times (0.228)^2 + \left(\frac{0.457}{2}\right)^2} \times \frac{0.33}{3}$$

$$\cong 0.15A \quad (9)$$

$$\text{where, } I_{EDC} = \frac{\Delta I}{2 \times K_{RF}} \cong 0.228$$

$$\Delta I = \frac{V_{DC}^{min} \times D_{max}}{L_m \times f_s} \cong 0.457$$

## 4.5. Determine Transformer Core Size ( $A_e$ ) and Minimum Primary-Side Turns ( $N_p^{min}$ )

### 6. Determine the proper core and the minimum primary turns

Saturation flux density ( $B_{sat}$ )	0.35 T
Cross sectional area of core ( $A_e$ )	22.8 mm <sup>2</sup>
Minimum primary turns ( $N_p^{min}$ )=	105.0 T

Figure 24. Determination of Transformer Core Size & Minimum Primary-Side Turns

Choose EPC17 core in this application notes. With the chosen core, the minimum number of turns for the transformer primary side to avoid the core saturation is given by:

$$N_p^{min} = \frac{L_m \times I_{LIM} \times 1.12}{B_{sat} \times A_e} \times 10^6 \quad (10)$$

$$\cong \frac{1.438mH \times 0.52A \times 1.12}{0.35T \times 22.8mm^2} \times 10^6 \cong 105 Turns$$

where  $B_{max}$  is the saturation magnetic flux density,  $A_e$  is the cross-sectional of the core.

Figure 25 shows the typical characteristics of ferrite core from TDK (PC40). Since the saturation flux density ( $B_{sat}$ ) decreases as the temperature goes high, the high temperature characteristics should be considered. If there is no reference data, use  $B_{sat} = 0.3 \sim 0.35$  T. Since the MOSFET drain current exceeds  $I_{ds}^{peak}$  and reaches  $I_{LIM}$  in a transition or fault condition,  $I_{LIM}$  is used in equation (8) instead of  $I_{ds}^{peak}$  to prevent core saturation during transition.

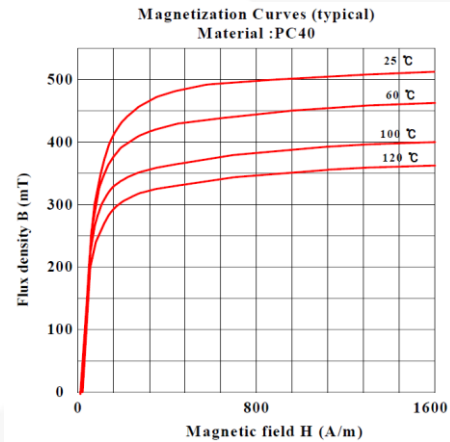


Figure 25. Typical B-H Characteristics of Ferrite Core (TDK/PC40)

## 4.6. Determine Secondary-Side Turns ( $N_s$ ), $V_{CC}$ Winding Turns ( $N_A$ )

### 7. Determine the number of turns for each output

	$V_{(in)}$	$V_{F(in)}$		# of turns
Vcc (Use Vcc start voltage)	14 V	1.2 V	20.0 $\geq$	20 T
1st output for feedback	20 V	0.5 V	27 $\geq$	27 T
VF : Forward voltage drop of rectifier diode			Primary turns ( $N_p$ )=	105 T
			→enough turns	

Figure 26. Determination of Number of Turns for each Output

First, determine the turns ratio (n) between the primary side and the feedback controlled secondary side as a reference.

$$n = \frac{N_P}{N_{S1}} = \frac{V_{RO}}{V_{O1} + V_{F1}} \quad (11)$$

where  $N_P$  and  $N_{S1}$  are the number of turns for primary side and reference output, respectively,  $V_{O1}$  is the output voltage and  $V_{F1}$  is the diode forward voltage drop of the reference output.

Then, determine the proper integer for  $N_{S1}$  so that the resulting  $N_P$  is larger than  $N_P^{\min}$  obtained from equation (10).

The number of turns for output and  $V_{CC}$  are determined as

$$N_{S1} = \frac{N_P \times (V_{O1} + V_{F1})}{V_{RO}} = \frac{105 \times (20V + 0.5V)}{80V} \cong 27 \text{ Turns} \quad (12)$$

$$N_A = \frac{N_{S1} \times (V_{CC} + V_{Fa})}{V_{O1} + V_{F1}} = \frac{27 \times (14V + 1.2V)}{20V + 0.5V} \cong 20 \text{ Turns} \quad (13)$$

where,  $V_{Fa}$  is the forward voltage in the  $V_{CC}$  diode,  $V_{F1}$  is the forward voltage in the secondary-side diode.

$V_{CC}$  is the nominal value of the supply voltage of the FSL4110LR. Since  $V_{CC}$  increases as the output load increases, it is proper to set  $V_{CC}$  as 14 V to avoid the over voltage protection condition during normal operation.

## 4.7. Choose the Rectifier Diode in the Secondary-Side

### 9. Choose the rectifier diode in the secondary side

	$V_{D(n)}$	$I_{D(n)}^{rms}$
Vcc diode	138 V	0.10 A
1st output diode	187 V	0.84 A

Figure 27. Choose the Rectifier Diode in the Secondary-Side

The maximum reverse voltage and the rms current of the rectifier diode of the output are obtained as;

$$V_D = V_{O1} + \frac{V_{DC}^{\max} \times (V_{O1} + V_{F1})}{V_{RO}} \quad (14)$$

$$= 20V + \frac{651V \times (20V + 0.5V)}{80V} \cong 187V$$

$$I_D^{rms} = I_{ds}^{rms} \times \sqrt{\frac{1 - D_{\max}}{D_{\max}}} \times \frac{V_{RO} \times K_{L(1)}}{V_{O1} + V_{F1}} \quad (15)$$

$$= 0.15A \times \sqrt{\frac{1 - 0.33}{0.33}} \times \frac{80V \times 1}{20V + 0.5V} \cong 0.84A$$

Normally, maximum reverse voltage ( $V_{RRM}$ ) of diode is 1.3 times of  $V_D$  and average forward current of diode is 1.5 times of  $I_D^{rms}$ . But output voltage is not enough to charge output capacitor during soft-start as output capacitance and output voltage is large,  $V_{RRM}$  of diode should be use 3 times of  $V_D$ , so select EGP30J rectifier diode. (Specification of EGP30J as: the maximum reverse voltage,  $V_{RRM}$  is 600 V and average forward current,  $I_F$  is 3 A).

## 4.8. Determine Primary-Side RCD Snubber

### 11. Design RCD snubber for SenseFET (at peak load)

Primary side leakage inductance ( $L_{lk}$ )	16 $\mu$ H
Maximum Voltage of snubber capacitor ( $V_{sn}$ )	155 V
Maximum snubber capacitor voltage ripple	6 %
Power loss in snubber resistor ( $P_{sn}$ )=	0.2 W
Snubber resistor ( $R_{sn}$ )=	139.3 K $\Omega$
Snubber capacitor ( $C_{sn}$ )=	2.4 nF

Figure 28. Determination of Primary-Side RCD Snubber

When the power MOSFET is turned off, there is a high voltage spike on the drain due to the transformer leakage inductance. This excessive voltage on the MOSFET may lead to an avalanche breakdown and eventual failure of FSL4110LR. Therefore, it is necessary to use an additional network to clamp the voltage.

The RCD snubber circuit and MOSFET drain voltage waveform are shown in Figure 29 and Figure 30, respectively. The RCD snubber network absorbs the current in the leakage inductance by turning on the snubber diode ( $D_{sn}$ ) once the MOSFET drain voltage exceeds the voltage of node X as depicted in Figure 29. In the analysis of snubber network, it is assumed that the snubber capacitor is large enough that its voltage does not change significantly during one switching cycle.

The first step in designing the snubber circuit is to determine the snubber capacitor voltage at the minimum input voltage and full load condition ( $V_{sn}$ ). Once  $V_{sn}$  is determined, the power dissipated in the snubber network at the minimum input voltage and full load condition is obtained as;

$$P_{sn} = \frac{V_{sn}^2}{R_{sn}} = \frac{1}{2} L_{lk} \times (I_{ds}^{peak})^2 \times f_s \times \frac{V_{sn}}{V_{sn} - V_{RO}} \quad (16)$$

$$= 0.5 \times 20\mu H \times (0.46A)^2 \times 50kHz \times \frac{160V}{160V - 80V}$$

$$\cong 0.2W$$

$V_{sn}$  should be larger than  $V_{RO}$  and it is typical to set  $V_{sn}$  to be 2 ~ 2.5 times of  $V_{RO}$ . Too small  $V_{sn}$  results in a severe loss in the snubber network as shown in equation (16). The leakage inductance is measured at the switching frequency on the primary winding with all other windings shorted.

Then, the snubber resistor with proper rated wattage should be chosen based on the power loss. In general, ripple of the snubber capacitor voltage is 5 ~ 10%. The snubber resistance ( $R_{sn}$ ) and capacitance ( $C_{sn}$ ) are obtained as;

$$R_{sn} = \frac{V_{sn}^2}{P_{sn}} = \frac{[155V]^2}{0.2W} \cong 139.3k\Omega \quad (17)$$

$$C_{sn} = \frac{V_{sn}}{\Delta V_{sn} \times R_{sn} \times f_s} \quad (18)$$

$$= \frac{155V}{6\% \times 155V \times 139.3k\Omega \times 50kHz} \cong 2.4nF$$

To reduce the power loss from  $R_{sn}$ , the  $R_{sn}$  should be selected higher than 139.3 k $\Omega$  from equation (17); if the  $R_{sn}$

increases, the  $V_{sn}$  also increases. The  $R_{sn}$  recommended value is between 200 k $\Omega$  and 47 k $\Omega$ . Check if  $V_{ds}^{max}$  is below 800 V (80% of rated voltage of the SenseFET) as shown Figure 30. Choose 2.2 nF and 150 k $\Omega$  for  $C_{sn}$  and  $R_{sn}$  in this application note.

The voltage rating of the snubber diode should be higher than  $BV_{dss}$ . Usually, an ultra-fast diode with 1 A current rating is used for the snubber network.

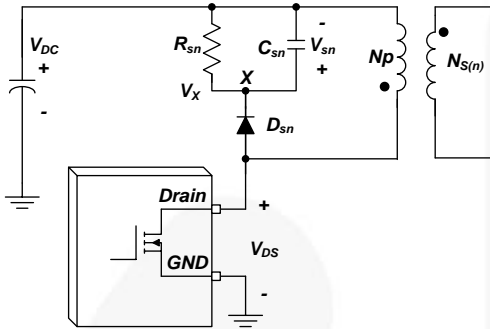


Figure 29. Primary-Side RCD Snubber Circuit

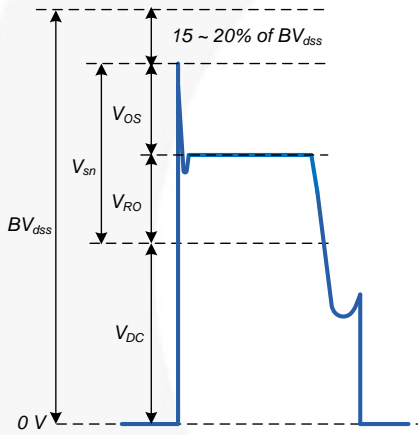


Figure 30. MOSFET Drain Voltage Waveforms

#### 4.9. Determine Secondary-Side Snubber

12. Design snubber for Output Diode (at startup)	
Ringing frequency for 2'nd diode ( $f_{RING}$ )	25 MHz
Capacitance of 2'nd diode ( $C_D$ )	75 pF
Peak Voltage of 2'nd diode	328 V
Snubber capacitor ( $C_{sns}$ ) for 2'nd diode =	225.0 pF
Inductance ( $L_{sec}$ ) at 2'nd side =	0.54 $\mu$ H
Snubber resistor ( $R_{sns}$ ) for 2'nd diode =	84.9 $\Omega$
Power loss in 2'nd snubber resistor ( $P_{sns}$ )=	0.6 W

Figure 31. Determination of Primary-Side RCD Snubber

During startup, output voltage is very low, and the Flyback converter operates at CCM mode. If the output voltage is high and output capacitor is large, voltage spike of diode of secondary-side is very large as shown in Figure 32. For reducing the voltage spike, snubber of diode in secondary-side should be used.

$C_D$  is capacitance of diode in secondary-side.  $C_{sns}$  and  $R_{sns}$  are external snubber network as Figure 33.

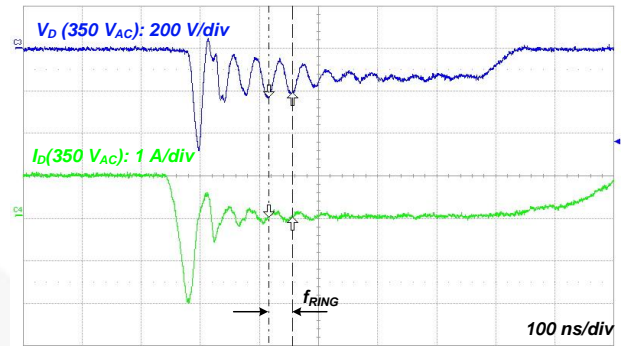


Figure 32. Secondary-Side Voltage-Spike without Snubber

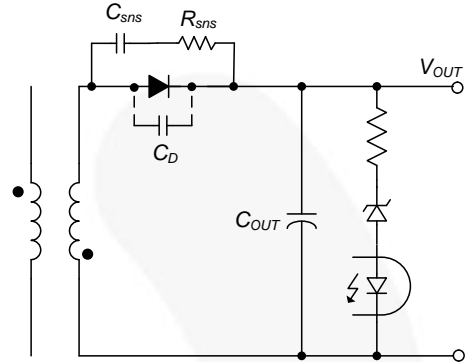


Figure 33. Secondary-Side Snubber Circuit

For design a snubber, the ringing frequency of the oscillation of the secondary-side as shown in Figure 32 should be measured and capacitance of diode in the secondary side should be checked.

$$\begin{aligned} f_{RING} &= 25\text{MHz} \\ C_D &= 75\text{pF} \end{aligned} \quad (19)$$

$C_{sns}$  which is half of  $f_{RING}$  can be obtained by

$$C_{sns} = 3 \times C_D = 3 \times 75\text{pF} = 225\text{pF} \quad (20)$$

Once  $C_{sns}$  are determined and secondary-side inductance ( $L_{sec}$ ) can be obtained by

$$L_{sec} = \frac{\left(\frac{2}{f_{RING} \times 2\pi}\right)^2}{C_D + C_{sns}} = \frac{\left(\frac{2}{(25\text{MHz} \times 2\pi)}\right)^2}{75\text{pF} + 225\text{pF}} \cong 0.54\mu\text{H} \quad (21)$$

And  $R_{sns}$  can be obtained by  $L_{sec}$  and  $C_D$ .

$$R_{sns} = \sqrt{\frac{L_{sec}}{C_D}} = \sqrt{\frac{0.54\mu\text{H}}{75\text{pF}}} \cong 84.9\Omega \quad (22)$$

$R_{sns}$  of power loss can be obtained by

$$P_{sns} = \frac{C_{sns} \times V^2 \times f_s}{2} = \frac{225\text{pF} \times (328\text{V})^2 \times 50\text{kHz}}{2} \cong 0.6\text{W} \quad (23)$$

In this application note, choose 330 pF for  $C_{sns}$  and 150  $\Omega$  for  $R_{sns}$ .

### 4.10. Determine DC Link Voltage for Line Over Voltage Protection (LOVP).

13. Line Over Voltage Protection	
Target line over AC voltage	472 Vac
Maximum DC voltage at target line over AC voltage =	667.5 V
Line over voltage threshold voltage (V <sub>INH</sub> )	2.00 V
Selected upper side resistor (R <sub>high</sub> )	9.0 MΩ
Recommended V <sub>IN</sub> pin lower side resistor (R <sub>low</sub> ) =	27.0 KΩ
Recommended minimum V <sub>IN</sub> pin filter capacitor =	1.2 nF
Maximum power loss on V <sub>IN</sub> sense resistors =	46.9 mW

Figure 34. Determination of Line Over Voltage

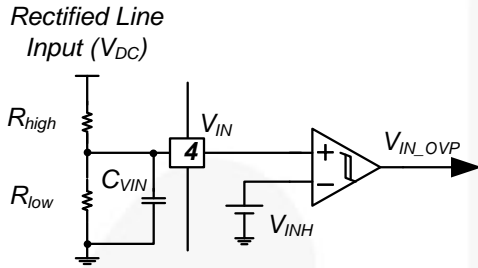


Figure 35. LOVP Circuit

Equation (24) calculates the low side resistor.

$$R_{low} = \frac{V_{INH} \times R_{high}}{V_{DC} - V_{INH}} = \frac{2V \times 9M\Omega}{667.5V - 2V} \approx 27k\Omega \quad (24)$$

The resistance of divided resistor can be adjusted as necessary. Small resistance can bring relatively large stand-by power consumption at light-load condition. To avoid this situation, a several MΩ resistor is recommended. For stable operation, a several MΩ resistor should accompany a capacitor (C<sub>VIN</sub>) with hundreds of pF capacitance between the V<sub>IN</sub> pin and GND.

### 4.11. Determine Feedback Resistors.

14. Design Feedback control loop & Determine OLP delay time	
Voltage divider resistor (R <sub>1</sub> )	33.0 KΩ
Voltage divider resistor (R <sub>2</sub> ) =	4.7 KΩ

Figure 36. Feedback Resistors

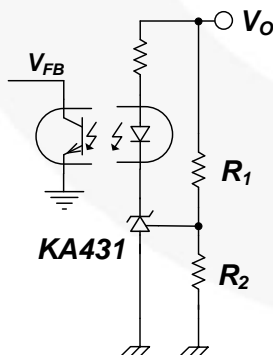


Figure 37. Feedback Circuit for Single Output

Equation (25) calculates the low side feedback resistor.

$$R_2 = \frac{R_1 \times 2.5V}{V_{O1} - 2.5V} = \frac{33k\Omega \times 2.5V}{20V - 2.5V} = 4.7k\Omega \quad (25)$$

where, reference voltage of KS431 is 2.5 V

To give a weighting factor to the feedback circuit can be applied for multi output as Figure 38.

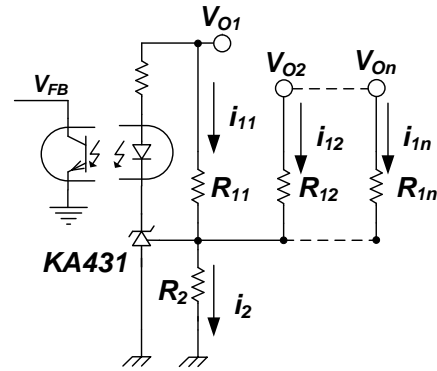


Figure 38. Weight the Feedback Circuit for Multi Output

Equation (26) calculates feedback resistors for weighting the feedback circuit.

$$i_2 = i_{11} + i_{12} + \dots + i_{1n} = (W_{11} \times i_2) + (W_{12} \times i_2) + \dots + (W_{1n} \times i_2)$$

$$W_{11} + W_{12} + \dots + W_{1n} = 1 \quad (26)$$

$$R_{1k} = \frac{V_{On} - V_{ref}}{W_{1k} \times i_2}, \quad k = 1 \dots n.$$

where, W<sub>1k</sub> is significance weight value of output.

If output condition is as follows.

- V<sub>O1</sub> = 20 V, W<sub>1</sub> = 0.1
- V<sub>O2</sub> = 5 V, W<sub>2</sub> = 0.9
- i<sub>2</sub> = 1 mA
- V<sub>ref</sub> = 2.5 V.

Feedback resistance can be obtained by

$$R_2 = \frac{V_{ref}}{i_2} = \frac{2.5V}{1mA} = 2.5k\Omega$$

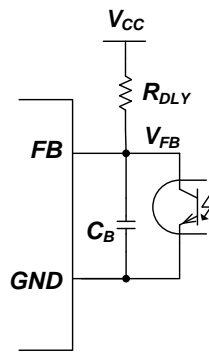
$$R_{11} = \frac{V_{O1} - V_{ref}}{W_1 \times i_2} = \frac{20V - 2.5V}{0.1 \times 1mA} = 175k\Omega \quad (27)$$

$$R_{12} = \frac{V_{O2} - V_{ref}}{W_2 \times i_2} = \frac{5V - 2.5V}{0.9 \times 1mA} = 2.8k\Omega$$

### 4.12. Determine Over Load Protection (OLP) Delay Time (t<sub>OLP</sub>).

14. Design Feedback control loop & Determine OLP delay time	
Feedback pin capacitor (C <sub>B</sub> ) =	68 nF
Internal OLP delay time (t <sub>DELAY</sub> )	100 ms
OLP delay resistor (R <sub>DLY</sub> )	4.7 MΩ
Total OLP delay time =	160.5 ms

Figure 39. OLP Delay Time



**Figure 40. External Circuit for FB**

Total Overload Protection (OLP) delay time can be calculated by the following equation:

$$\begin{aligned}
 t_{OLP} &= t_{DELAY} + t_{DLY} \\
 &= 100ms - R_{DLY} \times C_{FB} \times \ln\left(1 - \frac{2}{V_{CC} - 2.4}\right) \\
 &= 100ms - 4.7M\Omega \times 68nF \times \ln\left(1 - \frac{2V}{14V - 2.4V}\right) \\
 &\cong 160.5ms
 \end{aligned}
 \tag{28}$$

## 5. Printed Circuit Board Layout

High-frequency switching current / voltage makes printed circuit board layout a very important design issue. Good PCB layout minimizes excessive EMI helps the power supply survive during surge/ESD tests.

### 5.1. Guidelines

To improve EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor  $C_{DC}$  first, then to the switching circuits. Refer to Figure 41.

The high-frequency current loop is in  $C_{DC}$  – Transformer – Drain PIN – GND PIN –  $C_{DC}$ . The area enclosed by this current loop should be as small as possible. Keep the traces (especially  $GND2 \rightarrow GND1$ ) short, direct, and wide. High-voltage traces related the drain of MOSFET and RCD snubber should be kept far away from control circuits to prevent unnecessary interference.

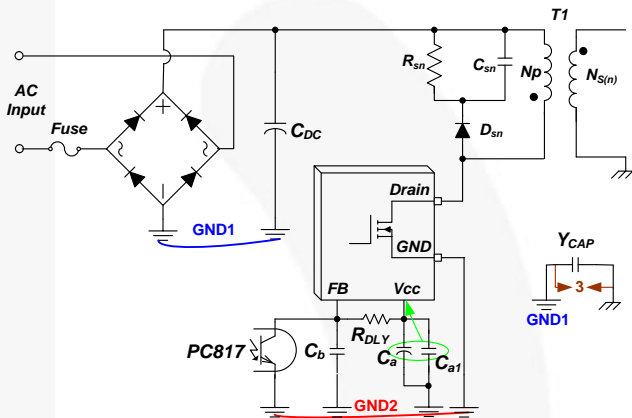
- As indicated by  $GND2$ , the ground of control circuits should be connected first, then to other circuitry.
- Place  $C_a$  and  $C_{a1}$  close to the controller for good decoupling. Especially, A ceramic capacitor ( $C_{a1}$ ) needs to be placed as close as possible between  $V_{CC}$  pin and pin 1 (GND). Recommended distance is less than 3 mm.

Two suggestions with different advantages and disadvantages for ground connections are recommended.

- $GND2 \rightarrow GND1$ : This could avoid common impedance interference for the sense signal.
- Regarding the ESD discharge path, the charges go from secondary, through the transformer stray capacitance,

to  $GND1$  first, and back to mains. Noted that control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high-frequency impedance and increase ESD immunity.

- $3$  should be a point-discharger route to bypass the static electricity energy. As shown in Figure 30, it is suggested to map out this discharge route.
- Should a Y-cap be required between the primary and the secondary, connect this Y-cap to the positive terminal of  $C_{DC}$ . If this Y-cap is connected to primary GND, it should be connected to the negative terminal of  $C_{DC}$  ( $GND1$ ) directly. Point discharge of this Y-cap helps for ESD; however, the creepage between these two pointed ends should be at least 5 mm according to safety requirements.



**Figure 41. Layout Considerations**

## 6. Typical Application Circuit

Application	Output Power	Input Voltage Range	Output Voltage / Maximum Current
E-metering	6.0 W	85~460 V <sub>AC</sub>	20 V / 0.3 A

### 6.1. Features

- Built-in Avalanche Rugged 1 kV SenseFET
- Precise Fixed Operating Frequency: 50 kHz
- V<sub>CC</sub> can be supplied from either bias-winding or self-biasing.
- Soft Burst-Mode Operation Minimizing Audible Noise
- Random Frequency Fluctuation for Low EMI
- Pulse-by-Pulse Current Limit
- Various Protection Functions: Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD) with Hysteresis. Under-Voltage Lockout (UVLO) and Line Over-Voltage Protection (LOVP) with Hysteresis.
- Built-in Internal Startup and Soft-Start Circuit
- Fixed 1.6 s Restart Time for Safe Auto-Restart Mode of All Protections

6.2. Schematic

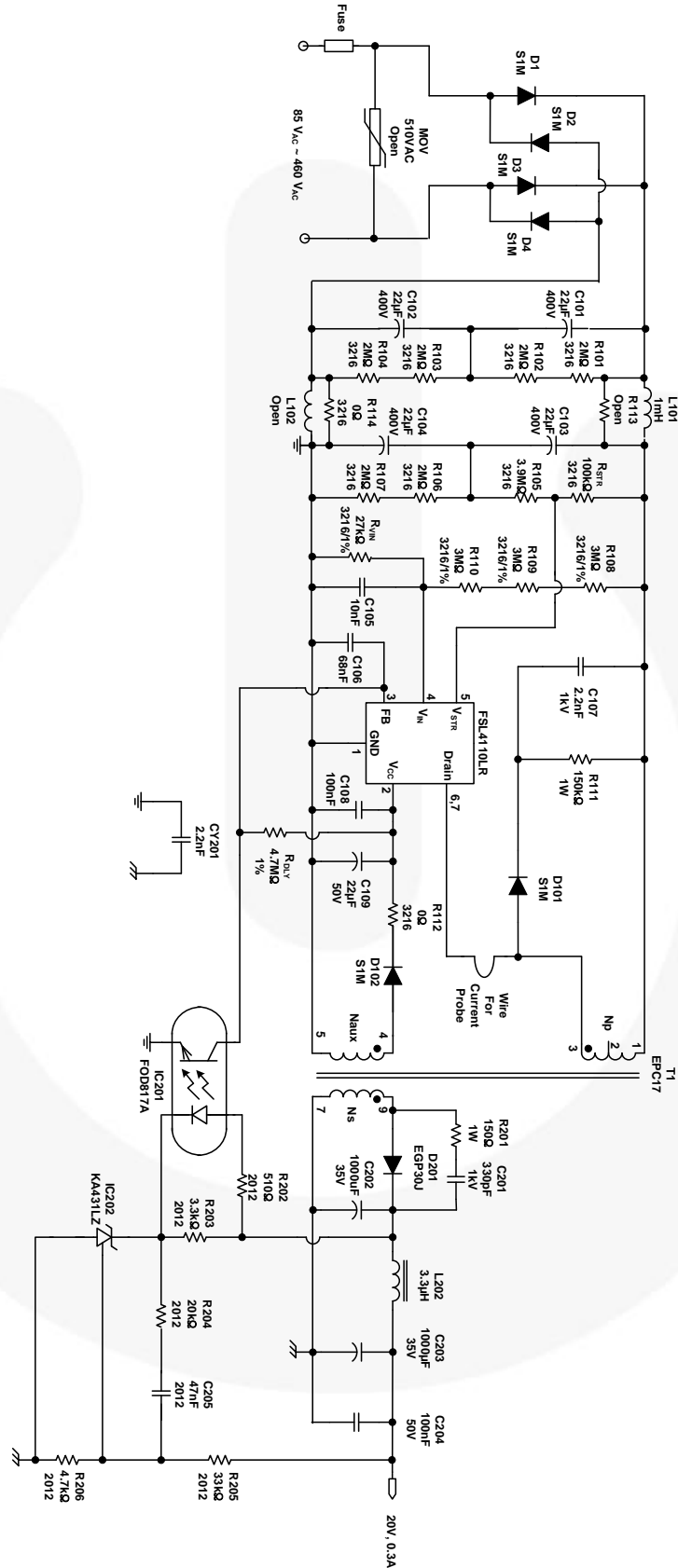


Figure 42. Schematic



**Table 1. Part List for 6 W Evaluation Board**

Item No.	Part Reference	Part Number	Qty.	Description
1	IC101	FSL4110LRN	1	7-DIP, Fairchild
2	IC201	FOD817A	1	4-DIP, Fairchild
3	IC202	KA431LZ	1	TO-92, Fairchild
4	D1, D2, D3, D4, D101, D102	S1M	6	1000 V / 1 A General Purpose Rectifiers, SMA, Fairchild
5	D202	EGP30J	1	1000 V / 3 A Rectifiers, DO-201AD, Fairchild
6	F1	SS-5-1 A	1	1 A Fuse
7	MOV	510 V <sub>RMS</sub>	1	510 V <sub>RMS</sub>
8	L101	1 mH	1	Filter Inductor, 10Φ
9	L102	Open		Open
10	L202	3.3 μH	1	Filter Inductor, 8Φ
11	T1	Lm = 1.4 mH	1	EPC17 Core
12	R101, R102, R103, R104, R106, R107	2 MΩ	4	SMD Resistor 3216
13	RSTR	100 kΩ	2	SMD Resistor 3216
14	R105	3.9 MΩ	2	SMD Resistor 3216
16	R108, R109, R110	3 MΩ	3	SMD Resistor 3216
17	RVIN	27 kΩ	1	SMD Resistor 3216 / 1%
18	R111	150 kΩ	1	Resistor 1 W
19	R112, R114	0 Ω	2	SMD Resistor 3216
20	R113	Open		Open
21	RDLY	4.7 MΩ	1	SMD Resistor 2012 / 1%
22	R201	150 Ω	1	Resistor 1 W
23	R202	510 Ω	1	SMD Resistor 2012
24	R203	3.3 kΩ	1	SMD Resistor 2012
25	R204	20 kΩ	1	SMD Resistor 2012
26	R205	33 kΩ	1	SMD Resistor 2012 / 1%
27	R206	4.7 kΩ	1	SMD Resistor 2012 / 1%
28	C101, C102, C103, C104	22 μF / 400 V	4	Electrolytic Capacitor, 105°C
29	C105	10 nF / 50 V	1	SMD Capacitor 2012
30	C106	68 nF / 50 V	1	SMD Capacitor 2012
31	C107	2.2 nF / 1 kV	1	Ceramic Capacitor
32	C108	100 nF / 50 V	1	SMD Capacitor 2012
33	C109	22 μF / 50 V	1	Electrolytic Capacitor, 105°C
34	C201	330 pF / 1 kV	1	Ceramic Capacitor
35	C202, C203	1000 μF / 35 V	2	Electrolytic Capacitor, 105°C
36	C204	100 nF / 50 V	1	SMD Capacitor 2012
37	C205	47 nF / 50 V	1	SMD Capacitor 2012
38	CY201	2.2 nF	1	Y-Capacitor

### 6.3. Transformer Specification

- Core: EPC17 (PC-40,  $A_e=22.8 \text{ mm}^2$ )
- Bobbin: 10-pin

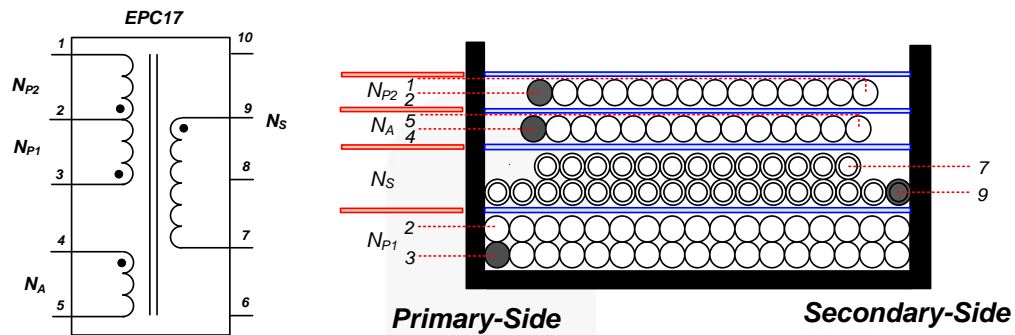


Figure 43. Transformer Specification

Table 2. Winding Specification

	Pin (S → F)	Wire	Turns	Winding Method
$N_{P1}$	3 → 2	$0.2\phi \times 1$	72 Ts	Solenoid Winding
Insulation: Polyester Tape $t = 0.025 \text{ mm}$ , 3-Layer				
$N_S$	9 → 7	$0.2\phi \times 1$ (TEX)	27 Ts	Solenoid Winding
Insulation: Polyester Tape $t = 0.025 \text{ mm}$ , 3-Layer				
$N_A$	4 → 5	$0.15\phi \times 1$	20 Ts	Solenoid Winding
Insulation: Polyester Tape $t = 0.025 \text{ mm}$ , 3-Layer				
$N_{P2}$	2 → 1	$0.2\phi \times 1$	33 Ts	Solenoid Winding
Insulation: Polyester Tape $t = 0.025 \text{ mm}$ , 3-Layer				

Table 3. Electrical Characteristics

	Pin	Specification	Remark
Inductance	1 – 3	$1.4 \text{ mH} \pm 6\%$	50 kHz, 1 V
Leakage	1 – 3	20 $\mu\text{H}$ Maximum	Short All Other Pins

### 6.4. Experimental Results

Table 4. Efficiency

	85 V <sub>AC</sub>	110 V <sub>AC</sub>	230 V <sub>AC</sub>	265 V <sub>AC</sub>	350 V <sub>AC</sub>	400 V <sub>AC</sub>	460 V <sub>AC</sub>
<b>Full-Load</b>	83.97%	84.85%	83.71%	82.78%	80.29%	78.69%	76.60%
<b>75% Load</b>	84.13%	84.82%	83.07%	82.20%	79.53%	77.61%	75.01%
<b>50% Load</b>	84.20%	84.18%	80.34%	78.87%	74.59%	71.72%	68.13%
<b>25% Load</b>	81.05%	80.71%	72.76%	70.25%	63.58%	59.52%	55.08%

Table 5. Operating Temperature

	85 V <sub>AC</sub>	460 V <sub>AC</sub>	Remark
<b>FSL4110LRN</b>	42.0°C	48.4°C	Box 2
<b>Transformer</b>	47.0°C	51.5°C	Circle 1
<b>Secondary Rectifier with Snubber</b>	41.8°C	49.0°C	Box 3

### 6.5. Experimental Waveform

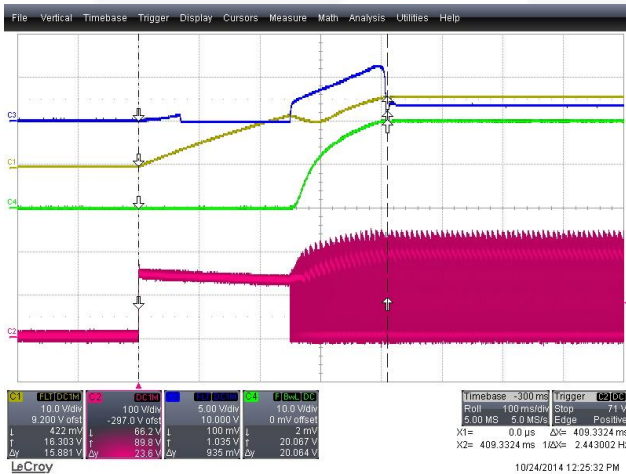


Figure 44. Startup Time = 409 ms, 85 V<sub>AC</sub>, Full-Load Condition (CH1: V<sub>CC</sub> (10 V/div), CH2: V<sub>DS</sub> (100 V/div), CH3: V<sub>FB</sub> (5V/div), CH4: V<sub>OUT</sub> (10 V/div), Time: 100 ms/div)

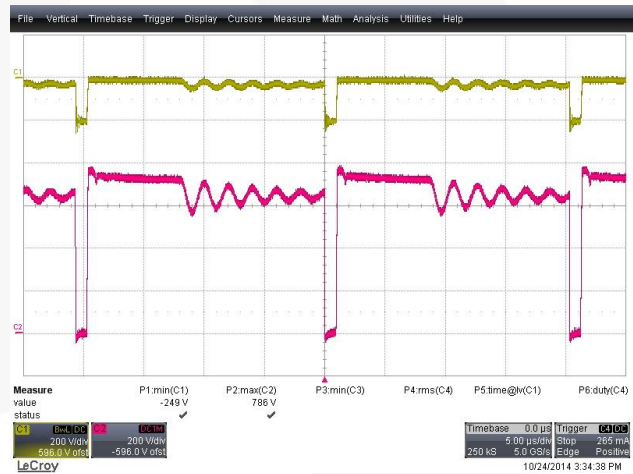
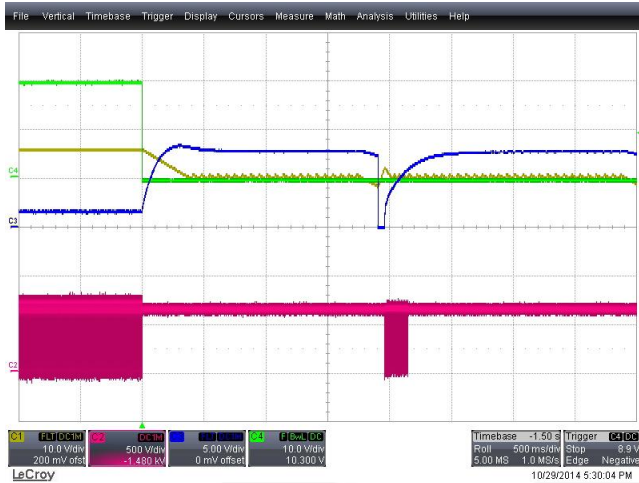
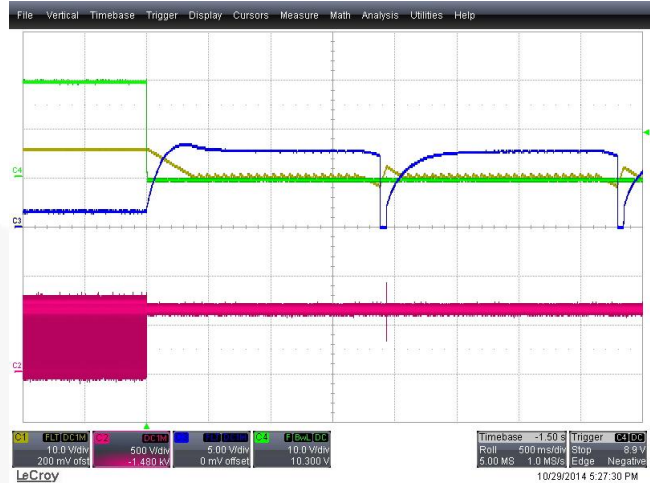


Figure 45. V<sub>DS</sub>=786 V, V<sub>DIODE</sub>=249 V, Steady-State, Full-Load Condition, 460 V<sub>AC</sub>, (CH1: V<sub>DIODE</sub> (200 V/div), CH2: V<sub>DS</sub> (200 V/div), Time: 5 μs/div)



**Figure 46. OLP Triggered, Output Short with 460 V<sub>AC</sub>, Full-Load, (CH1: V<sub>CC</sub> (10 V/div), CH2: V<sub>DS</sub> (500 V/div), CH3: V<sub>FB</sub> (5 V/div), CH4: V<sub>OUT</sub> (10 V/div), Time: 500 ms/div)**



**Figure 47. AOCV Triggered, Output Short with 460 V<sub>AC</sub>, Full-Load, (CH1: V<sub>CC</sub> (10 V/div), CH2: V<sub>DS</sub> (500 V/div), CH3: V<sub>FB</sub> (5 V/div), CH4: V<sub>OUT</sub> (10 V/div), Time: 500 ms/div)**

## 7. References

[FSL4110LR Product Information](#)

[AN-4137 — Design Guidelines for Offline Flyback Converters Using the FPS™](#)

[AN-4147 — Design Guideline for RCD Snubber of Flyback Converters](#)

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