

ON Semiconductor

Is Now

onsemi™

To learn more about onsemi™, please visit our website at
www.onsemi.com

onsemi and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

Electrostatic Discharge Prevention-Input Protection Circuits and Handling Guide for CMOS Devices

Introduction

During the past few years, there have been significant increase in the usage of low-power CMOS devices in system designs. This has resulted in more stringent attention to handling techniques of these devices, due to their static sensitivity, than ever before.

All CMOS devices, which are composed of complementary pairs of N- and P-channel MOSFETs, are susceptible to damage by the discharge of electrostatic energy between any two pins. This sensitivity to static charge is due to the fact that gate input capacitance (5 pF typical) in parallel with an extremely high input resistance ($10^{12}\Omega$ typical) lends itself to a high input impedance and hence readily builds up the electrostatic charges, unless proper precautionary measures are taken. This voltage build-up on the gate can easily break down the thin (1000Å) gate oxide insulator beneath the gate metal. Local defects such as pinholes or lattice defects of gate oxide can substantially reduce the dielectric strength from a breakdown field of $8-10 \times 10^6 \text{V/cm}$ to $3-4 \times 10^6 \text{V/cm}$. This then becomes the limiting factor on how much voltage can be applied safely to the gates of CMOS devices.

When a higher voltage, resulting from a static discharge, is applied to the device, permanent damage like a short to substrate, V_{DD} pin, V_{SS} pin, or output can occur. Now static electricity is always present in any manufacturing environment. It is generated whenever two different materials are rubbed together. A person walking across a production floor can generate a charge of thousands of volts. A person working at a bench, sliding around on a stool or rubbing his arms on the work bench can develop a high static potential. Table 1 shows the results of work done by Speakman¹ on various static potentials developed in a common environment. The ambient relative humidity, of course, has a great effect on the amount of static charge developed, as moisture tends to provide a leakage path to ground and helps reduce the static charge accumulation.

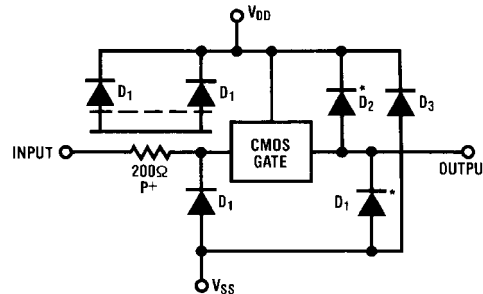
TABLE 1. Various Voltages Generated in 15%–30% Relative Humidity (after Speakman¹)

Condition	Most Common Reading (Volts)	Highest Reading (Volts)
Person walking across carpet	12,000	39,000
Person walking across vinyl floor	4,000	13,000
Person working at bench	500	3,000
16-lead DIPs in plastic box	3,500	12,000
16-lead DIPs in plastic shipping tube	500	3,000

Standard Input Protection Networks

In order to protect the gate oxide against moderate levels of electrostatic discharge, protective networks are provided on all Fairchild CMOS devices, as described below.

Figure 1 shows the standard protection circuit used on all A, B, and 74C series CMOS devices. The series resistance of 200Ω using a P⁺ diffusion helps limit the current when the input is subjected to a high-voltage zap. Associated with this resistance is a distributed diode network to V_{DD} which protects against positive transients. An additional diode to V_{SS} helps to shunt negative surges by forward conduction. Development work is currently being done at Fairchild on various other input protection schemes.



Diode Breakdown

$D_1 = 25\text{V}$

$D_2 = 60\text{V}$

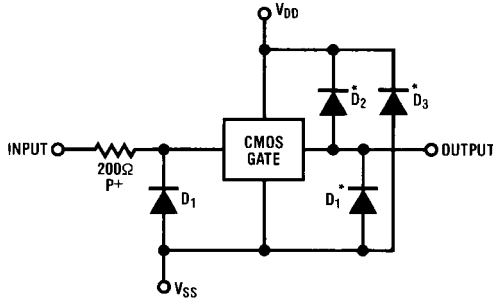
$D_3 = 100\text{V}$

*These are intrinsic diodes

FIGURE 1. Standard Input Protection Network

Other Protective Networks

Figure 2 shows the modified protective network for CD4049/4050 buffer. The input diode to V_{DD} is deleted here so that level shifting can be achieved where inputs are higher than V_{DD} .



Diode Breakdown

$D_1 = 25V$

$D_2 = 60V$

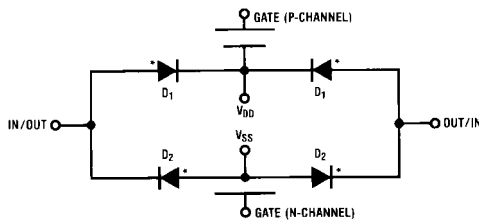
$D_3 = 100V$

*These are intrinsic diodes

FIGURE 2. Protective Network for CD4049/50 and MM74C901/2

Figure 3 shows a transmission gate with the intrinsic diode protection. No additional series resistors are used so the on resistance of the transmission gate is not affected.

All CMOS circuits from Fairchild's CD4000 Series and 74C Series meet MIL-STD-38510 zap test requirements of 400V from a 100 pF charging capacitor and 1.5 kΩ series resistance. This human body simulated model of 100 pF capacitance in series with 1.5 kΩ series resistance was proposed by Lenzlinger² and has been widely accepted by the industry. The set-up used to perform the zap test is shown in Figure 4.



Diode Breakdown

$D_1 = 25V$

$D_2 = 60V$

*These are intrinsic diodes

FIGURE 3. Transmission Gate with Intrinsic Diodes to Protect Against Static Discharge

V_{ZAP} is applied to DUT in the following modes by charging the 100 pF capacitor to V_{ZAP} with the switch S_1 in position 1 and then switching to position 2, thus discharging the charge through 1.5 kΩ series resistance into the device under test. Table 2 shows the various modes used for testing.

TABLE 2. Modes of High-Voltage Test

Mode	+ Terminal	- Terminal
1	Input	V_{SS}
2	V_{DD}	Input
3	Input	Associated Output
4	Associated Output	Input

Pre- and post-zap performance is monitored on the input leakage parameter at $V_{DD} = 18V$. It has been found that all Fairchild's CMOS devices of CD4000 and 74C families can withstand 400V zap testing with above mentioned conditions and still be under the pre- and post-zap input leakage conditions of ± 10 nA.

Handling Guide for CMOS Devices

From Table 1, it is apparent that extremely high static voltages generated in a manufacturing environment can destroy even the optimally protected devices by reaching their threshold failure energy levels. For preventing such catastrophes, simple precautions taken could save thousands of dollars for both the manufacturer and the user.

In handling unmounted chips, care should be taken to avoid differences in voltage potential between pins. Conductive carriers such as conductive foams or conductive rails should be used in transporting devices. The following simple precautions should also be observed.

1. Soldering-iron tips, metal parts of fixtures and tools, and handling facilities should be grounded.
2. Devices should not be inserted into or removed from circuits with the power on because transient voltages may cause permanent damage.
3. Table tops should be covered with grounded conductive tops. Also test areas should have conductive floor mats.

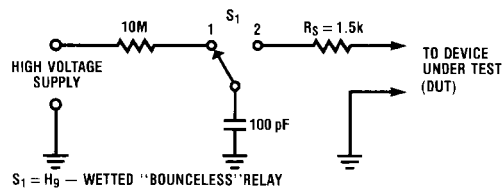


FIGURE 4. Equivalent RC Network to Simulate Human Body Static Discharge (after Lenzlinger²)

Above all, there should be static awareness amongst all personnel involved who handle CMOS devices or the sub-assembly boards. Automated feed mechanisms for testing of devices, for example, must be insulated from the device under test at the point where devices are connected to the test set. This is necessary as the transport path of devices can generate very high levels of static electricity due to continuous sliding of devices. Proper grounding of equipment or presence of ionized-air blowers can eliminate all these problems.

At Fairchild all CMOS devices are handled using all the precautions described above. The devices are also transported in anti-static rails or conductive foams. Anti-static, by definition³ means a container which resists generation of triboelectric charge (frictionally generated) as the device is inserted into, removed from, or allowed to slide around in it. It must be emphasized here that packaging problems will

Handling Guide for CMOS Devices (Continued)

not be solved merely by using anti-static rails or containers as they do not necessarily shield devices from external static fields, such as those generated by a charged person. Commercially available static shielding bags, such as 3M company's low resistivity ($\leq 10^4 \Omega/\text{sq.}$) metallic coated polyester bags, will help prevent damages due to external stray fields. These bags work on the well-known Faraday cage principle. Other commercially available materials are Legge company's conductive wrist straps, conductive floor coating, and various other grounding straps which help prevent against the electrostatic damage by providing conductive paths for the generated charge and equipotential surfaces.

It can be concluded that electrostatic discharge prevention is achievable with simple awareness and careful handling of CMOS devices. This will mean wide and useful applications of CMOS in system designs.

Footnotes

1. T.S. Speakman, "A Model for the Failure of Bipolar Silicon Integrated Circuits Subjected to ESD," 12th Annual Proc. of Reliability Physics, 1974.
2. M. Lenzlinger, "Gate Protection of MIS Devices," IEEE Transac. on Electron Devices, ED-18, No. 4, April 1971.
3. J.R. Huntsman, D.M. Yenni, G. Mueller, "Fundamental Requirements for Static Protective Containers." Presented at 1980 Nepcon/West Conference, Application Note—3M Static Control Systems.

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative