

74LCXZ16244

Low Voltage 16-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The LCXZ16244 contains sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

When V_{CC} is between 0 and 1.5V, the LCXZ16244 is in the high impedance state during power up or power down. This places the outputs in high impedance (Z) state preventing intermittent low impedance loading or glitching in bus oriented applications.

The LCXZ16244 is designed for low voltage (2.7V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCXZ16244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- Guaranteed power up/down high impedance
- Supports live insertion/withdrawal
- 2.7V–3.6V V_{CC} specifications provided
- 4.5 ns t_{PD} max ($V_{CC} = 3.0V$, 20% I_{CC} max)
- ± 24 mA output drive ($V_{OL} = 3.0V$)
- Implements patented non-EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance
- Human body model > 2000V
- Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

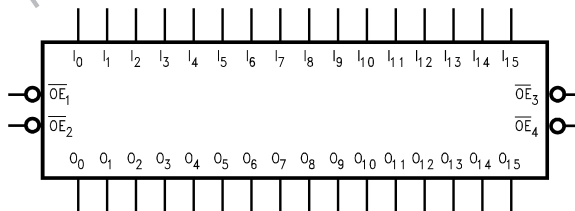
Ordering Code:

Order Number	Package Number	Package Description
74LCXZ16244GX (Note 1)	PC16244A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide (TAPE and REEL)
74LCXZ16244TA (Note 2)	MTD48A	18-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LCXZ16244MT (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 1: BGA package available in Tape and Reel only.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

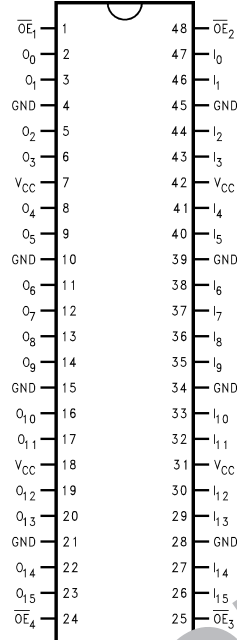
Logic Symbol



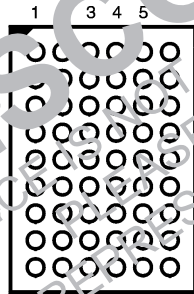
74LCXZ16244 Low Voltage 16-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs

Connection Diagrams

Pin Assignment for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
I_0-I_{15}	Inputs
O_0-O_{15}	Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	O_0	NC	\overline{OE}_1	\overline{OE}_2	NC	I_0
B	O_2	O_1	NC	NC	I_1	I_2
C	O_4	O_3	V_{CC}	V_{CC}	I_3	I_4
D	O_6	O_5	GND	GND	I_5	I_6
E	O_8	O_7	GND	GND	I_7	I_8
F	O_{10}	O_9	GND	GND	I_9	I_{10}
G	O_{12}	O_{11}	V_{CC}	V_{CC}	I_{11}	I_{12}
H	O_4	I_3	NC	NC	I_{13}	I_{14}
I	O_{15}	NC	\overline{OE}_4	\overline{OE}_3	NC	I_{15}

Truth Tables

Inputs		Outputs
\overline{OE}_1	I_0-I_2	O_0-O_3
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_2	I_4-I_7	O_4-O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_3	I_8-I_{11}	O_8-O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_4	$I_{12}-I_{15}$	$O_{12}-O_{15}$
L	L	L
L	H	H
H	X	Z

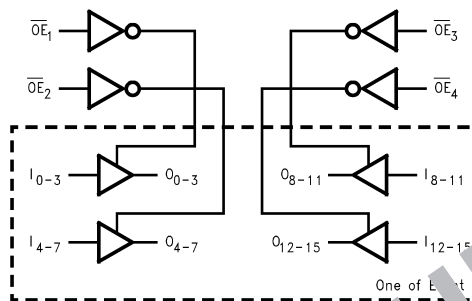
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Functional Description

The LCXZ16244 contains sixteen non-inverting buffers with 3-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The

3-STATE outputs are controlled by an Output Enable (\overline{OE}_n) input for each nibble. When \overline{OE}_n is LOW, the outputs are in 2-state mode. When \overline{OE}_n is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram



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Absolute Maximum Ratings (Note 3)						
Symbol	Parameter	Value	Conditions	Units		
V_{CC}	Supply Voltage	-0.5 to +7.0		V		
V_I	DC Input Voltage	-0.5 to +7.0		V		
V_O	DC Output Voltage	-0.5 to +7.0 -0.5 to $V_{CC} + 0.5$	Output in 3-STATE or $V_{CC} = 0-1.5V$ Output in HIGH or LOW State (Note 4)	V		
I_{IK}	DC Input Diode Current	-50	$V_I < GND$	mA		
I_{OK}	DC Output Diode Current	-50 +50	$V_O < GND$ $V_O > V_{CC}$	mA		
I_O	DC Output Source/Sink Current	± 50		mA		
I_{CC}	DC Supply Current per Supply Pin	± 100		mA		
I_{GND}	DC Ground Current per Ground Pin	± 100		mA		
T_{STG}	Storage Temperature	-65 to +150		°C		
Recommended Operating Conditions (Note 5)						
Symbol	Parameter	Min	Max	Units		
V_{CC}	Supply Voltage	2.7	3.6	V		
V_I	Input Voltage	0	5.5	V		
V_O	Output Voltage	0 0	V_{CC} 5.5	V		
I_{OH}/I_{OL}	Output Current	0	12 12	mA		
T_A	Free-Air Operating Temperature	0	85	°C		
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V-2.0V$	0	10	ns/V		
<p>Note 3: The Absolute Maximum Ratings are the values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.</p> <p>Note 4: I_O Absolute Maximum Rating must be observed.</p> <p>Note 5: Unused inputs must be held HIGH or LOW. They may not float.</p>						
DC Electrical Characteristics						
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40^\circ C$ to $+85^\circ C$		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7 - 3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.7 - 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -12 mA$	2.7	2.2		
		$I_{OH} = -18 mA$	3.0	2.4		
		$I_{OH} = -24 mA$	3.0	2.2		
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.7 - 3.6		0.2	V
		$I_{OL} = 12 mA$	2.7		0.4	
		$I_{OL} = 16 mA$	3.0		0.4	
		$I_{OL} = 24 mA$	3.0		0.55	
I_I	Input Leakage Current	$0 \leq V_I \leq 5.5V$	2.7 - 3.6		± 5.0	μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or V_{IL}	2.7 - 3.6		± 5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or $V_O = 5.5V$	0		10	μA
$I_{PU/PD}$	Power Up/Down 3-STATE Output Current	$V_O = 0.5V$ to V_{CC} $V_I = GND$ or V_{CC}	0 - 1.5		± 5.0	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7 - 3.6		225	μA
		$3.6V \leq V_I, V_O \leq 5.5V$ (Note 6)	2.7 - 3.6		± 225	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7 - 3.6		500	μA
Note 6: Outputs disabled or 3-STATE only.						

AC Electrical Characteristics						
Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, R_L = 500 \Omega$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		$C_L = 50 \text{ pF}$				
		Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.0	4.5	1.0	5.2	ns
t_{PLH}	Data to Output	1.0	4.5	1.0	5.2	
t_{PZL}	Output Enable Time	1.0	5.5	1.0	6.3	ns
t_{PZH}		1.0	5.5	1.0	6.3	
t_{PLZ}	Output Disable Time	1.0	5.4	1.0	5.7	ns
t_{PHZ}		1.0	5.4	1.0	5.7	
t_{OSHL}	Output to Output Skew (Note 7)		1.0			ns
t_{OSLH}			1.0			

Note 7: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameters are guaranteed by design.

Dynamic Switching Characteristics					
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25^\circ\text{C}$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50 \text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50 \text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$	3.3	-0.8	V

Capacitance				
Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_C = 0V, V_I = 0V \text{ or } V_{CC}$	7	pF
C_{OUT}	Output Capacitance	$V_C = 3.3V, V_I = 0V \text{ or } V_{CC}$	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}, f = 10 \text{ MHz}$	20	pF

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AC LOADING and WAVEFORMS Generic for LCX Family

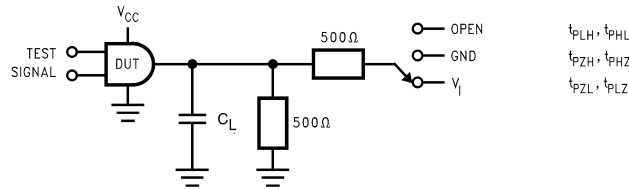
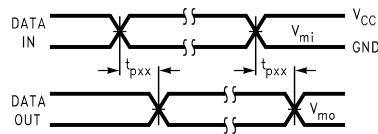
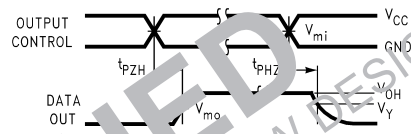


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

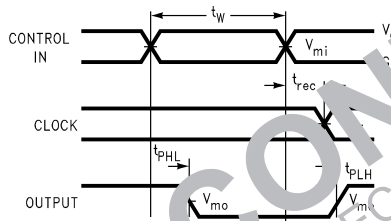
V_I	C_L
6V for $V_{CC} = 3.3V, 2.7V$	50 pF



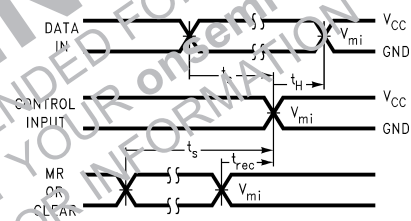
Waveform for Inverting and Non-Inverting Functions



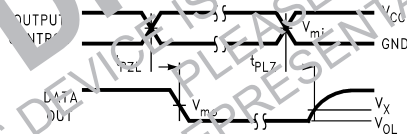
3-STATE Output High Enable and Disable Times for Logic



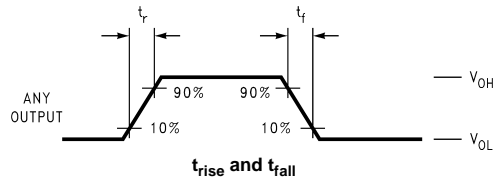
Propagation Delay, Pulse Width, and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

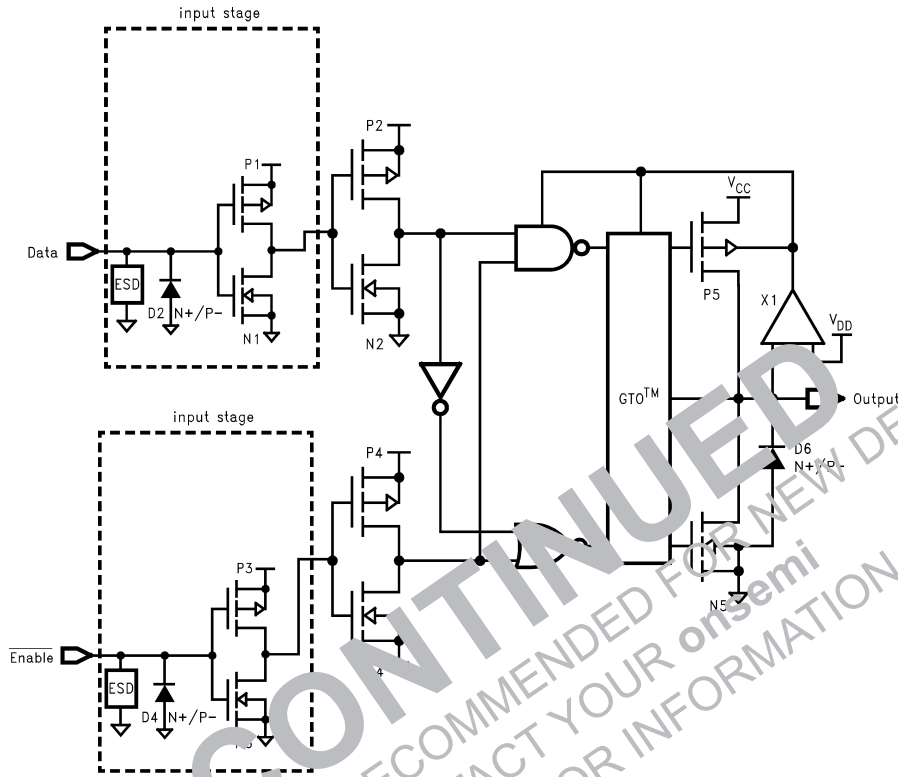


t_{rise} and t_{fall}

FIGURE 2. Waveforms
 (Input Characteristics; $f = 1\text{ MHz}, t_r = t_f = 3\text{ ns}$)

Symbol	V_{CC}	
	$3.3V \pm 0.3V$	$2.7V$
V_{mi}	1.5V	1.5V
V_{mo}	1.5V	1.5V
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$

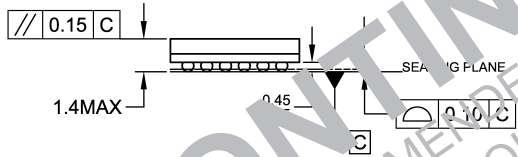
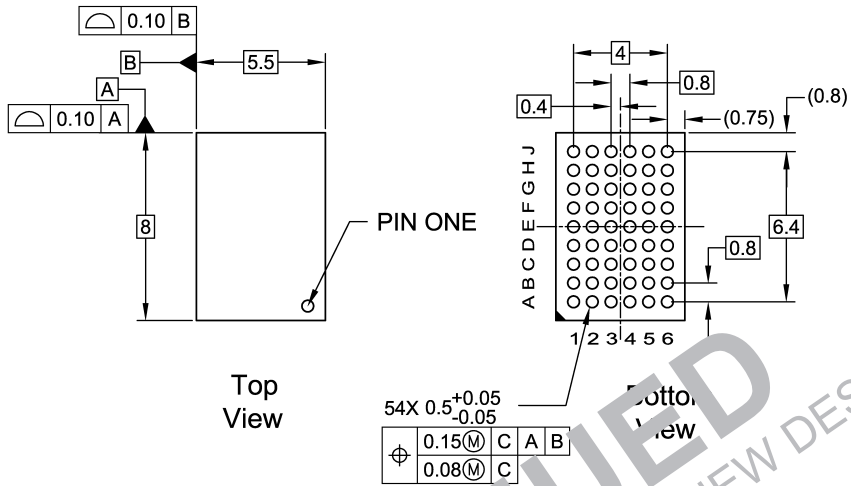
Schematic Diagram Generic for LCX Family



74LCXZ16244

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Physical Dimensions inches (millimeters) unless otherwise noted

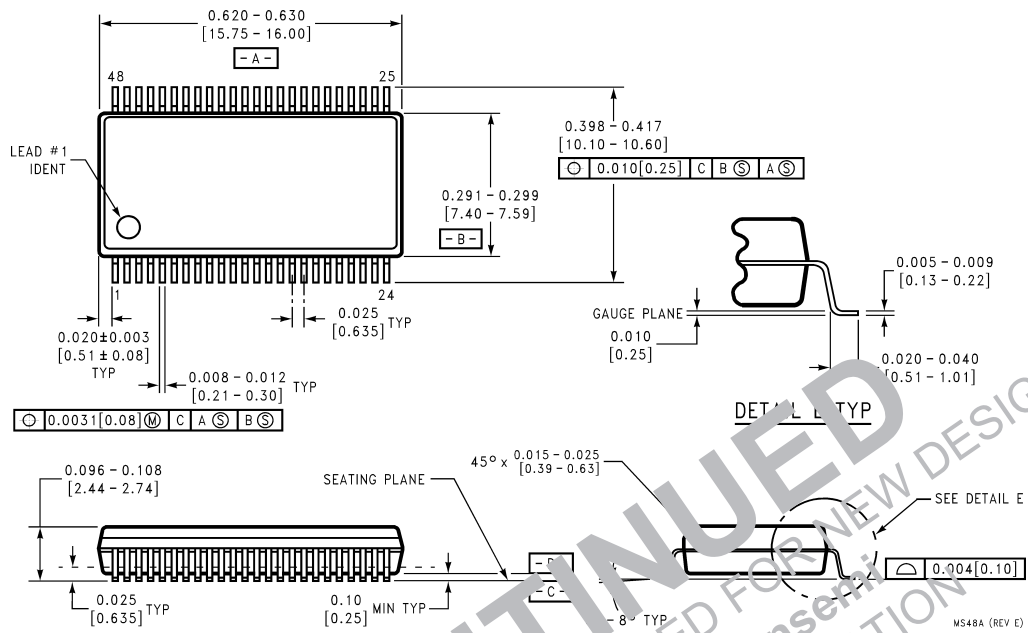


- NOTES:
- A. THIS PACKAGE CONFORMS TO JEDEC MO-205
 - B. ALL DIMENSIONS IN MILLIMETERS
 - C. BALL AND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
 - D. 0.5MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
 - E. DRAWING CONFORMS TO ASME Y14.3M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A
Preliminary**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

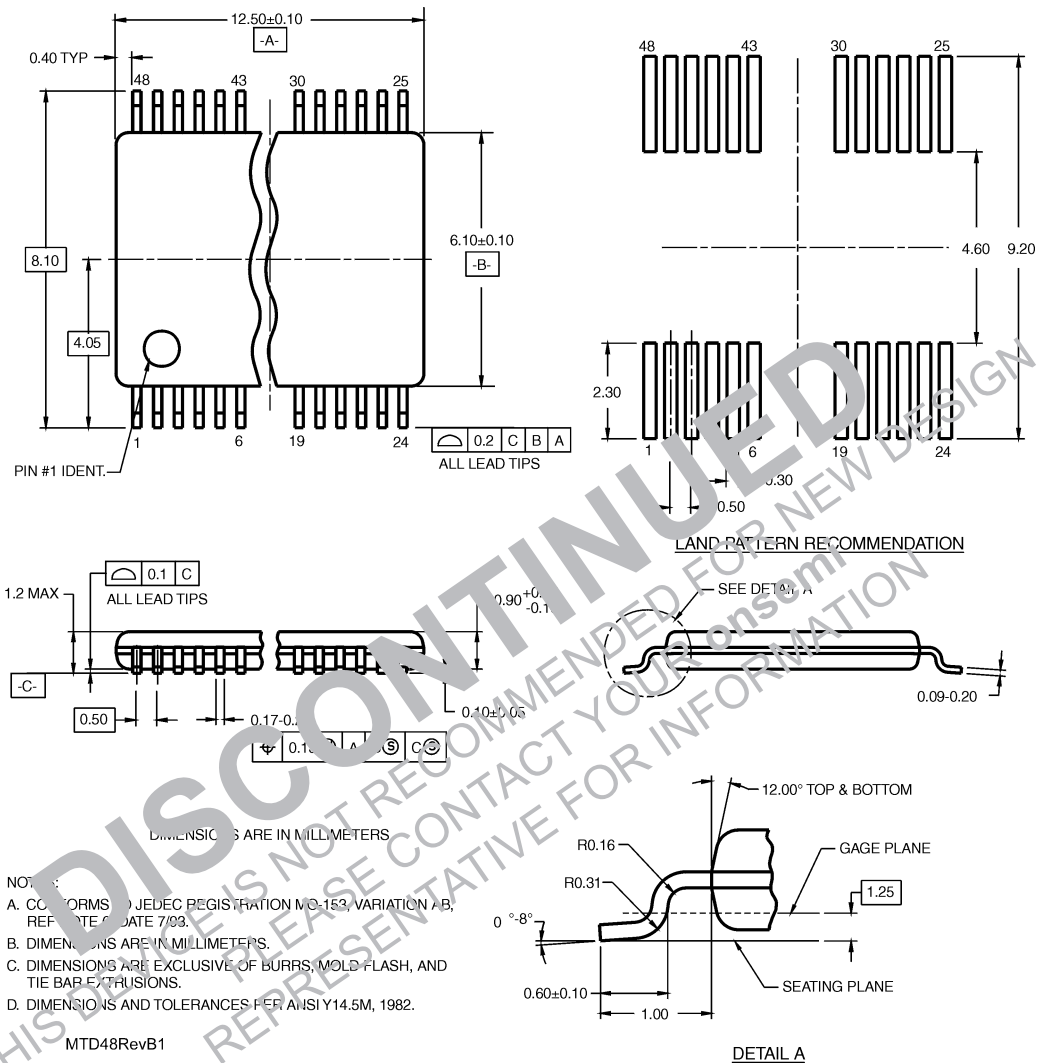


48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
 Part Number MS48A

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**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48**

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