

MOSFET - Power, Single N-Channel, D²PAK

650 V, 82 mΩ, 40 A

NVB082N65S3F

Description

SUPERFET[®] III MOSFET is ON Semiconductor’s brand–new high voltage super–junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on–resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency. SUPERFET III FRFET[®] MOSFET’s optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

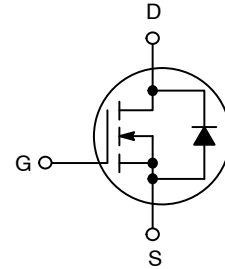
Features

- 700 V @ T_J = 150°C
- Typ. R_{DS(on)} = 64 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 81 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 722 pF)
- 100% Avalanche Tested
- Qualified with AEC–Q101
- These Devices are Pb–Free and are RoHS Compliant

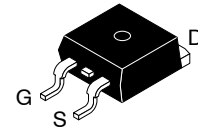
Typical Applications

- Automotive On Board Charger
- Automotive DC/DC Converter for HEV

| V _{(BR)DSS} | R _{DS(ON)} MAX | I _D MAX |
|----------------------|-------------------------|--------------------|
| 650 V | 82 mΩ @ 10 V | 40 A |

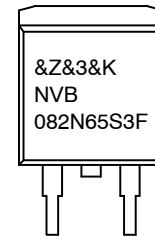


N-CHANNEL MOSFET



D²PAK–3
 TO–263
 CASE 418AJ

MARKING DIAGRAM



- &Z = Assembly Plant Code
- &3 = Data Code (Year & Week)
- &K = Lot
- NVB082N65S3F = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

NVB082N65S3F

Table 1. ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise stated)

| Symbol | Parameter | Value | Unit |
|----------------|--|--|------------------|
| V_{DSS} | Drain-to-Source Voltage | 650 | V |
| V_{GS} | Gate-to-Source Voltage | - DC | ± 30 |
| | | - AC ($f > 1$ Hz) | ± 30 |
| I_D | Drain Current | - Continuous ($T_C = 25^\circ\text{C}$) | 40 |
| | | - Continuous ($T_C = 100^\circ\text{C}$) | 25.5 |
| I_{DM} | Drain Current | - Pulsed (Note 1) | 100 |
| E_{AS} | Single Pulse Avalanche Energy (Note 2) | 510 | mJ |
| I_{AS} | Avalanche Current | 4.8 | A |
| E_{AR} | Repeated Avalanche Energy (Note 1) | 3.13 | mJ |
| dv/dt | MOSFET dv/dt | 100 | V/ns |
| | Peak Diode Recovery dv/dt (Note 3) | 50 | |
| P_D | Power Dissipation | $T_C = 25^\circ\text{C}$ | 313 |
| | | - Derate Above 25°C | 2.5 |
| T_J, T_{stg} | Operating Junction and Storage Temperature | -55 to 150 | $^\circ\text{C}$ |
| T_L | Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds | 300 | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{AS} = 4.8$ A, $R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $ISD \leq 20$ A, $di/dt \leq 200$ A/_s, $V_{DD} \leq 400$ V, starting $T_C = 25^\circ\text{C}$.

Table 2. THERMAL RESISTANCE RATINGS

| Symbol | Parameter | Max | Unit |
|-----------------|---|------|---------------------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case, Max. | 0.40 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient, Max. | 40 | |

NVB082N65S3F

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------|-----------|-----------------|-----|-----|-----|------|
|--------|-----------|-----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|------------------------------|---|--|-----|-----|-----------|---------------------|
| BV_{DSS} | Drain-to-Source Breakdown Voltage | $V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$ | 650 | - | - | V |
| | | $V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 150^\circ\text{C}$ | 700 | - | - | V |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D = 20\text{ mA}$, Referenced to 25°C | - | 0.7 | - | V/ $^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$ | - | - | 10 | μA |
| | | $V_{DS} = 520\text{ V}, T_C = 125^\circ\text{C}$ | - | 175 | - | μA |
| I_{GSS} | Gate-to-Body Leakage Current | $V_{DS} = 0\text{ V}, V_{GS} = \pm 30\text{ V}$ | - | - | ± 100 | nA |

ON CHARACTERISTICS

| | | | | | | |
|--------------|--------------------------------------|---|-----|----|-----|------------|
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS} = V_{DS}, I_D = 1\text{ mA}$ | 3.0 | - | 5.0 | V |
| $R_{DS(on)}$ | Static Drain-to-Source On Resistance | $V_{GS} = 10\text{ V}, I_D = 20\text{ A}$ | - | 64 | 82 | m Ω |
| g_{FS} | Forward Transconductance | $V_{GS} = 20\text{ V}, I_D = 20\text{ A}$ | - | 24 | - | S |

DYNAMIC CHARACTERISTICS

| | | | | | | |
|-----------------|-----------------------------------|--|---|------|---|----------|
| C_{iss} | Input Capacitance | $V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | - | 3410 | - | pF |
| C_{oss} | Output Capacitance | | - | 70 | - | pF |
| $C_{oss(eff.)}$ | Effective Output Capacitance | $V_{DS} = 0\text{ to }400\text{ V}, V_{GS} = 0\text{ V}$ | - | 722 | - | pF |
| $C_{oss(er.)}$ | Energy Related Output Capacitance | $V_{DS} = 0\text{ to }400\text{ V}, V_{GS} = 0\text{ V}$ | - | 126 | - | pF |
| $Q_{g(total)}$ | Total Gate Charge at 10 V | $V_{DS} = 400\text{ V}, I_D = 20\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4) | - | 81 | - | nC |
| Q_{gs} | Gate-to-Source Gate Charge | | - | 24 | - | nC |
| Q_{gd} | Gate-to-Drain "Miller" Charge | | - | 32 | - | nC |
| ESR | Equivalent Series Resistance | $F = 1\text{ MHz}$ | - | 1.9 | - | Ω |

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$

| | | | | | | |
|--------------|---------------------|--|---|----|---|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 400\text{ V}, I_D = 20\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 4.7\text{ }\Omega$ (Note 4) | - | 31 | - | ns |
| t_r | Rise Time | | - | 29 | - | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | - | 76 | - | ns |
| t_f | Fall Time | | - | 16 | - | ns |

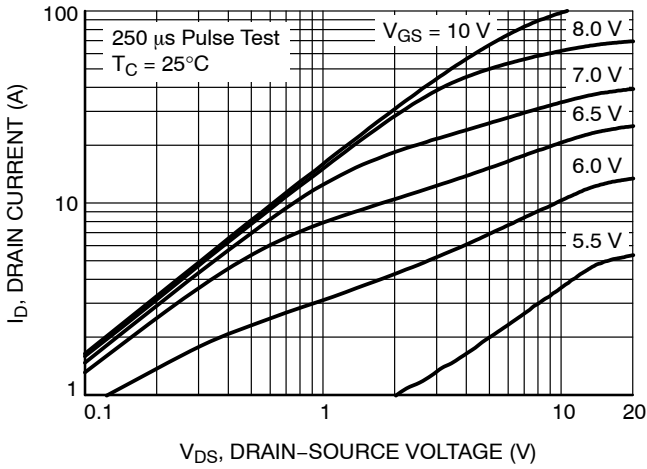
SOURCE-DRAIN DIODE CHARACTERISTICS

| | | | | | | |
|----------|--|--|---|-----|-----|----|
| I_S | Maximum Continuous Source-to-Drain Diode Forward Current | - | - | 40 | A | |
| I_{SM} | Maximum Pulsed Source-to-Drain Diode Forward Current | - | - | 100 | A | |
| V_{SD} | Source-to-Drain Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_{SD} = 20\text{ A}$ | - | - | 1.3 | V |
| t_{rr} | Reverse-Recovery Time | $V_{GS} = 0\text{ V}, I_{SD} = 20\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$ | - | 108 | - | ns |
| Q_{rr} | Reverse-Recovery Charge | | - | 410 | - | nC |

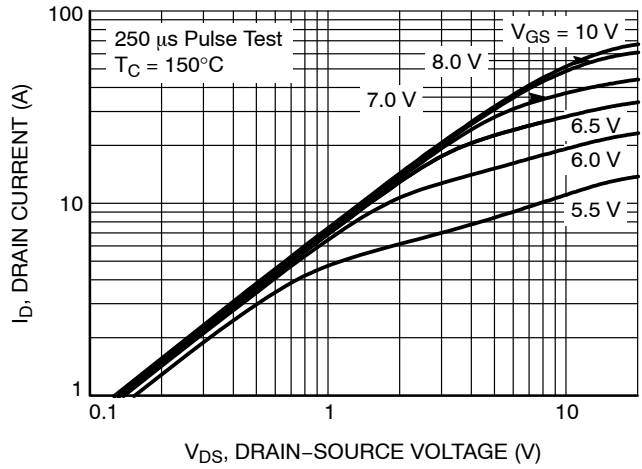
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS



**Figure 1. On-Region Characteristics
25°C**



**Figure 2. On-Region Characteristics
150°C**

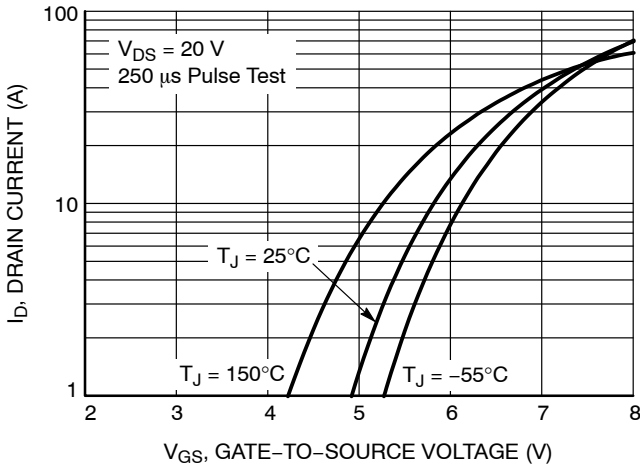
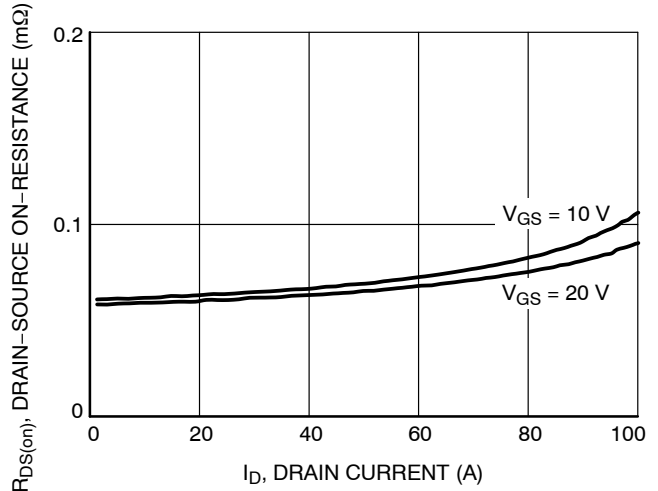
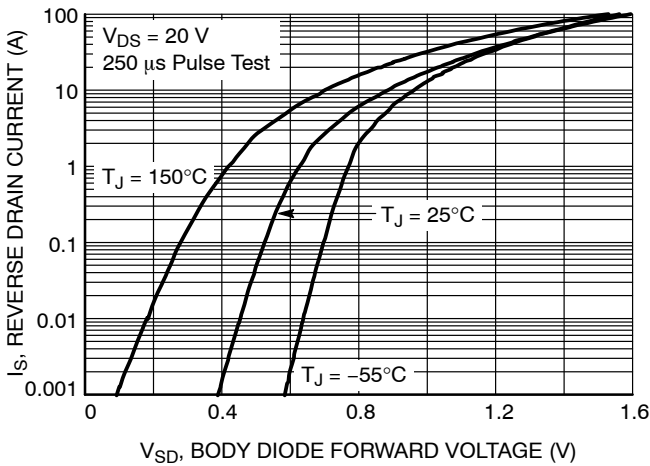


Figure 3. Transfer Characteristics



**Figure 4. On-Resistance Variation vs. Drain
Current and Gate Voltage**



**Figure 5. Body Diode Forward Voltage
Variation vs. Source Current and Temperature**

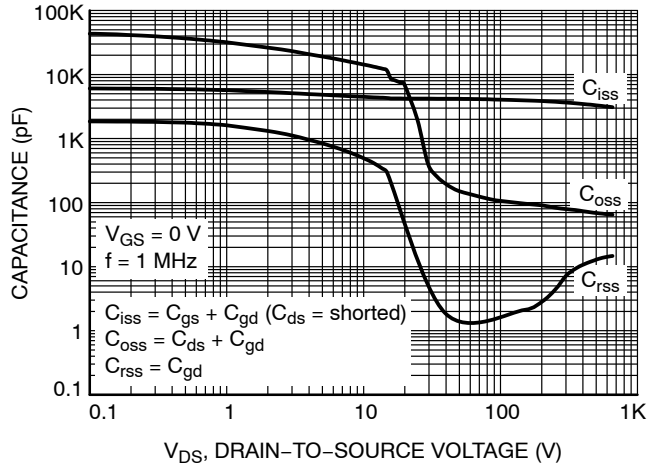


Figure 6. Capacitance Characteristics

TYPICAL CHARACTERISTICS

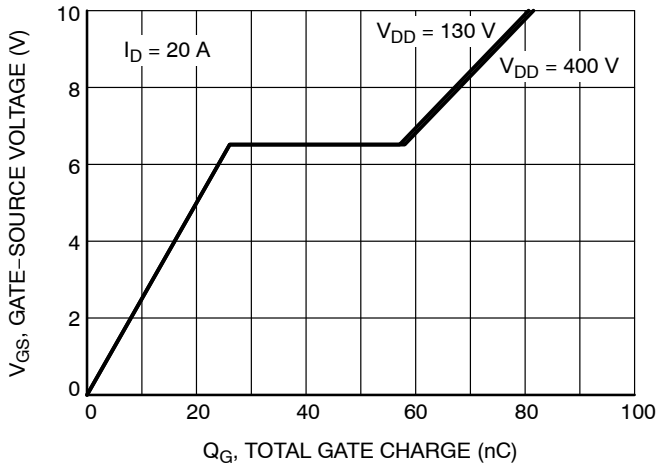


Figure 7. Gate Charge Characteristics

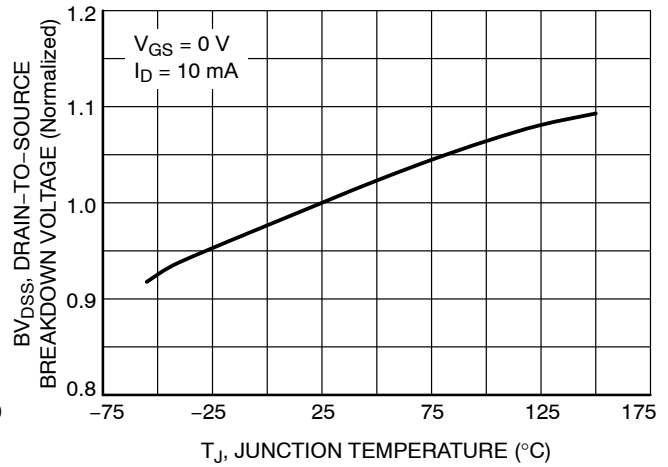


Figure 8. Breakdown Voltage Variation vs. Temperature

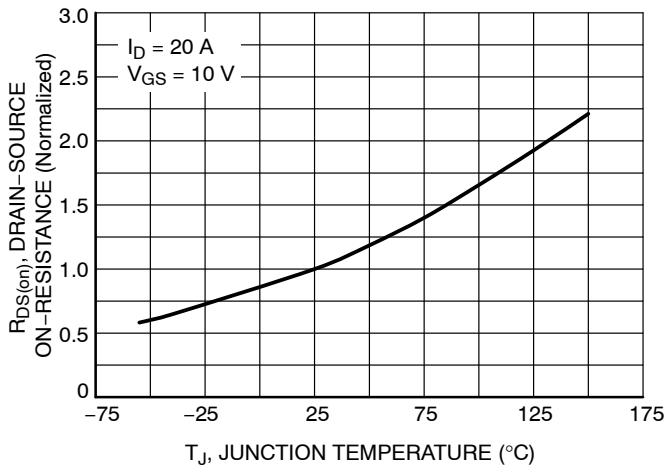


Figure 9. On-Resistance Variation vs. Temperature

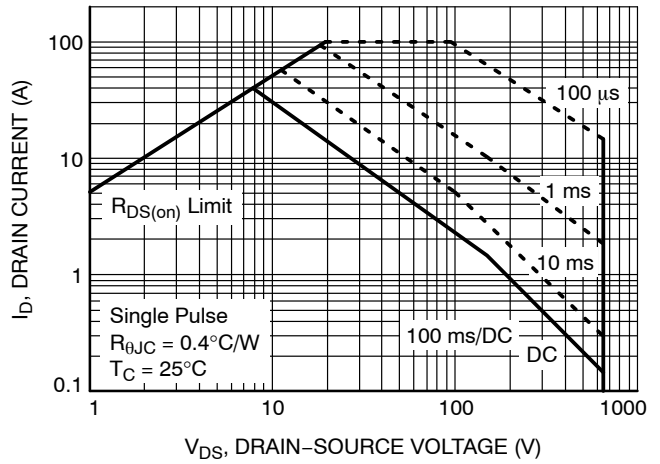


Figure 10. Maximum Safe Operating Area

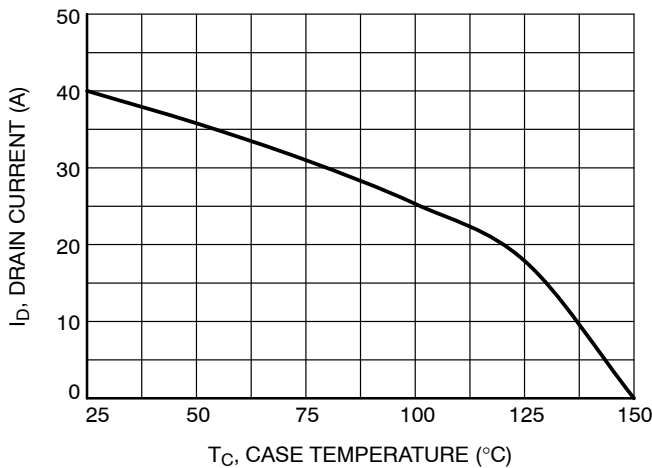


Figure 11. Maximum Drain Current vs. Case Temperature

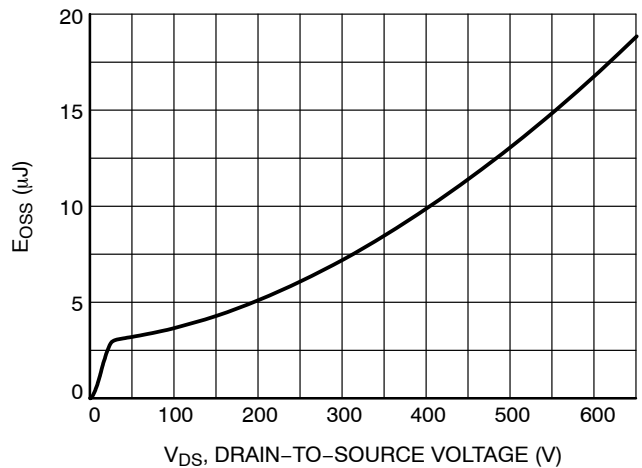


Figure 12. E_{OSS} vs. Drain-to-Source Voltage

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TYPICAL CHARACTERISTICS

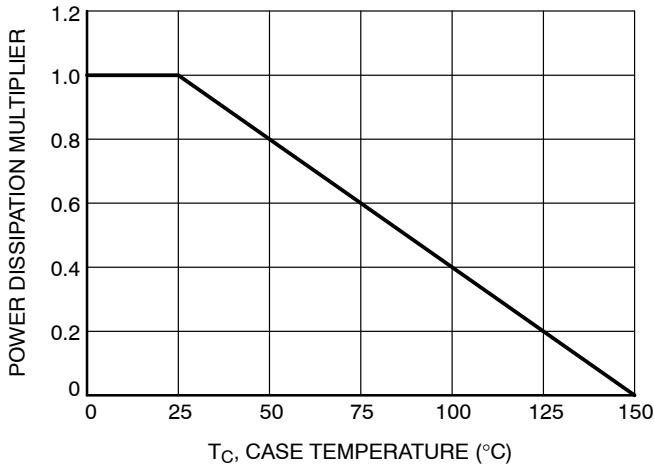


Figure 13. Normalized Power Dissipation vs. Case Temperature

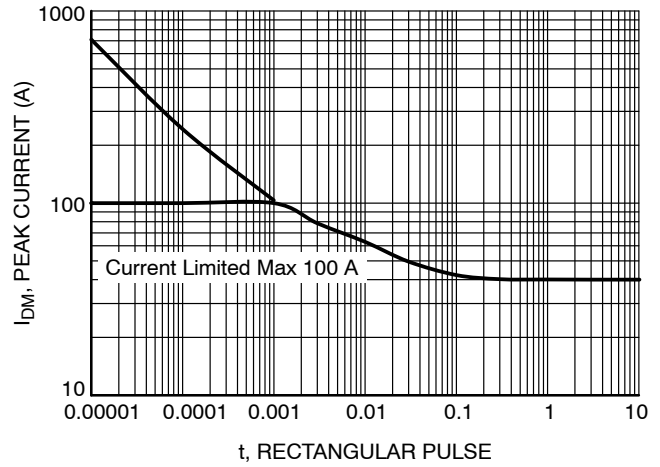


Figure 14. Peak Current Capability

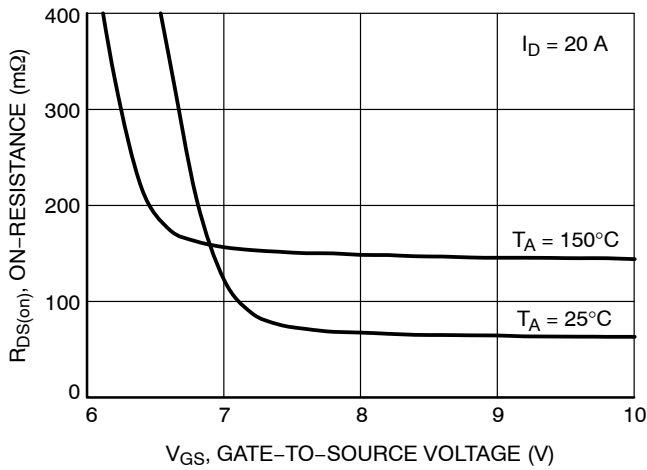


Figure 15. $R_{DS(on)}$ vs. Gate Voltage

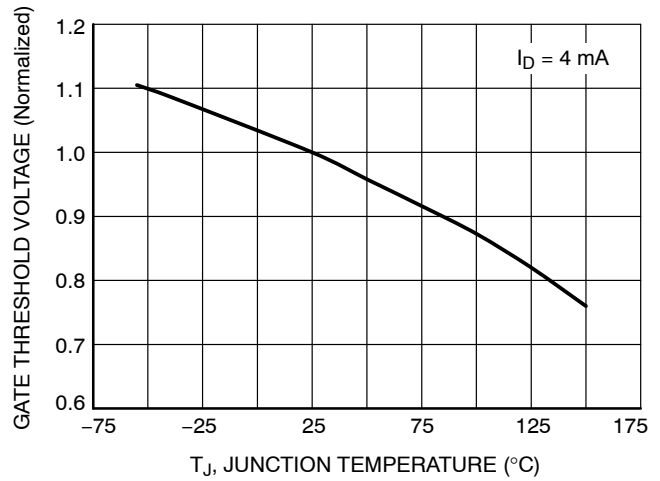


Figure 16. Normalized Gate Threshold Voltage vs. Temperature

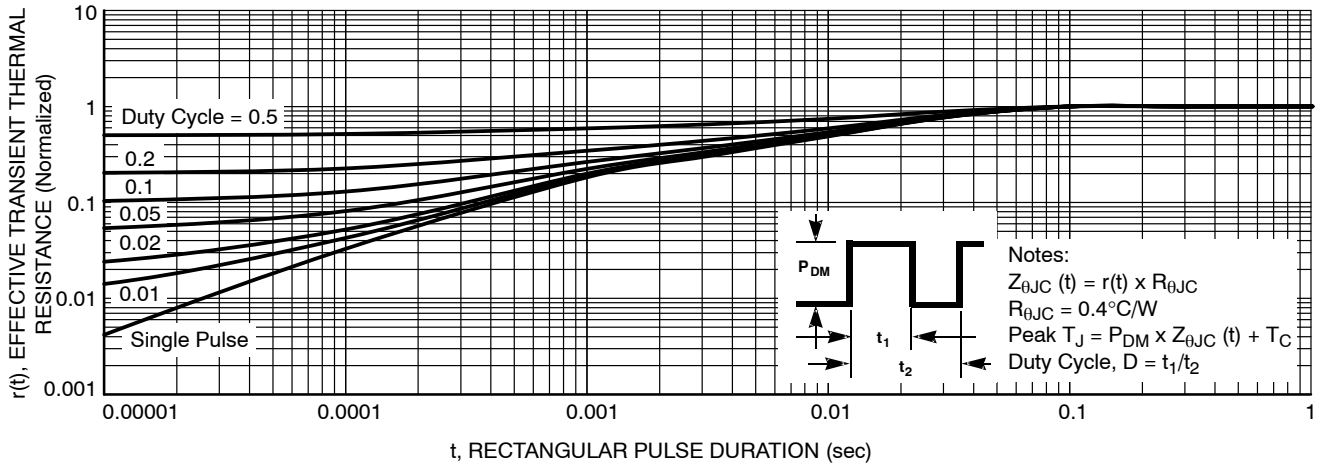


Figure 17. Transient Thermal Response

NVB082N65S3F

PACKAGE MARKING AND ORDERING INFORMATION

| Part Number | Top Marking | Package | Packing Method | Reel Size | Tape Width | Quantity |
|--------------|--------------|--------------------|----------------|-----------|------------|-----------|
| NVB082N65S3F | NVB082N65S3F | D ² PAK | Tape & Reel† | 330 mm | 24 mm | 800 Units |

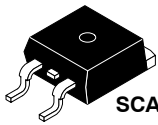
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



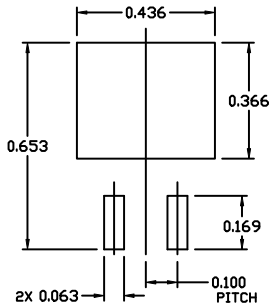
SCALE 1:1

D²PAK-3 (TO-263, 3-LEAD)

CASE 418AJ

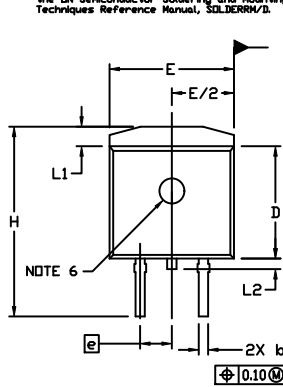
ISSUE F

DATE 11 MAR 2021



RECOMMENDED MOUNTING FOOTPRINT

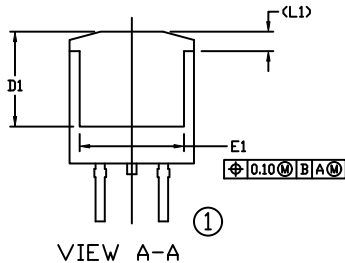
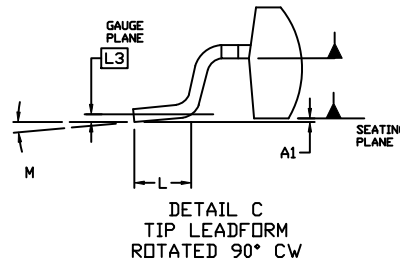
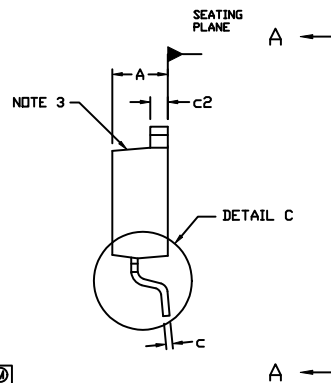
■ For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



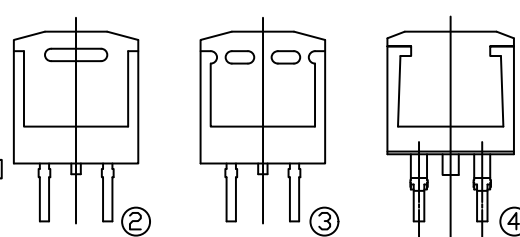
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: INCHES
- CHAMFER OPTIONAL.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
- OPTIONAL MOLD FEATURE.
- ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.160 | 0.190 | 4.06 | 4.83 |
| A1 | 0.000 | 0.010 | 0.00 | 0.25 |
| b | 0.020 | 0.039 | 0.51 | 0.99 |
| c | 0.012 | 0.029 | 0.30 | 0.74 |
| c2 | 0.045 | 0.065 | 1.14 | 1.65 |
| D | 0.330 | 0.380 | 8.38 | 9.65 |
| D1 | 0.260 | --- | 6.60 | --- |
| E | 0.380 | 0.420 | 9.65 | 10.67 |
| E1 | 0.245 | --- | 6.22 | --- |
| e | 0.100 | BSC | 2.54 | BSC |
| H | 0.575 | 0.625 | 14.60 | 15.88 |
| L | 0.070 | 0.110 | 1.78 | 2.79 |
| L1 | --- | 0.066 | --- | 1.68 |
| L2 | --- | 0.070 | --- | 1.78 |
| L3 | 0.010 | BSC | 0.25 | BSC |
| M | 0* | 8* | 0* | 8* |

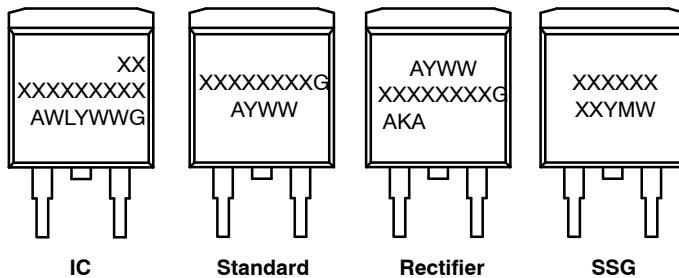


VIEW A-A



VIEW A-A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC

Standard

Rectifier

SSG

- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- W = Week Code (SSG)
- M = Month Code (SSG)
- G = Pb-Free Package
- AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|------------------|---------------------------------------|--|
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| DESCRIPTION: | D ² PAK-3 (TO-263, 3-LEAD) | PAGE 1 OF 1 |

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