

# NTMFS4H01NF

## MOSFET – Power, Single, N-Channel, SO-8FL 25 V, 334 A



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### Features

- Integrated Schottky Diode
- Optimized Design to Minimize Conduction and Switching Losses
- Optimized Package to Minimize Parasitic Inductances
- Optimized material for improved thermal performance
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- High Performance DC-DC Converters
- System Voltage Rails
- Netcom, Telecom
- Servers & Point of Load

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter	Symbol	Value	Units
Drain-to-Source Voltage	V <sub>DSS</sub>	25	V
Gate-to-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current R <sub>θJA</sub> (T <sub>A</sub> = 25°C, Note 1)	I <sub>D</sub>	54	A
Power Dissipation R <sub>θJA</sub> (T <sub>A</sub> = 25°C, Note 1)	P <sub>D</sub>	3.2	W
Continuous Drain Current R <sub>θJC</sub> (T <sub>C</sub> = 25°C, Note 1)	I <sub>D</sub>	334	A
Power Dissipation R <sub>θJC</sub> (T <sub>C</sub> = 25°C, Note 1)	P <sub>D</sub>	125	W
Pulsed Drain Current (t <sub>p</sub> = 10 μs)	I <sub>DM</sub>	568	A
Single Pulse Drain-to-Source Avalanche Energy (Note 1) (I <sub>L</sub> = 57 A <sub>pk</sub> , L = 0.3 mH)	E <sub>AS</sub>	487	mJ
Drain to Source dV/dt	dV/dt	7	V/ns
Maximum Junction Temperature	T <sub>J(max)</sub>	150	°C
Storage Temperature Range	T <sub>STG</sub>	-55 to 150	°C
Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions (Note 2)	T <sub>SLD</sub>	260	°C

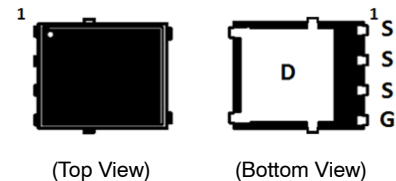
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Values based on copper area of 645 mm<sup>2</sup> (or 1 in<sup>2</sup>) of 2 oz copper thickness and FR4 PCB substrate.
2. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
3. This is the absolute maximum rating. Parts are 100% UIS tested at T<sub>J</sub> = 25°C, V<sub>GS</sub> = 10 V, I<sub>L</sub> = 37 A, E<sub>AS</sub> = 205 mJ.

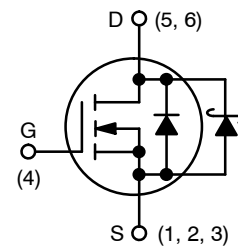
V <sub>GS</sub>	MAX R <sub>DS(on)</sub>	TYP Q <sub>GTOT</sub>
4.5 V	1.0 mΩ	37.8 nC
10 V	0.7 mΩ	82 nC

### PIN CONNECTIONS

SO8-FL (5 x 6 mm)



### N-CHANNEL MOSFET



### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 7 of this data sheet.

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## THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Units
Thermal Resistance, Junction-to-Ambient (Note 1 and 4)	$R_{\theta JA}$	38.9	$^{\circ}\text{C}/\text{W}$
Junction-to-Case (Note 1 and 4)	$R_{\theta JC}$	1.0	

4. Thermal Resistance  $R_{\theta JA}$  and  $R_{\theta JC}$  as defined in JESD51-3.

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## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	25			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 10\text{ mA}$ reference to $25^\circ\text{C}$		16		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$			500	$\mu\text{A}$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = +20\text{ V}$			+100	nA

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.2		2.1	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 10\text{ mA}$ reference to $25^\circ\text{C}$		3.7		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$	0.56	0.7		$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 30\text{ A}$	0.79	1		
Forward Transconductance	$g_{FS}$	$V_{DS} = 12\text{ V}, I_D = 20\text{ A}$		101		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 12\text{ V}$		5538		$\text{pF}$
Output Capacitance	$C_{OSS}$			3416		
Reverse Transfer Capacitance	$C_{RSS}$			175.3		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 12\text{ V}; I_D = 30\text{ A}$		37.8		$\text{nC}$
Threshold Gate Charge	$Q_{G(TH)}$			2.3		
Gate-to-Source Charge	$Q_{GS}$			11.8		
Gate-to-Drain Charge	$Q_{GD}$			8		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 12\text{ V}; I_D = 30\text{ A}$		82		$\text{nC}$
Gate Resistance	$R_G$	$T_A = 25^\circ\text{C}$		1.3	2	$\Omega$

### SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$ (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 12\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		16.9		$\text{ns}$
Rise Time	$t_r$			42.3		
Turn-Off Delay Time	$t_{d(OFF)}$			46.3		
Fall Time	$t_f$			30.9		

### SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DD} = 12\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		10.9		$\text{ns}$
Rise Time	$t_r$			33.2		
Turn-Off Delay Time	$t_{d(OFF)}$			58.3		
Fall Time	$t_f$			23.3		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 2.0\text{ A}$	$T_J = 25^\circ\text{C}$	0.35	0.6	V
			$T_J = 125^\circ\text{C}$	0.27		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 30\text{ A}$		66.7		$\text{ns}$
Charge Time	$t_a$			33.1		
Discharge Time	$t_b$			33.6		
Reverse Recovery Charge	$Q_{RR}$			90		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

6. Switching characteristics are independent of operating junction temperatures.

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## TYPICAL CHARACTERISTICS

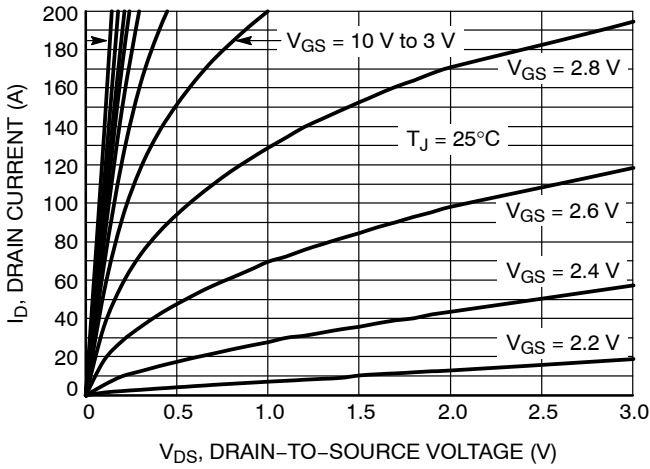


Figure 1. On-Region Characteristics

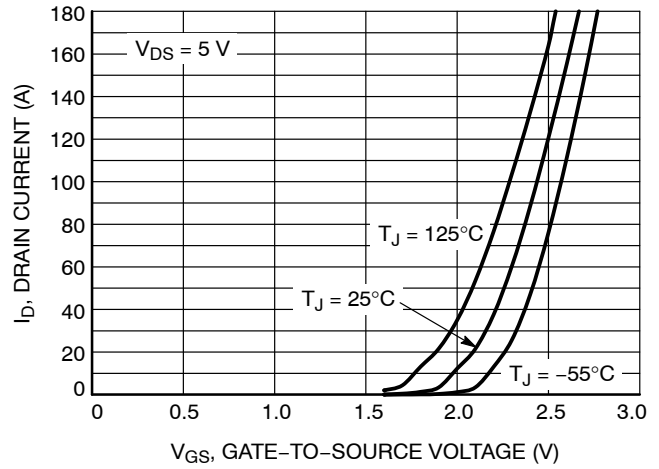


Figure 2. Transfer Characteristics

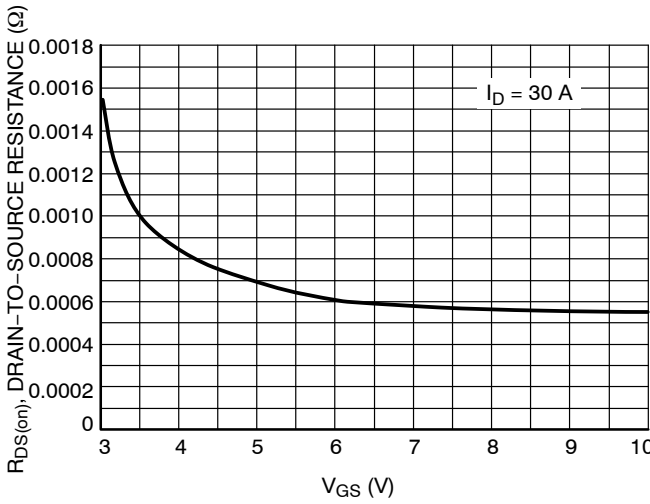


Figure 3. On-Resistance vs.  $V_{GS}$

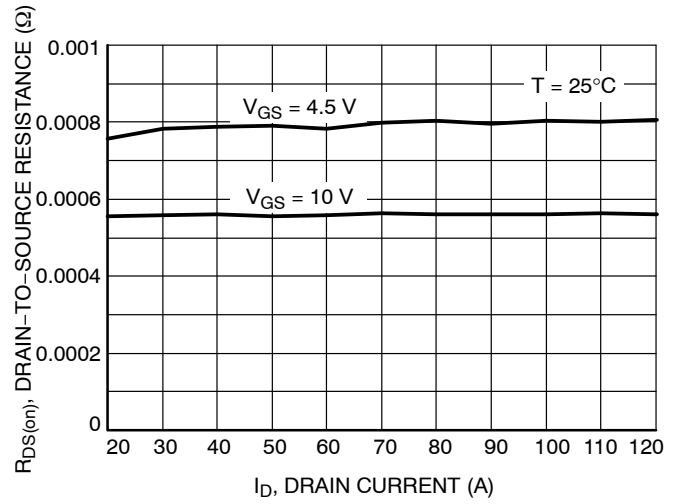


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

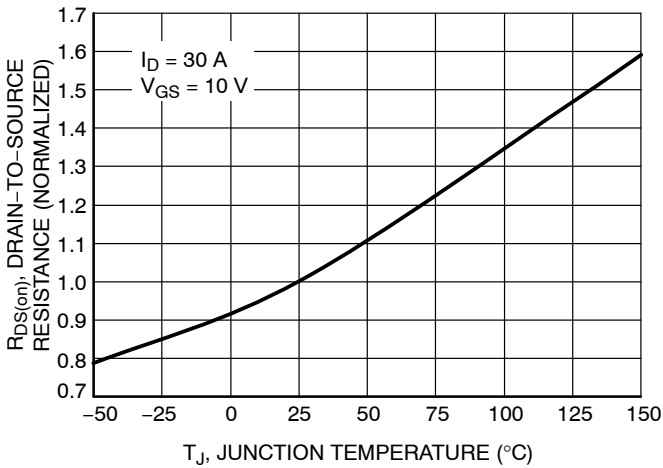


Figure 5. On-Resistance Variation with Temperature

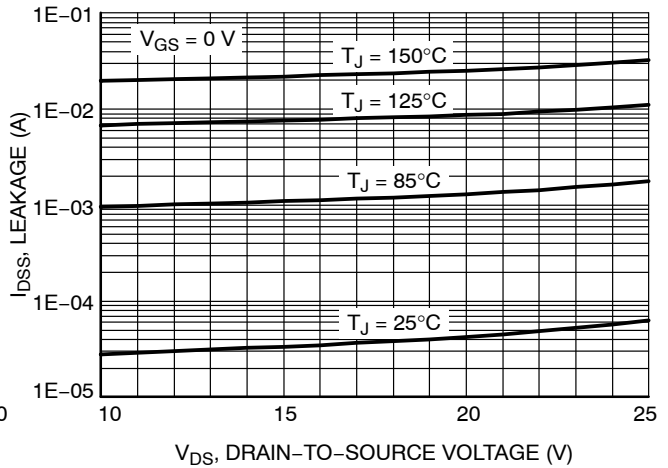
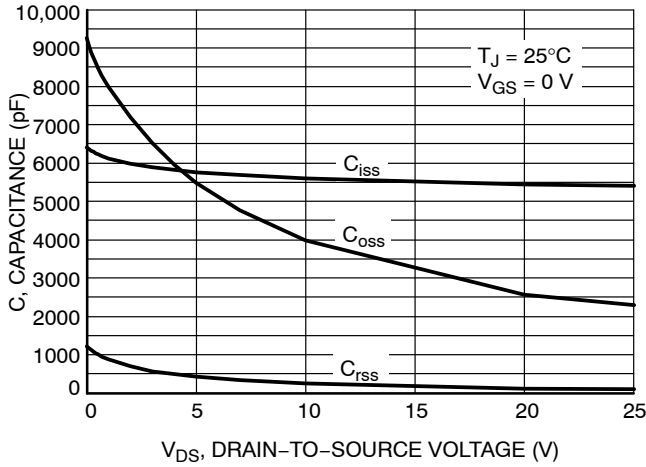


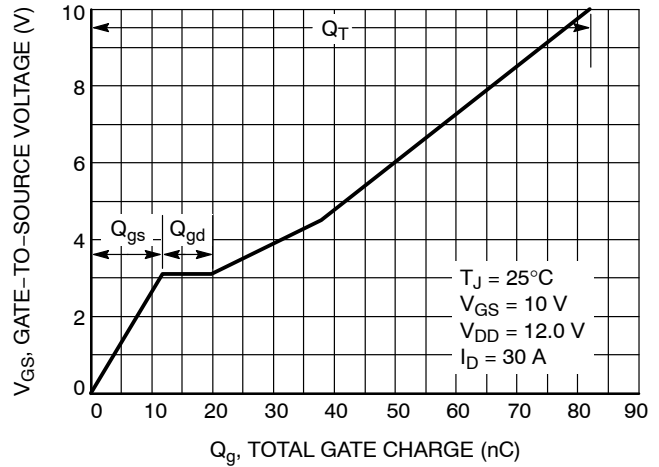
Figure 6. Drain-to-Source Leakage Current vs. Voltage

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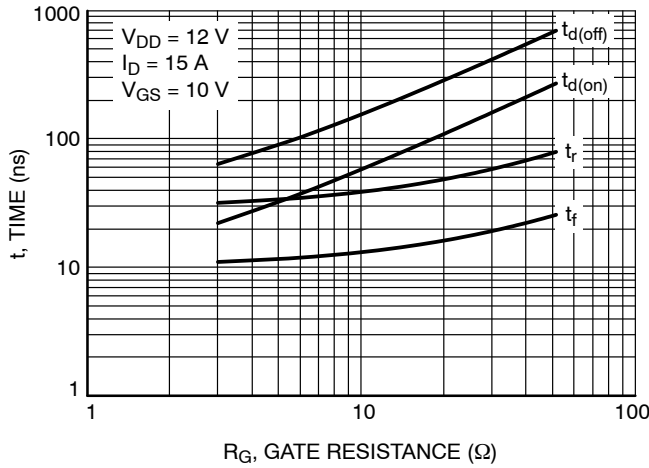
## TYPICAL CHARACTERISTICS



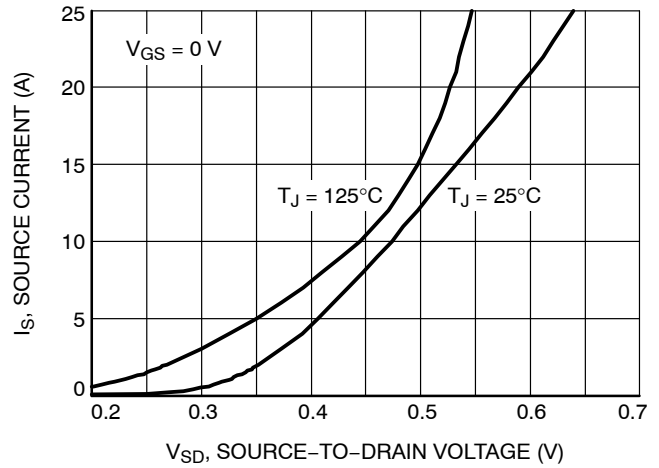
**Figure 7. Capacitance Variation**



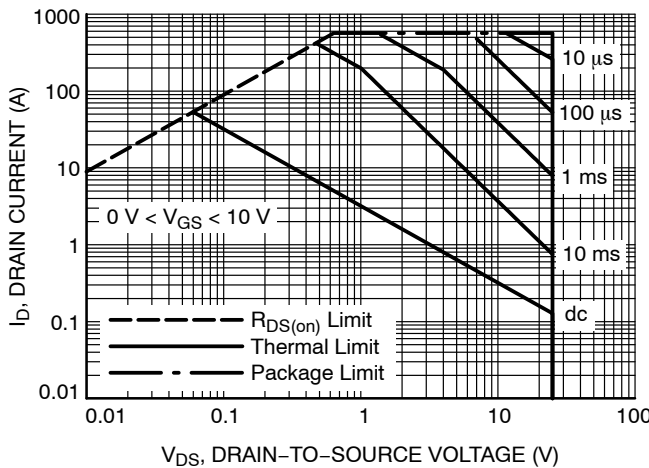
**Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



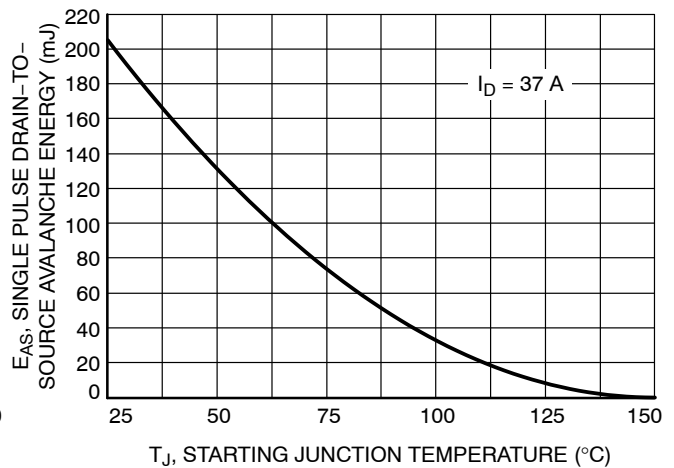
**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 10. Diode Forward Voltage vs. Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

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## TYPICAL CHARACTERISTICS

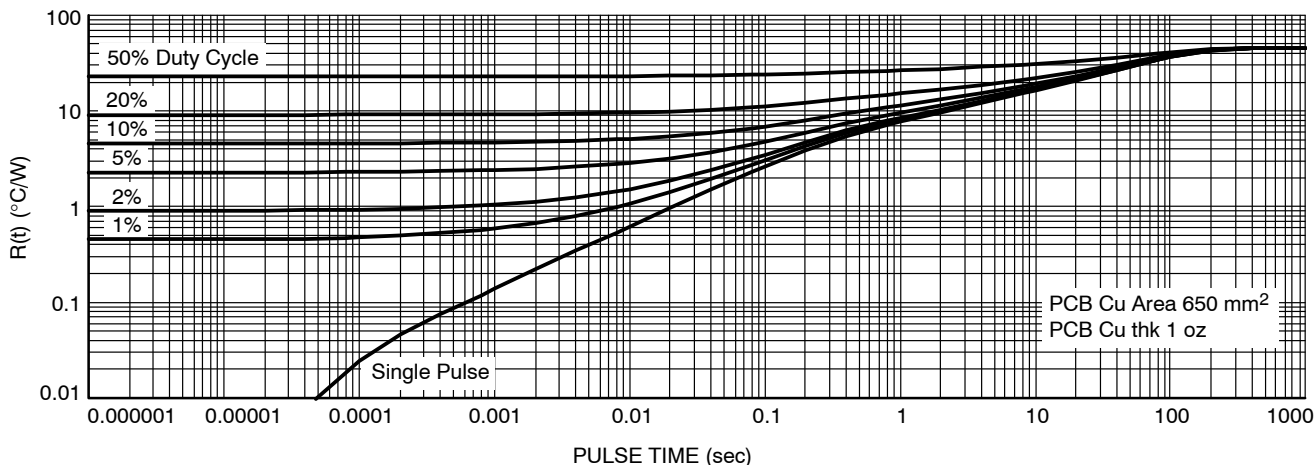


Figure 13. Thermal Characteristics

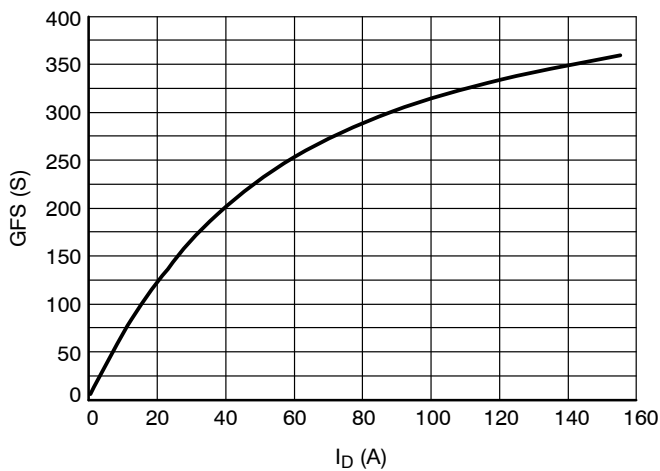


Figure 14. GFS vs.  $I_D$

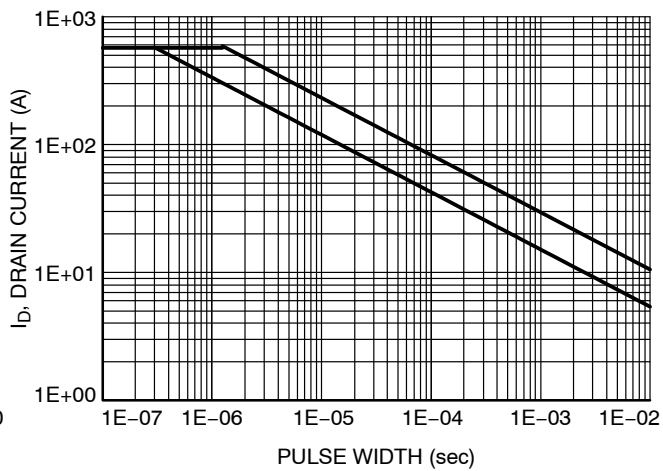


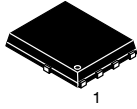
Figure 15. Avalanche Characteristics

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## ORDERING INFORMATION

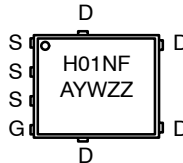
Device	Package	Shipping†
NTMFS4H01NFT1G	SO8-FL (Pb-Free)	1500 / Tape & Reel
NTMFS4H01NFT3G	SO8-FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



**SO-8 FLAT LEAD  
CASE 488AA  
STYLE 1**

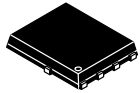
### MARKING DIAGRAM



A = Assembly Location  
 Y = Year  
 W = Work Week  
 ZZ = Lot Traceability

# MECHANICAL CASE OUTLINE

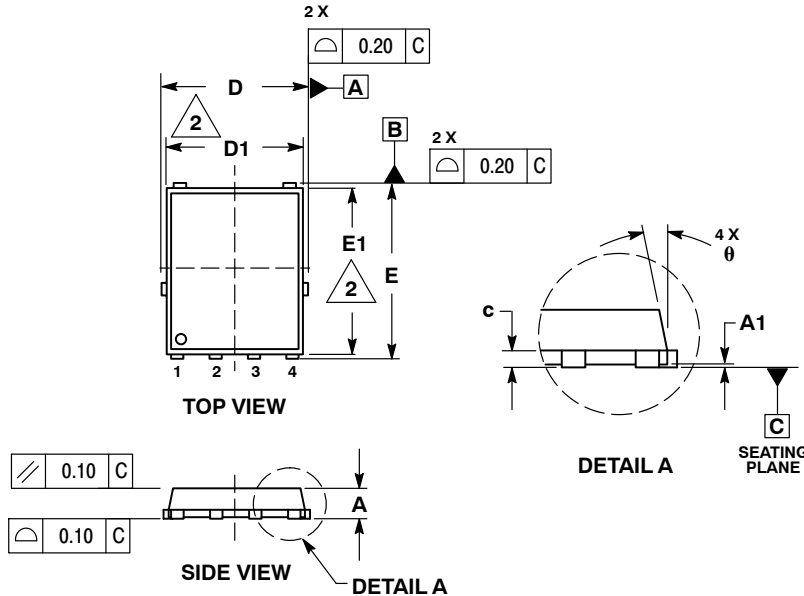
## PACKAGE DIMENSIONS



1  
SCALE 2:1

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE N

DATE 25 JUN 2018

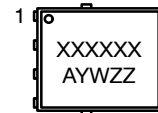


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

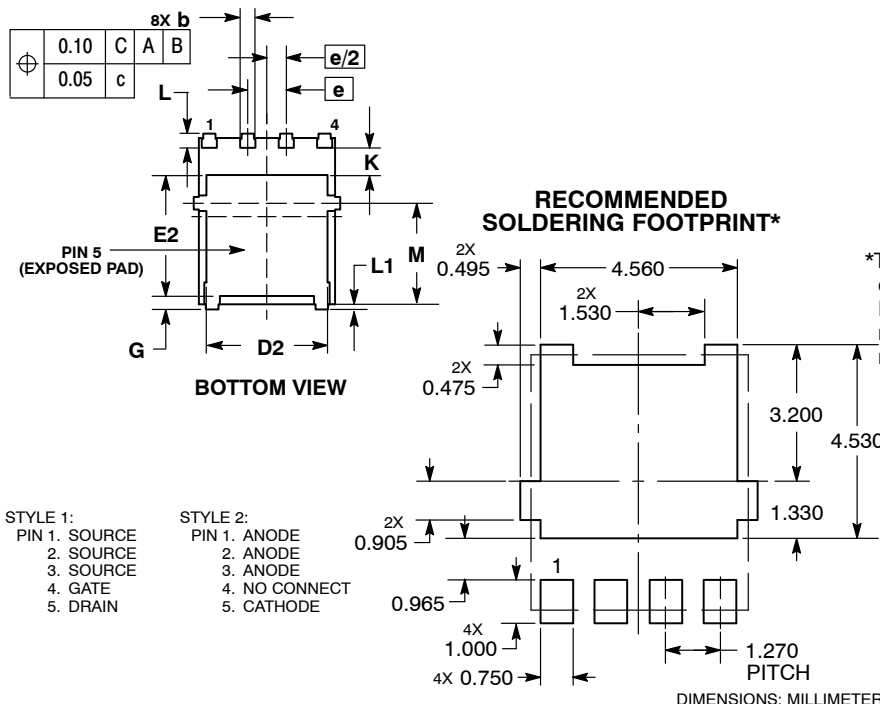
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



- STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN
- STYLE 2:  
PIN 1. ANODE  
2. ANODE  
3. ANODE  
4. NO CONNECT  
5. CATHODE

DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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