

NST3946DP6T5G

Dual Complementary General Purpose Transistor

The NST3946DP6T5G device is a spin-off of our popular SOT-23/SOT-323/SOT-563 three-leaded device. It is designed for general purpose amplifier applications and is housed in the SOT-963 six-leaded surface mount package. By putting two discrete devices in one package, this device is ideal for low-power surface mount applications where board space is at a premium.

Features

- h_{FE} , 100–300
- Low $V_{CE(sat)}$, ≤ 0.4 V
- Reduces Board Space and Component Count
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector – Emitter Voltage	V_{CEO}	40	Vdc
Collector – Base Voltage	V_{CBO}	60	Vdc
Emitter – Base Voltage	V_{EBO}	6.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Electrostatic Discharge	HBM MM	ESD Class	2 B

THERMAL CHARACTERISTICS

Characteristic (Single Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C (Note 1)	P_D	240 1.9	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	520	$^\circ\text{C}/\text{W}$
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C (Note 2)	P_D	280 2.2	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	446	$^\circ\text{C}/\text{W}$
Characteristic (Dual Heated) (Note 3)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C (Note 1)	P_D	350 2.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	357	$^\circ\text{C}/\text{W}$
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C (Note 2)	P_D	420 3.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	297	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

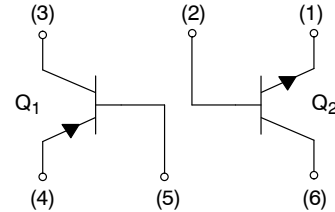
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR-4 @ 100 mm², 1 oz. copper traces, still air.
2. FR-4 @ 500 mm², 1 oz. copper traces, still air.
3. Dual heated values assume total power is sum of two equally powered channels



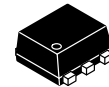
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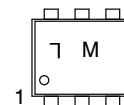
NST3946DP6T5G*

*Q1 PNP
Q2 NPN



SOT-963
CASE 527AD

MARKING DIAGRAM



L = Device Code
(180° Clockwise Rotation)
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NST3946DP6T5G	SOT-963 (Pb-Free)	8000/Tape & Reel
NSVT3946DP6T5G	SOT-963 (Pb-Free)	8000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (Note 4) (I _C = 1.0 mA _{dc} , I _B = 0) (I _C = -1.0 mA _{dc} , I _B = 0)	(NPN) (PNP)	V _{(BR)CEO}	40 -40	- -	V _{dc}
Collector–Base Breakdown Voltage (I _E = 10 μA _{dc} , I _E = 0) (I _C = -10 μA _{dc} , I _E = 0)	(NPN) (PNP)	V _{(BR)CBO}	60 -40	- -	V _{dc}
Emitter–Base Breakdown Voltage (I _E = 10 μA _{dc} , I _C = 0) (I _E = -10 μA _{dc} , I _C = 0)	(NPN) (PNP)	V _{(BR)EBO}	6.0 -5.0	- -	V _{dc}
Collector Cutoff Current (V _{CE} = 30 V _{dc} , V _{EB} = 3.0 V _{dc}) (V _{CE} = -30 V _{dc} , V _{EB} = -3.0 V _{dc})	(NPN) (PNP)	I _{CEX}	- -	50 -50	nA _{dc}
ON CHARACTERISTICS (Note 4)					
DC Current Gain (I _C = 0.1 mA _{dc} , V _{CE} = 1.0 V _{dc}) (I _C = 1.0 mA _{dc} , V _{CE} = 1.0 V _{dc}) (I _C = 10 mA _{dc} , V _{CE} = 1.0 V _{dc}) (I _C = 50 mA _{dc} , V _{CE} = 1.0 V _{dc}) (I _C = 100 mA _{dc} , V _{CE} = 1.0 V _{dc}) (I _C = -0.1 mA _{dc} , V _{CE} = -1.0 V _{dc}) (I _C = -1.0 mA _{dc} , V _{CE} = -1.0 V _{dc}) (I _C = -10 mA _{dc} , V _{CE} = -1.0 V _{dc}) (I _C = -50 mA _{dc} , V _{CE} = -1.0 V _{dc}) (I _C = -100 mA _{dc} , V _{CE} = -1.0 V _{dc})	(NPN) (PNP)	h _{FE}	40 70 100 60 30 60 80 100 60 30	- - 300 - - - - 300 - -	-
Collector–Emitter Saturation Voltage (I _C = 10 mA _{dc} , I _B = 1.0 mA _{dc}) (I _C = 50 mA _{dc} , I _B = 5.0 mA _{dc}) (I _C = -10 mA _{dc} , I _B = -1.0 mA _{dc}) (I _C = -50 mA _{dc} , I _B = -5.0 mA _{dc})	(NPN) (PNP)	V _{CE(sat)}	- - - -	0.2 0.3 -0.25 -0.4	V _{dc}
Base–Emitter Saturation Voltage (I _C = 10 mA _{dc} , I _B = 1.0 mA _{dc}) (I _C = 50 mA _{dc} , I _B = 5.0 mA _{dc}) (I _C = -10 mA _{dc} , I _B = -1.0 mA _{dc}) (I _C = -50 mA _{dc} , I _B = -5.0 mA _{dc})	(NPN) (PNP)	V _{BE(sat)}	0.65 - -0.65 -	0.85 0.95 -0.85 -0.95	V _{dc}

4. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

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ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Max	Unit
SMALL-SIGNAL CHARACTERISTICS				
Current - Gain - Bandwidth Product ($I_C = 10\text{ mAdc}$, $V_{CE} = 20\text{ Vdc}$, $f = 100\text{ MHz}$) (NPN) ($I_C = -10\text{ mAdc}$, $V_{CE} = -20\text{ Vdc}$, $f = 100\text{ MHz}$) (PNP)	f_T	200 250	- -	MHz
Output Capacitance ($V_{CB} = 5.0\text{ Vdc}$, $I_E = 0$, $f = 1.0\text{ MHz}$) (NPN) ($V_{CB} = -5.0\text{ Vdc}$, $I_E = 0$, $f = 1.0\text{ MHz}$) (PNP)	C_{obo}	- -	4.0 4.5	pF
Input Capacitance ($V_{EB} = 0.5\text{ Vdc}$, $I_C = 0$, $f = 1.0\text{ MHz}$) (NPN) ($V_{EB} = -0.5\text{ Vdc}$, $I_C = 0$, $f = 1.0\text{ MHz}$) (PNP)	C_{ibo}	- -	8.0 10.0	pF
Noise Figure ($V_{CE} = 5.0\text{ Vdc}$, $I_C = 100\text{ }\mu\text{Adc}$, $R_S = 1.0\text{ k}\Omega$, $f = 1.0\text{ kHz}$) (NPN) ($V_{CE} = -5.0\text{ Vdc}$, $I_C = -100\text{ }\mu\text{Adc}$, $R_S = 1.0\text{ k}\Omega$, $f = 1.0\text{ kHz}$) (PNP)	NF	- -	5.0 4.0	dB

SWITCHING CHARACTERISTICS

Delay Time	($V_{CC} = 3.0\text{ Vdc}$, $V_{BE} = -0.5\text{ Vdc}$) (NPN) ($V_{CC} = -3.0\text{ Vdc}$, $V_{BE} = 0.5\text{ Vdc}$) (PNP)	t_d	- -	35 35	ns
Rise Time	($I_C = 10\text{ mAdc}$, $I_{B1} = 1.0\text{ mAdc}$) (NPN) ($I_C = -10\text{ mAdc}$, $I_{B1} = -1.0\text{ mAdc}$) (PNP)	t_r	- -	35 35	
Storage Time	($V_{CC} = 3.0\text{ Vdc}$, $I_C = 10\text{ mAdc}$) (NPN) ($V_{CC} = -3.0\text{ Vdc}$, $I_C = -10\text{ mAdc}$) (PNP)	t_s	- -	275 250	ns
Fall Time	($I_{B1} = I_{B2} = 1.0\text{ mAdc}$) (NPN) ($I_{B1} = I_{B2} = -1.0\text{ mAdc}$) (PNP)	t_f	- -	50 50	

NPN TRANSISTOR

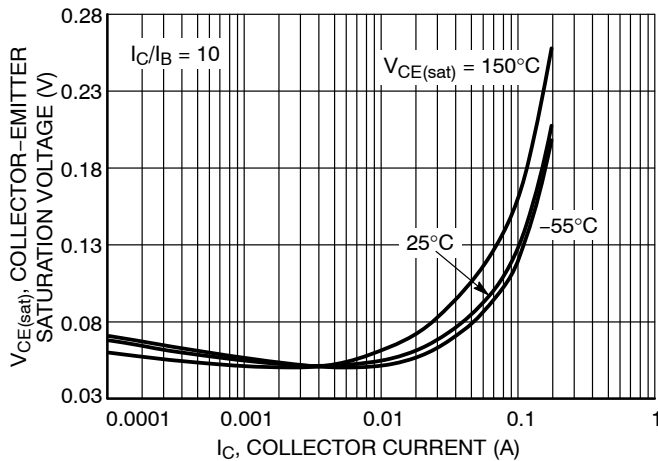


Figure 1. Collector Emitter Saturation Voltage vs. Collector Current

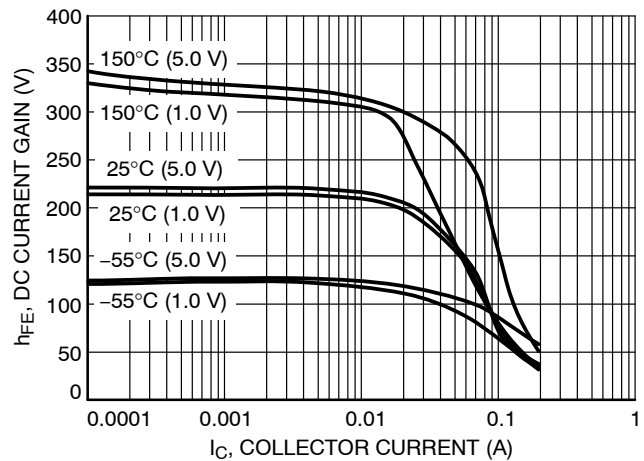


Figure 2. DC Current Gain vs. Collector Current

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NPN TRANSISTOR

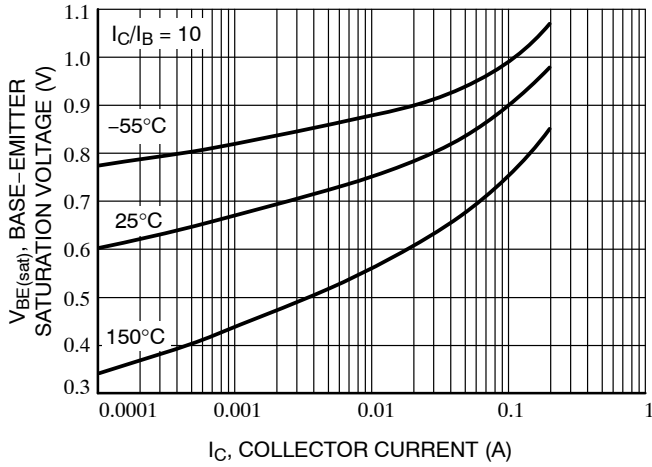


Figure 3. Base-Emitter Saturation Voltage vs. Collector Current

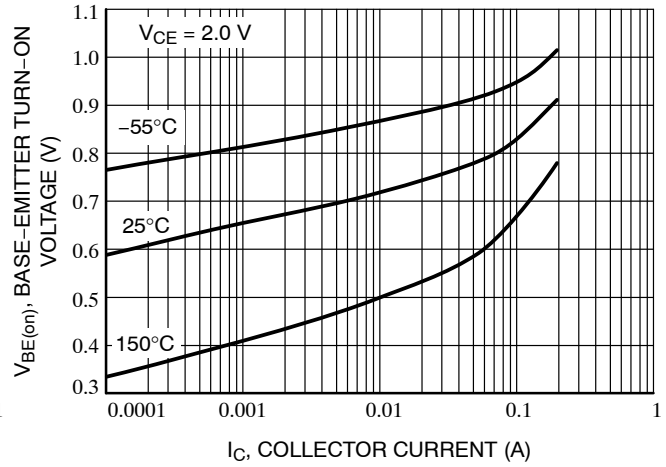


Figure 4. Base-Emitter Turn-On Voltage vs. Collector Current

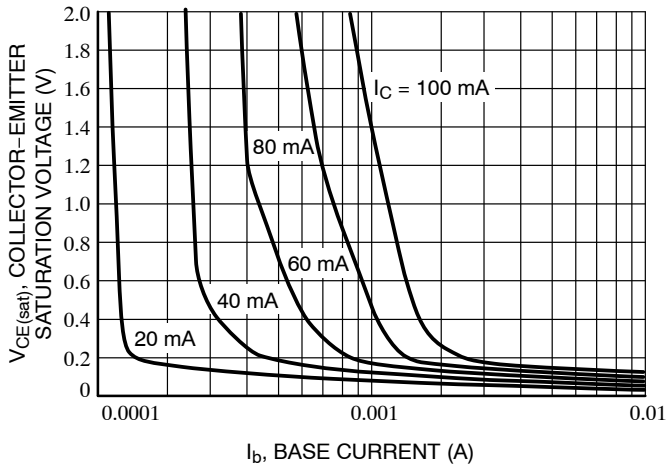


Figure 5. Saturation Region

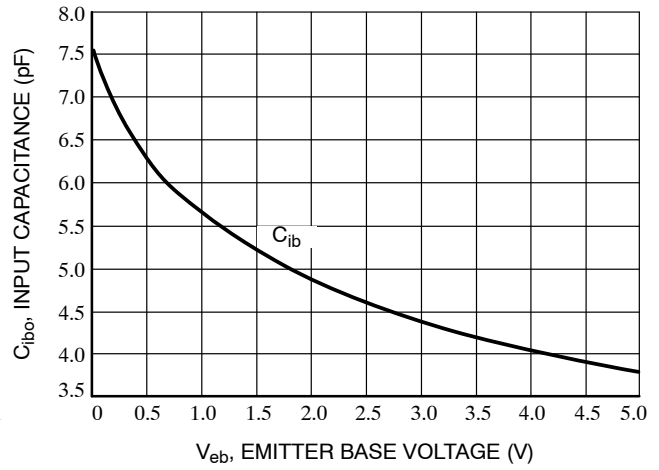


Figure 6. Input Capacitance

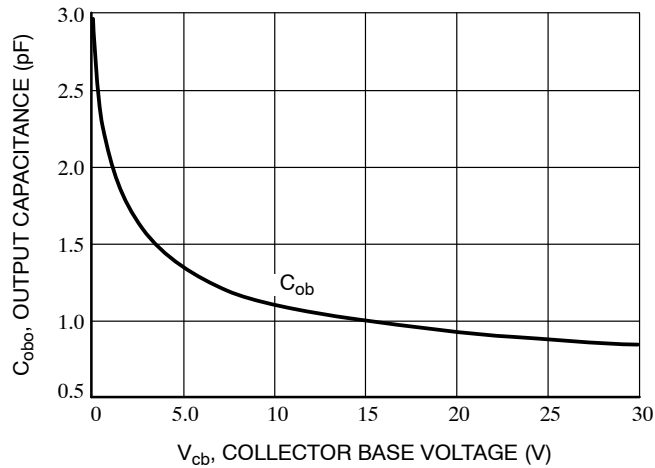


Figure 7. Output Capacitance

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PNP TRANSISTOR

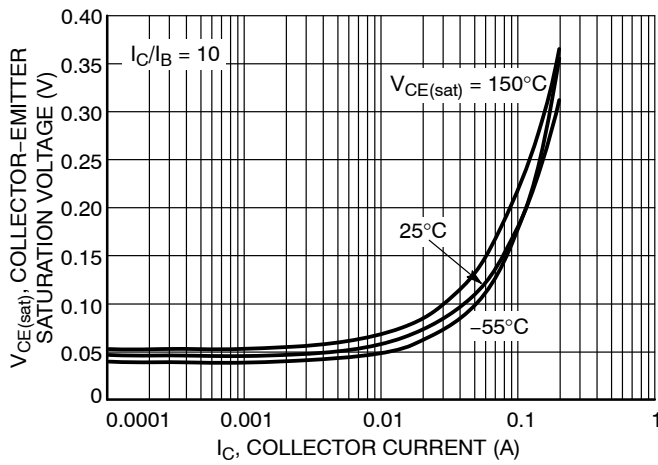


Figure 8. Collector-Emitter Saturation Voltage vs. Collector Current

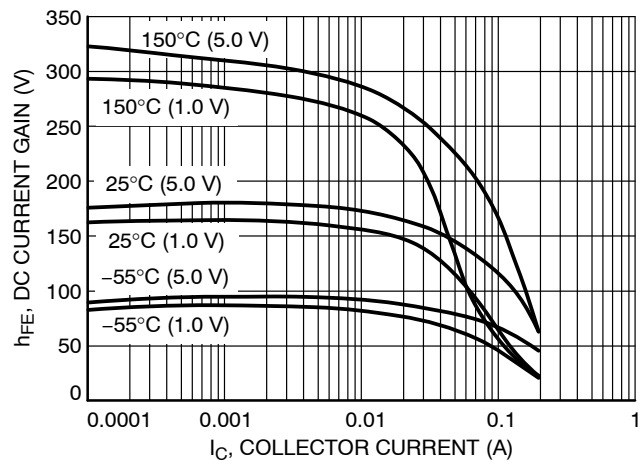


Figure 9. DC Current Gain vs. Collector Current

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PNP TRANSISTOR

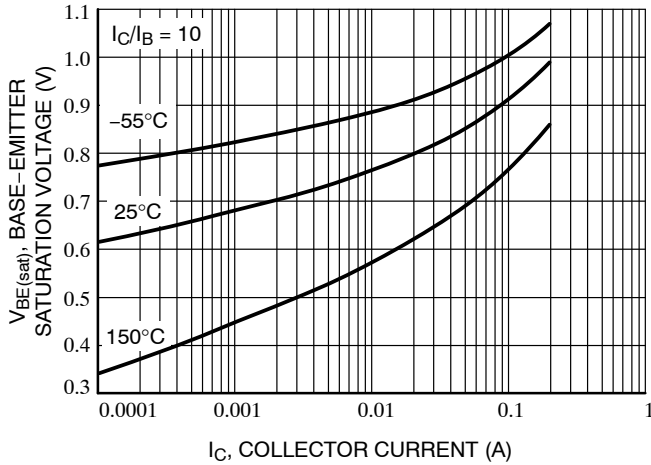


Figure 10. Base-Emitter Saturation Voltage vs. Collector Current

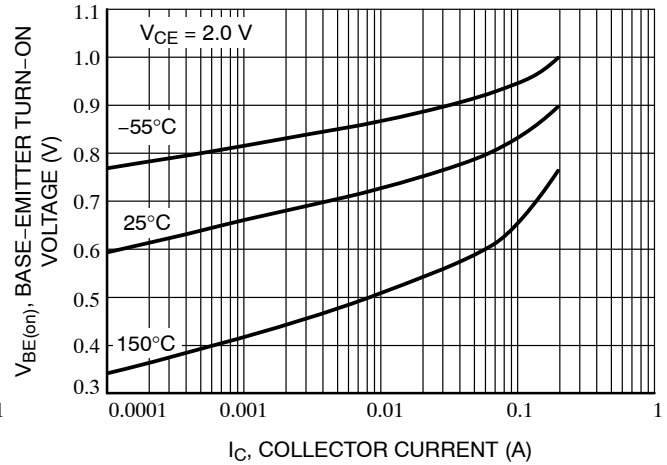


Figure 11. Base-Emitter Turn-On Voltage vs. Collector Current

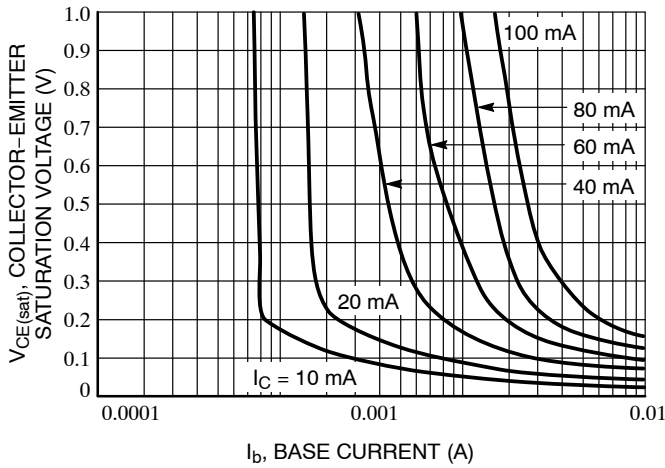


Figure 12. Saturation Region

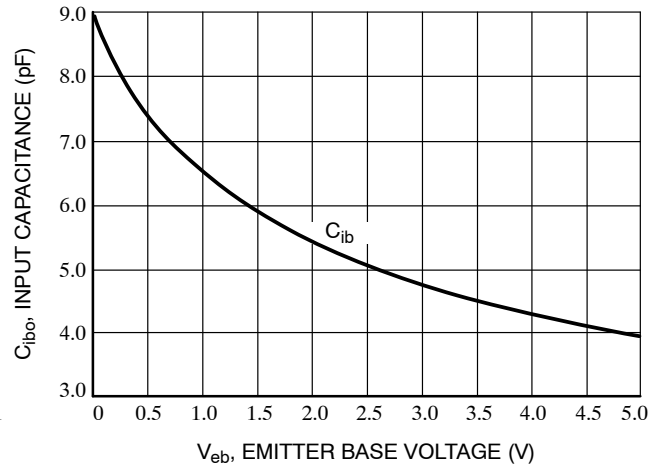


Figure 13. Input Capacitance

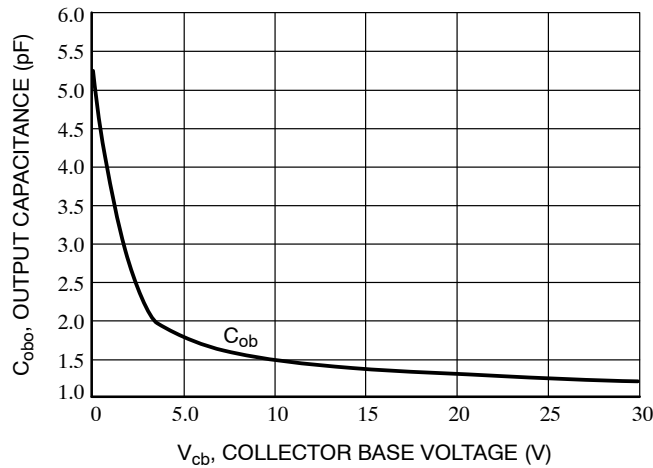
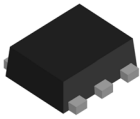


Figure 14. Output Capacitance

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

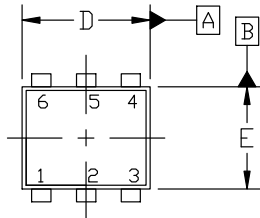


SOT-963 1.00x1.00x0.37, 0.35P
CASE 527AD
ISSUE F

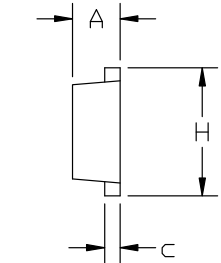
DATE 20 FEB 2024

NOTES:

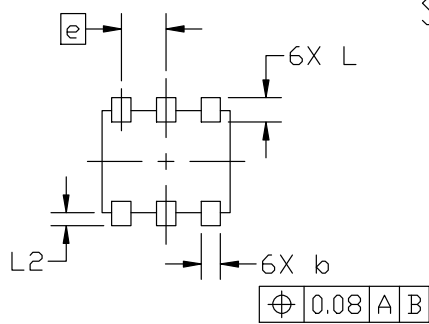
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.



TOP VIEW

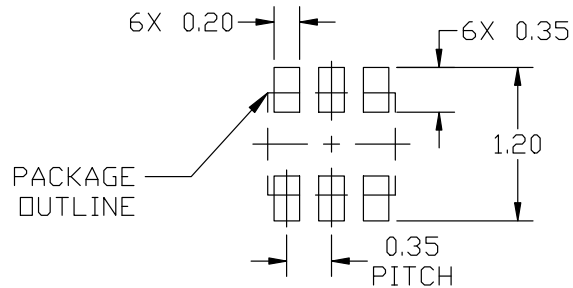


SIDE VIEW



BOTTOM VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.34	0.37	0.40
b	0.10	0.15	0.20
c	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H	0.95	1.00	1.05
L	0.19 REF		
L2	0.05	0.10	0.15



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

STYLE 1:

- PIN 1. EMITTER 1
- 2. BASE 1
- 3. COLLECTOR 2
- 4. EMITTER 2
- 5. BASE 2
- 6. COLLECTOR 1

STYLE 2:

- PIN 1. EMITTER 1
- 2. EMITTER2
- 3. BASE 2
- 4. COLLECTOR 2
- 5. BASE 1
- 6. COLLECTOR 1

STYLE 3:

- PIN 1. CATHODE 1
- 2. CATHODE 1
- 3. ANODE/ANODE 2
- 4. CATHODE 2
- 5. CATHODE 2
- 6. ANODE/ANODE 1

STYLE 4:

- PIN 1. COLLECTOR
- 2. COLLECTOR
- 3. BASE
- 4. EMITTER
- 5. COLLECTOR
- 6. COLLECTOR

STYLE 5:

- PIN 1. CATHODE
- 2. CATHODE
- 3. ANODE
- 4. ANODE
- 5. CATHODE
- 6. CATHODE

STYLE 6:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. CATHODE
- 5. CATHODE
- 6. CATHODE

STYLE 7:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. CATHODE
- 5. ANODE
- 6. CATHODE

STYLE 8:

- PIN 1. DRAIN
- 2. DRAIN
- 3. GATE
- 4. SOURCE
- 5. DRAIN
- 6. DRAIN

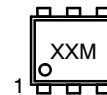
STYLE 9:

- PIN 1. SOURCE 1
- 2. GATE 1
- 3. DRAIN 2
- 4. SOURCE 2
- 5. GATE 2
- 6. DRAIN 1

STYLE 10:

- PIN 1. CATHODE 1
- 2. N/C
- 3. CATHODE 2
- 4. ANODE 2
- 5. N/C
- 6. ANODE 1

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	SOT-963 1.00x1.00x0.37, 0.35P	PAGE 1 OF 1

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