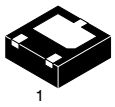
Bias Resistor Transistors (BRT)

PNP, 50 V, 100 mA

NSBAMXW Series



XDFNW3
CASE 521AC

The series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor contains a single transistor with a monolithic bias network consisting of two resistors: a series base resistor and a base−emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. They are housed in the DFN1010−3 package offering superior thermal performance. The transistor is ideal for surface mount applications where board space and reliability are at a premium.

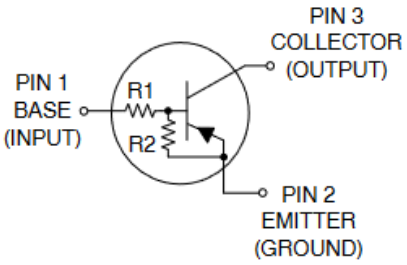
Features

- Built in Bias Resistors
- Complimentary NPN Types Available
- XDFNW3 Package Offers Low Seated Height – 0.44 mm Max
- Wettable Flank Package for Optimal Automated Optical Inspection (AOI)
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

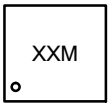
Applications

- Digital Switching
- Controlling IC Input

PIN CONNECTIONS



MARKING DIAGRAM



XX = Specific Device Code
M = Date Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Min	Max	Unit
Collector – Emitter Voltage	V_{CEO}		−50	V
Collector – Base Voltage	V_{CBO}		−50	V
Input Voltage NSBA114EMXWTBG NSBA124EMXWTBG NSBA143EMXWTBG NSBA144EMXWTBG NSBA123YMXWTBG	V_I	 −40 −40 −30 −40 −5	 +10 +10 +10 +10 +12	V
Collector Current	I_C		100	mA
Electrostatic Discharge (HBM)	ESD	Class 1B		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Power Dissipation @ T_A = 25°C (Note 1)	P_D	450	mW
Thermal Resistance, Junction−to−Ambient (Note 1)	$R_{\theta JA}$	145	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−65 to +150	°C

1. Per JESD51−7 with standard PCB footprint and 2 oz. Cu.

ORDERING INFORMATION

Device	Device−Automotive*	R1	R2	Part Marking	Package†	Shipping
NSBA114EMXWTBG	NSVBA114EMXWTBG	10	10	4X	XDFNW3 (Pb−Free)	3000 / Tape & Reel
NSBA124EMXWTBG	NSVBA124EMXWTBG	22	22	4Y		
NSBA143EMXWTBG	NSVBA143EMXWTBG	4.7	4.7	4V		
NSBA144EMXWTBG	NSVBA144EMXWTBG	47	47	4Z		
NSBA123YMXWTBG	NSVBA123YMXWTBG	2.2	10	4W		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Collector−Base Cutoff Current (V_{CB} = −50 V, I_E = 0)		I_{CBO}	–	–	−100	nA
Collector−Emitter Cutoff Current (V_{CE} = −50 V, I_B = 0)		I_{CEO}	–	–	−500	nA
Emitter−Base Cutoff Current (V_{EB} = −5 V, I_C = 0)	NSBA114E	I_{EBO}	–	–	−0.5	mA
	NSBA124E		–	–	−0.2	
	NSBA143E		–	–	−1.5	
	NSBA144E		–	–	−0.13	
	NSBA123Y		–	–	−0.7	
DC Current Gain (V_{CE} = −10.0 V, I_C = −5 mA)	NSBA114E	h_{FE}	35	–	–	
	NSBA124E		60	–	–	
	NSBA143E		15	–	–	
	NSBA144E		80	–	–	
	NSBA123Y		35	–	–	
Collector−Emitter Saturation Voltage (I_C = −10 mA, I_B = −0.3 mA)		$V_{CE(sat)}$	–	–	−0.25	V
Input Voltage (off) (V_{CE} = −5.0 V, I_C = −100 μA)	NSBA114E	$V_{I(off)}$	–	−1.2	−0.8	V
	NSBA124E		–	−1.2	−0.8	
	NSBA143E		–	−1.2	−0.5	
	NSBA144E		–	−1.2	−0.8	
	NSBA123Y		–	−0.75	−0.3	
Input Voltage (on)	NSBA114E (V_{CE} = −0.3 V, I_C = −10 mA)	$V_{I(on)}$	−2.5	−1.8	–	V
	NSBA124E (V_{CE} = −0.3 V, I_C = −5 mA)		−2.5	−1.7	–	
	NSBA143E (V_{CE} = −0.3 V, I_C = −20 mA)		−3	−2.4	–	
	NSBA144E (V_{CE} = −0.3 V, I_C = −5 mA)		−3	−1.6	–	
	NSBA123Y (V_{CE} = −0.3 V, I_C = −20 mA)		−2.5	−1.15	–	
Output Voltage (on) (V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ)		V_{OL}	–	–	0.2	V
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)		V_{OH}	4.9	–	–	V
Bias Resistor (R1)	NSBA114E	R1	7	10	13	kΩ
	NSBA124E		15.4	22	28.6	
	NSBA143E		3.3	4.7	6.1	
	NSBA144E		32.9	47	61.1	
	NSBA123Y		1.54	2.2	2.86	
Resistor Ratio	NSBA114E	R1/R2	0.8	1	1.2	
	NSBA124E		0.8	1	1.2	
	NSBA143E		0.8	1	1.2	
	NSBA144E		0.8	1	1.2	
	NSBA123Y		0.18	0.22	0.27	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS (Ref NSBA124E)

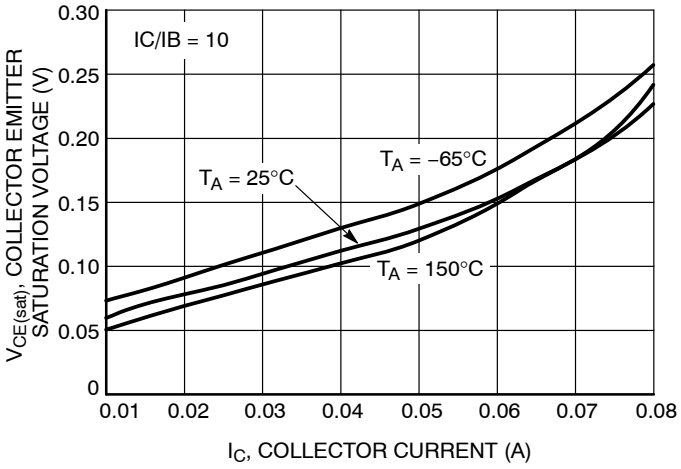


Figure 1. $V_{CE(sat)}$ vs. I_C

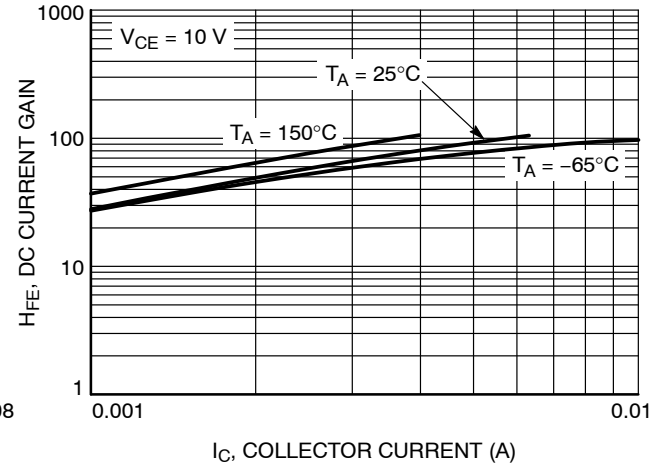


Figure 2. DC Current Gain

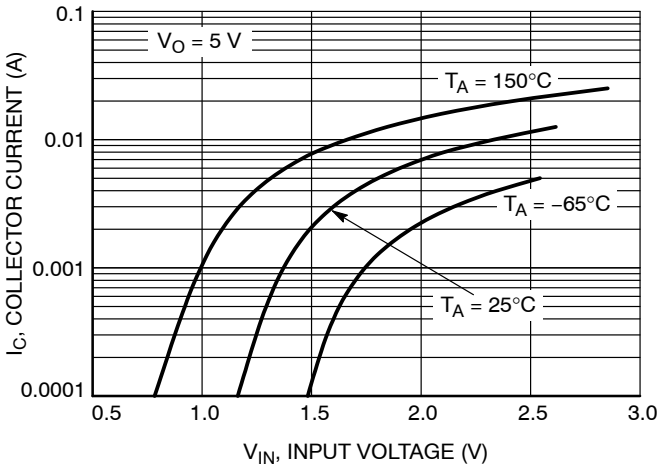


Figure 3. Output Current vs. Input Voltage

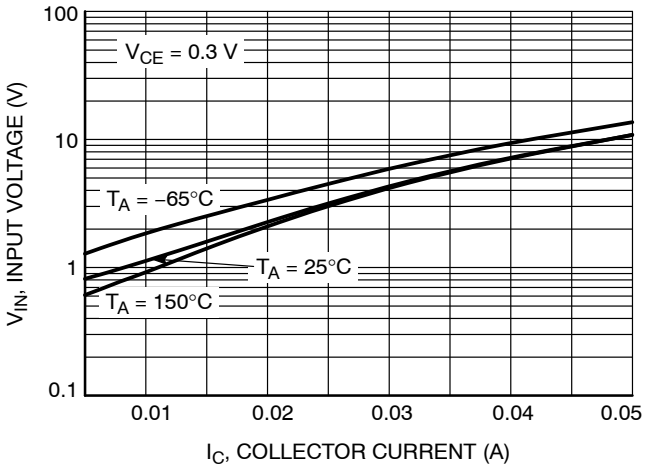


Figure 4. Input Voltage vs. Output Current

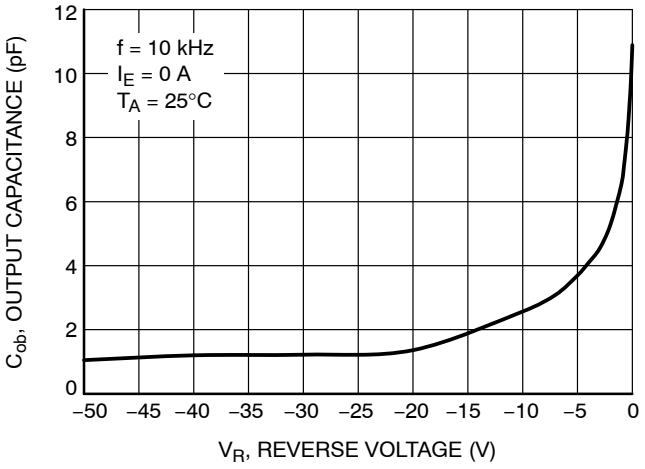


Figure 5. Output Capacitance

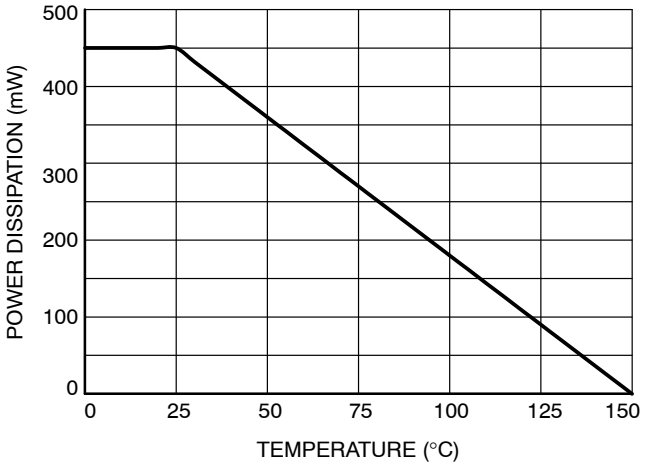


Figure 6. Derating Curve

TYPICAL CHARACTERISTICS

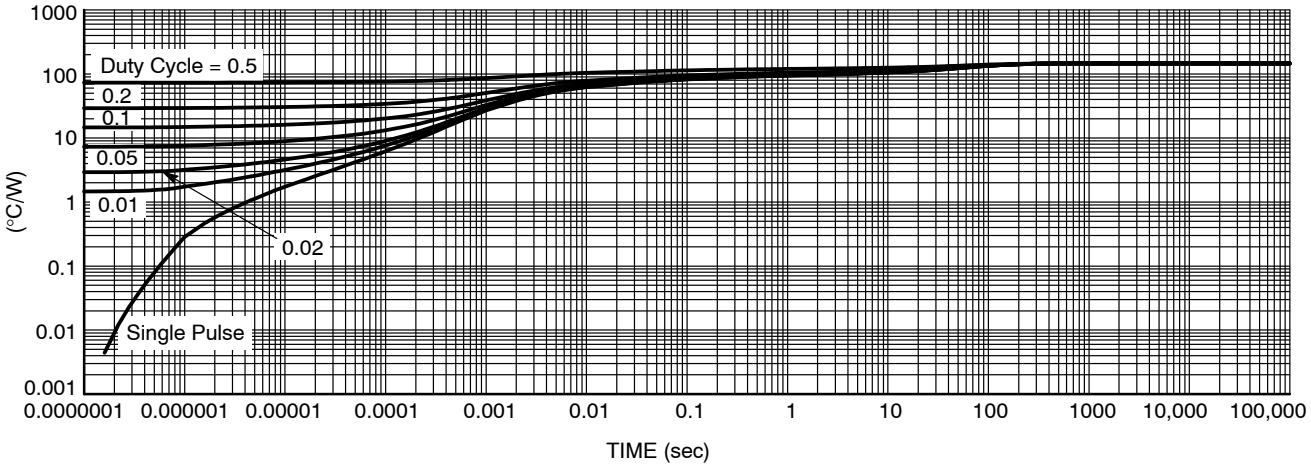
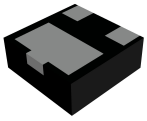
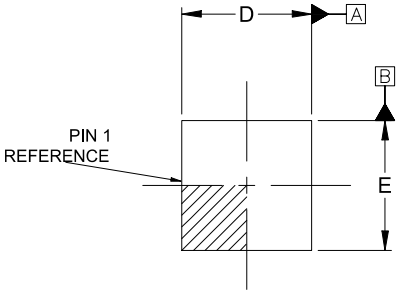


Figure 7. Transient Thermal Impedance from Junction−to−Ambient as a Function of Pulse Duration

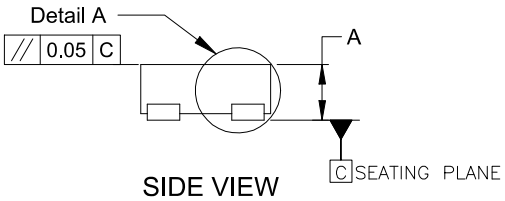


XDFNW3 1.00x1.00x0.38 0.65P
CASE 521AC
ISSUE B

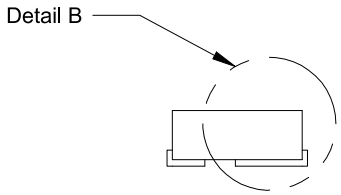
DATE 07 MAY 2024



TOP VIEW



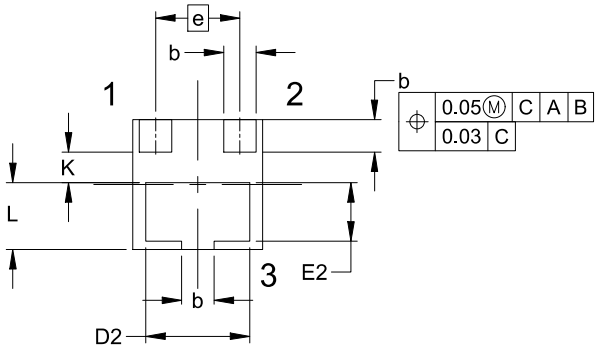
SIDE VIEW



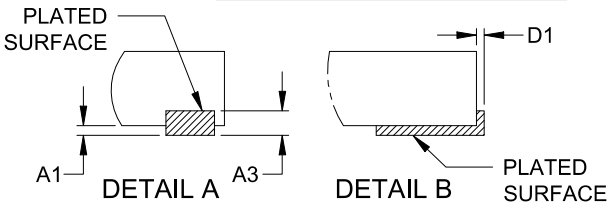
END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS

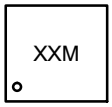
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.32	0.38	0.44
A1	0.00	---	0.04
A3		0.125 REF	
b	0.20	0.25	0.30
D	0.90	1.00	1.10
D1	0.00	---	0.04
D2	0.75	0.80	0.85
E	0.90	1.00	1.10
E2	0.40	0.45	0.50
e		0.65 BSC	
L	0.465	0.515	0.565
K		0.23 REF	



BOTTOM VIEW

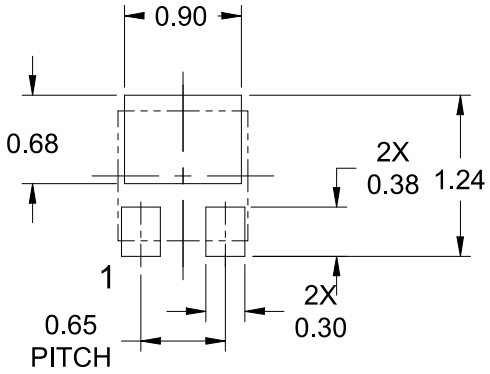


GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ONSEMI Soldering and Mounting Techniques Reference Manual, S●LDERRM/D.

DOCUMENT NUMBER:	**98AON11341H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**XDFNW3 1.00x1.00x0.38 0.65P**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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