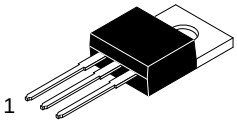
PNP Epitaxial Silicon Transistor

KSB596



1. Base
2. Collector
3. Emitter

TO−220−3LD
CASE 340AT

Features

- Complement to KSD526
- This is a Pb−Free Device

Applications

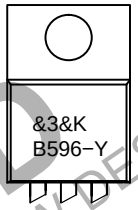
- Power Amplifier Applications

ABSOLUTE MAXIMUM RATINGS* (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{CBO}	Collector−Base Voltage	−80	V
V_{CEO}	Collector−Emitter Voltage	−80	V
V_{EBO}	Emitter−Base Voltage	−5	V
I_C	Collector Current (DC)	−4	A
I_B	Base Current	−0.4	A
P_C	Collector Dissipation (T_C = 25°C)	30	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	−55 ~ 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*These ratings are limiting values above which the serviceability of any semiconductor device may by impaired.

MARKING DIAGRAM



&3 = Date Code
&K = Lot Traceability Code
B596−Y = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
KSB596YTU	TO−220−3LD (Pb−Free)	1000 Units / Tube

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Characteristic	Test Condition	Min	Typ	Max	Unit
BV_{CEO}	Collector−Emitter Breakdown Voltage	I_C = −50 mA, I_B = 0	−80			V
BV_{EBO}	Emitter−Base Breakdown Voltage	I_E = −10 mA, I_C = 0	−5			V
I_{CBO}	Collector Cut−off Current	V_{CB} = −80 V, I_E = 0			−70	μA
I_{EBO}	Emitter Cut−off Current	V_{EB} = −5 V, I_C = 0			−100	μA
h_{FE1} h_{FE2}	DC Current Gain	V_{CE} = −5 V, I_C = −0.5 A V_{CE} = −5 V, I_C = −3 A	40 15		240	
V_{CE}(sat)	Collector−Emitter Saturation Voltage	I_C = −3 A, I_B = −0.3 A		−1	−1.7	V
V_{BE}(on)	Base−Emitter On Voltage	V_{CE} = −5 V, I_C = −3 A		−1	−1.5	V
f_T	Current Gain Bandwidth Product	V_{CE} = −5 V, I_C = −0.5 A	3			MHz
C_{cb}	Collector Output Capacitance	V_{CB} = −10 V, I_E = 0, f = 1 MHz		130		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

h_{FE} CLASSIFICATION

Classification	R	O	Y
h_{FE}	40 ~ 80	70 ~ 140	120 ~ 240

TYPICAL CHARACTERISTICS

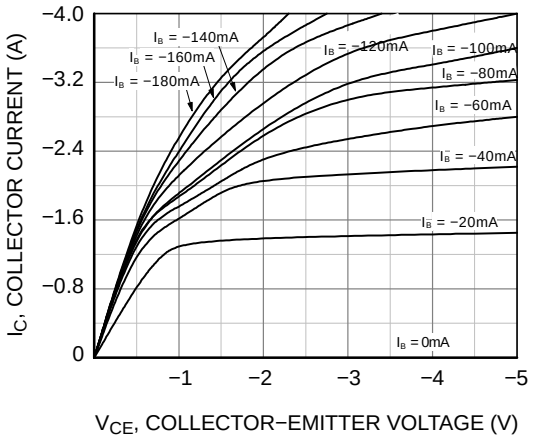


Figure 1. Static Characteristic

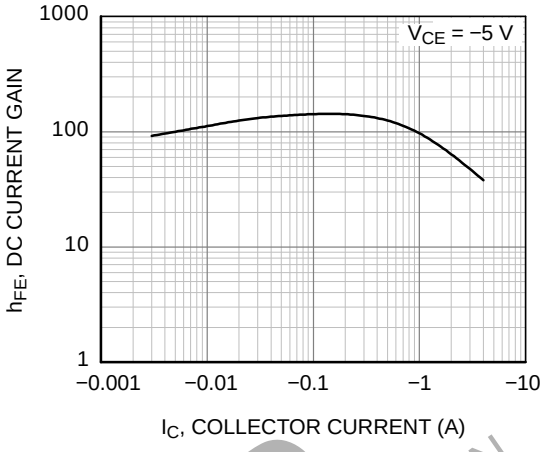


Figure 2. DC Current Gain

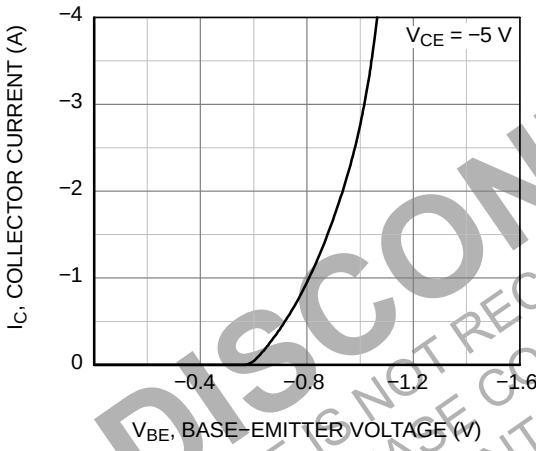


Figure 3. Base−Emitter Saturation Voltage

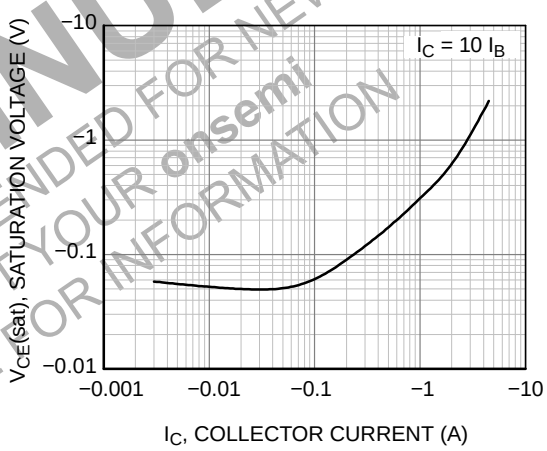


Figure 4. Collector−Emitter Saturation Voltage

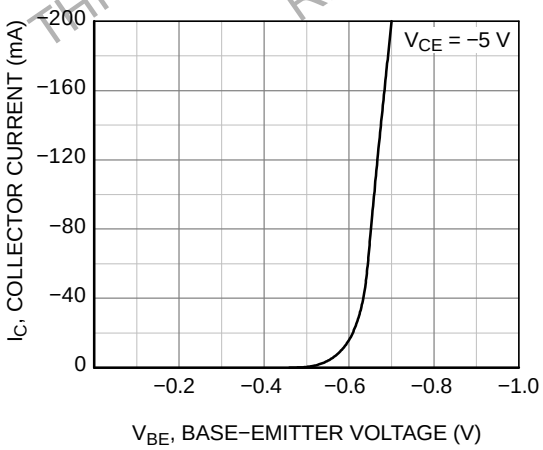


Figure 5. Base−Emitter On Voltage

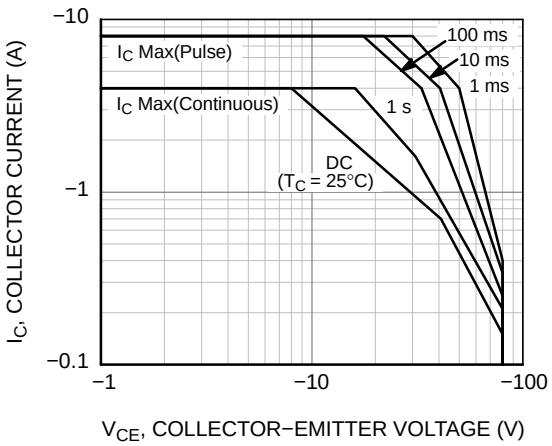


Figure 6. Safe Operating Area

TYPICAL CHARACTERISTICS (Continued)

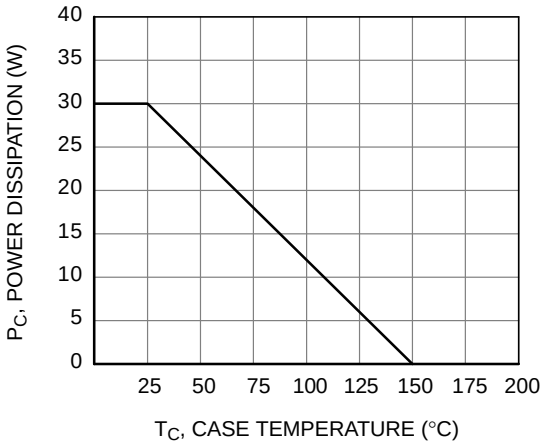


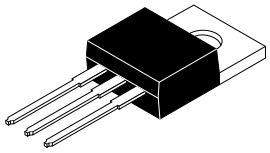
Figure 7. Power Derating

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−220−3LD
CASE 340AT
ISSUE A

DATE 03 OCT 2017



Scale 1:1

NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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