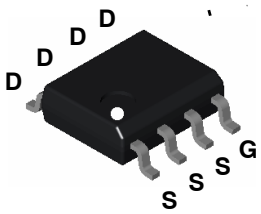
MOSFET – N-Channel POWERTRENCH®

30 V, 8.5 A, 23 mΩ

FDS8884



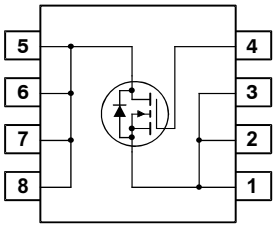
SOIC8,
CASE 751EB

Description

This N−Channel MOSFET has been Designed Specifically to improve the overall efficiency of DC/DC Converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(on)}$ and fast switching speed.

Features

- Max $R_{DS(on)}$ = 23 mΩ at V_{GS} = 10 V, I_D = 8.5 A
- Max $R_{DS(on)}$ = 30 mΩ at V_{GS} = 4.5 V, I_D = 7.5 A
- Low Gate Charge
- 100% R_G Tested
- These Device is Pb−Free and RoHS Compliant



MOSFET MAXIMUM RATINGS T_A = 25°C unless otherwise noted

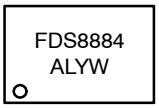
Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (Note 1a) Pulsed	8.5 40	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	32	mJ
P_D	Power Dissipation T_C = 25°C	2.5	W
	Derate Above 25°C	20	mW/°C
T_J, T_{stg}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Ambient (Note1a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Case (Note 1)	25	

MARKING DIAGRAM



FDS8884 = Specific Device Code
A = Assembly Location
L = Lot Traceability Code
YW = Date Code (Year and Week)

ORDERING INFORMATION

Device	Package	Shipping†
FDS8884	SO−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

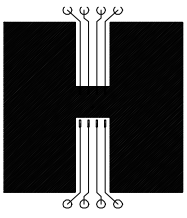
ELECTRICAL CHARACTERISTICS T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	23	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V V_{GS} = 0 V, T_J = 125°C	–	–	1 250	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V	–	–	±100	nA
On Characteristics (Note 3)						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.2	1.7	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 380 μA, Referenced to 25°C	–	−4.9	–	mV/°C
$R_{DS(on)}$	Drain to Source On−Resistance	V_{GS} = 10 V, I_D = 8.5 A	–	19	23	mΩ
		V_{GS} = 4.5 V, I_D = 7.5 A	–	23	30	
		V_{GS} = 10 V, I_D = 8.5 A, T_J = 125°C	–	26	32	
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	–	475	635	pF
C_{oss}	Output Capacitance		–	100	135	pF
C_{rss}	Reverse Transfer Capacitance		–	65	100	pF
R_g	Gate Resistance	f = 1 MHz	–	0.9	1.6	Ω
Switching Characteristics (Note 3)						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 15 V, I_D = 8.5 A, V_{GS} = 10 V, R_{GS} = 32 Ω	–	5	10	ns
t_r	Rise Time		–	9	18	ns
$t_{d(off)}$	Turn−Off Delay Time		–	42	68	ns
t_f	Fall Time		–	21	34	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 8.5 A	–	9.2	13	nC
Q_g	Total Gate Charge	V_{DS} = 15 V, V_{GS} = 5 V, I_D = 8.5 A	–	5.0	7	nC
Q_{gs}	Gate to Source Gate Charge		–	1.5	–	nC
Q_{gd}	Gate to Drain Charge		–	2.0	–	nC
Drain−Source Diode Characteristics and Maximum Ratings						
V_{SD}	Source to Drain Diode Forward Voltage	I_{SD} = 8.5 A	–	0.9	1.25	V
		I_{SD} = 2.1 A	–	0.8	1.0	V
t_{rr}	Reverse Recovery Time	I_F = 8.5 A, di/dt = 100 A/μs	–	–	33	ns
Q_{rr}	Reverse Recovery Charge		–	–	20	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

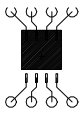
NOTES:

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

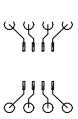


Scale 1 : 1 on letter size paper

a).50 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b).105 °C/W when mounted on a 0.4 in^2 pad of 2 oz copper.



c).125 °C/W when mounted on a minimum pad

2. Starting T_J = 25°C, L = 1 mH, I_{AS} = 8 A, V_{DD} = 27 V, V_{GS} =10 V.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

(T_J = 25 °C unless otherwise noted)

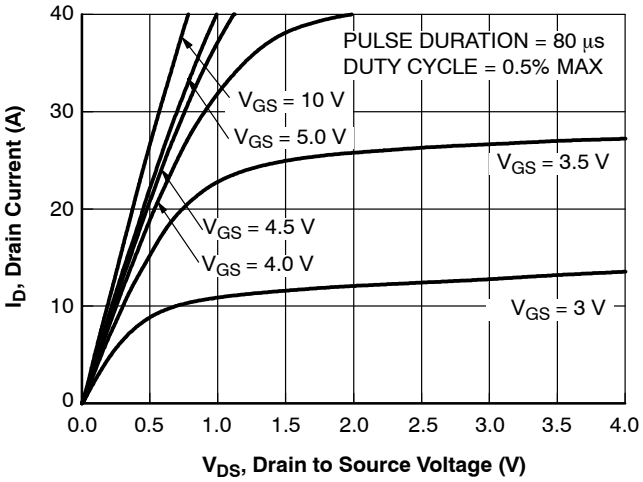


Figure 1. On−Region Characteristics

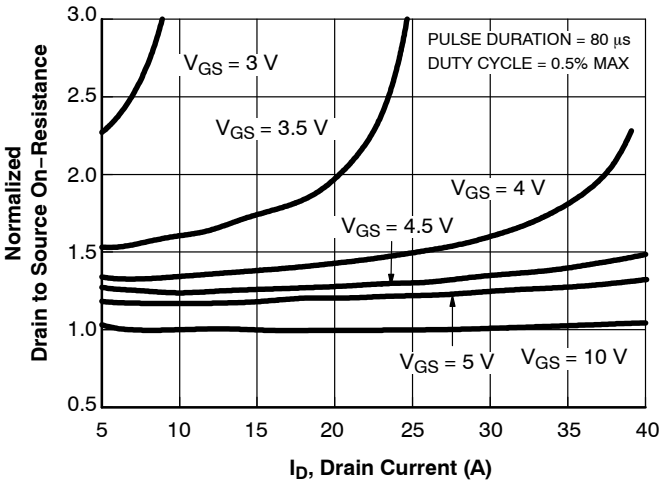


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

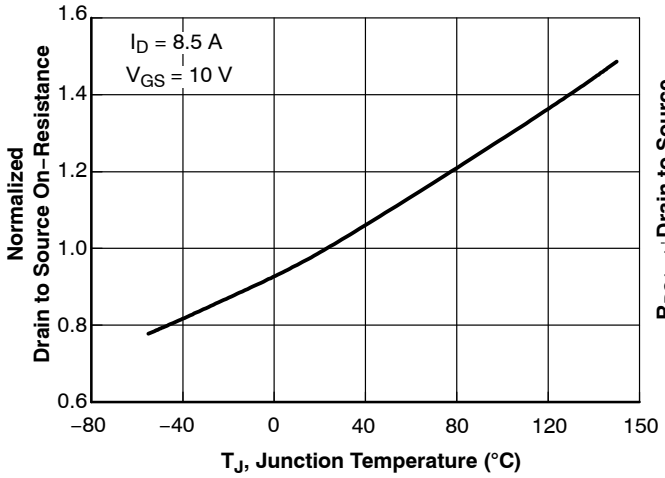


Figure 3. Normalized On−Resistance vs Junction Temperature

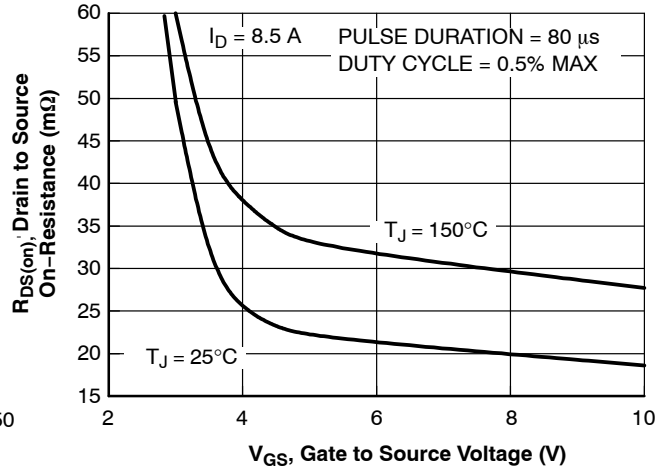


Figure 4. On−Resistance vs Gate to Source Voltage

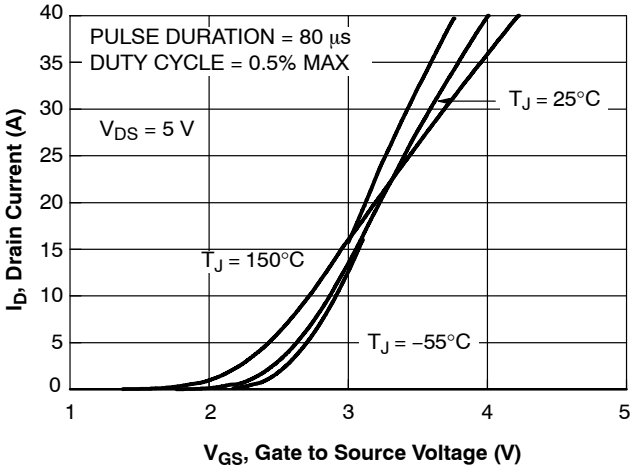


Figure 5. Transfer Characteristics

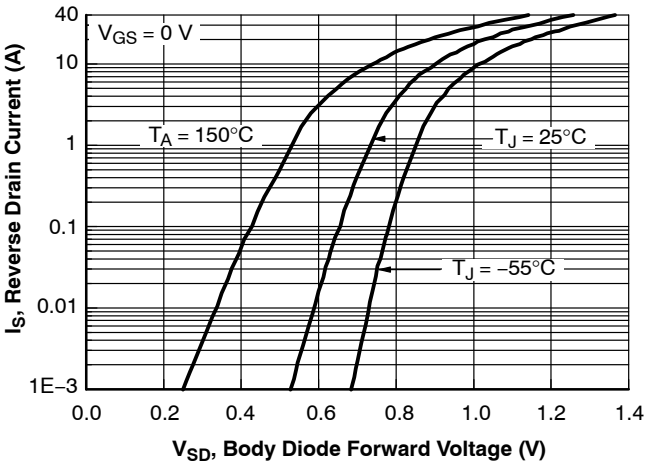


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS

(T_J = 25 °C unless otherwise noted) (CONTINUED)

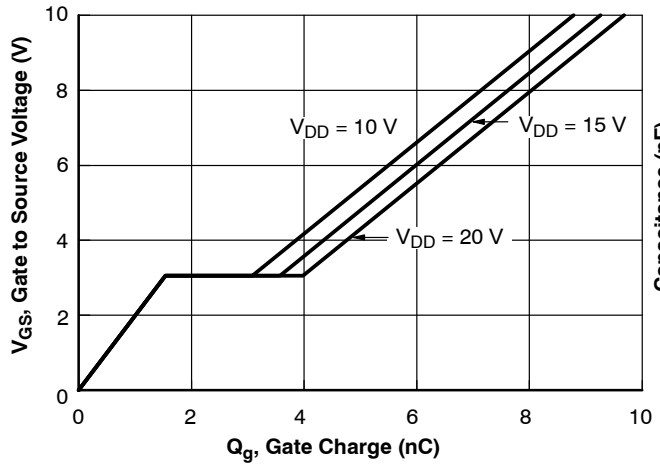


Figure 7. Gate Charge Characteristics

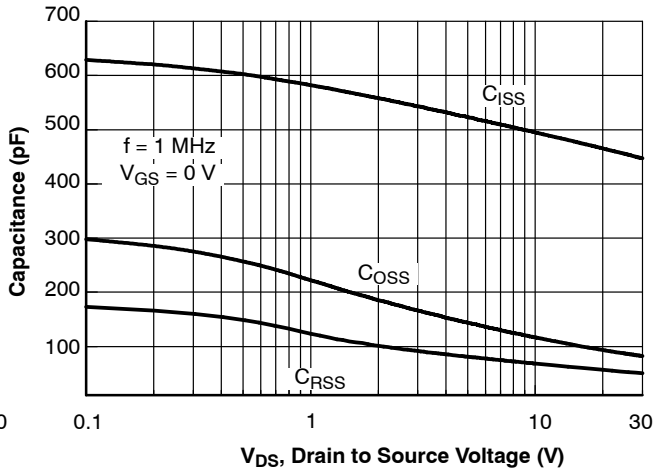


Figure 8. Capacitance vs Drain to Source Voltage

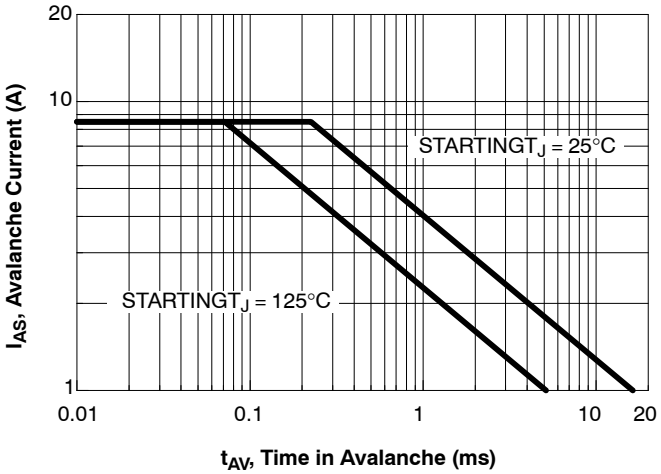


Figure 9. Unclamped Inductive Switching Capability

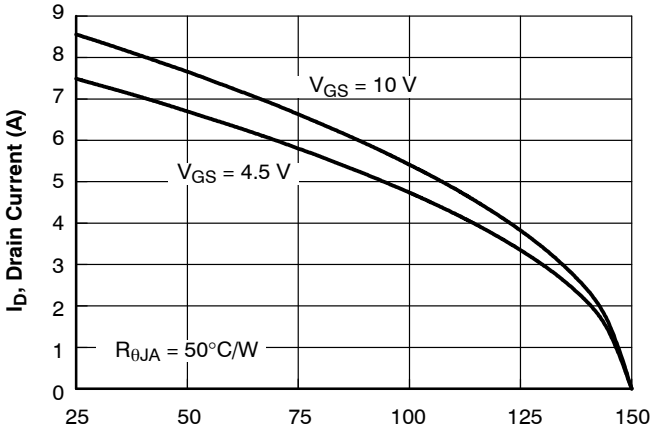


Figure 10. Maximum Continuous Drain Current vs. Ambient Temperature

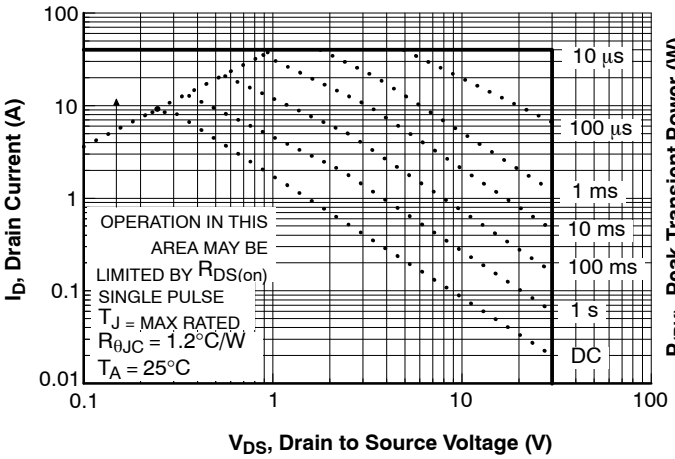


Figure 11. Forward Bias Safe Operating Area

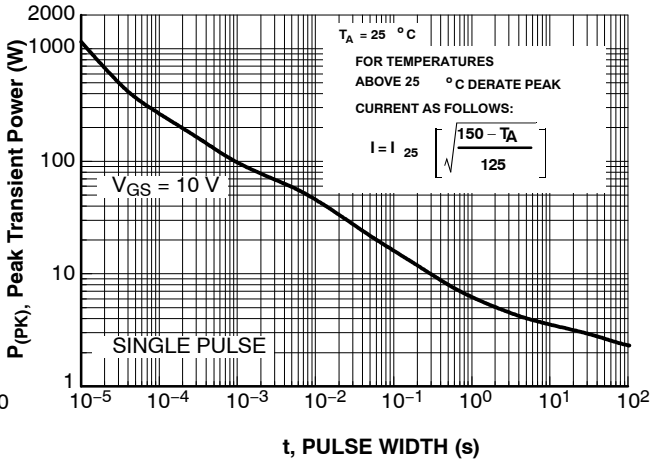


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

(T_J = 25 °C unless otherwise noted) (CONTINUED)

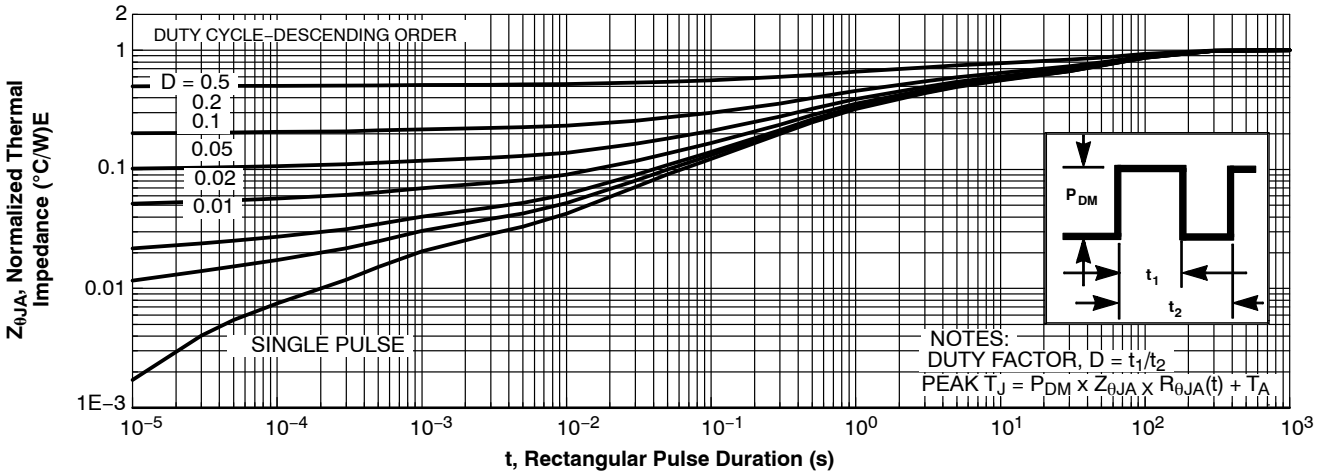


Figure 13. Transient Thermal Response Curve

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CASE 751EB
ISSUE A

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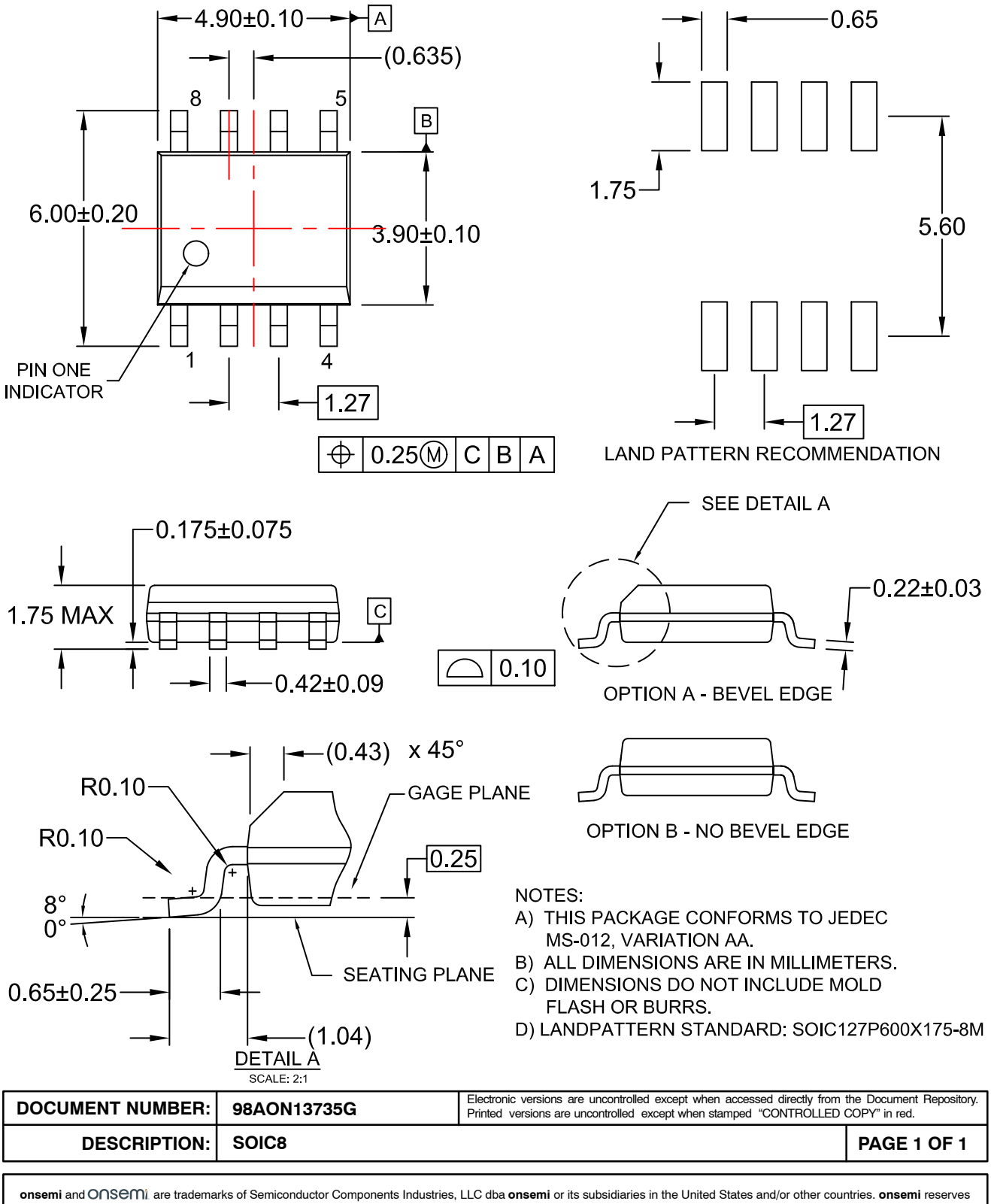

NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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