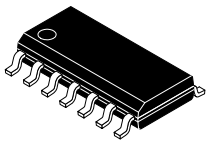
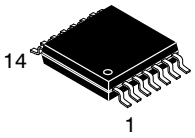
Low Voltage Quad Buffer with 5 V Tolerant Inputs and Outputs

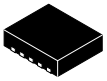
74LCX125



SOIC14,
CASE 751EF



TSSOP−14, WB
CASE 948G



QFN14, 3.0X2.5, 0.5P
CASE 510CB

Description

The LCX125 contains four independent non−inverting buffers with 3−STATE outputs. The inputs tolerate Voltages up to 7 V Allowing the interface of 5 V Systems to 3 V Systems.

The 74LCX125 is fabricated with an advanced CMOS technology to achieve high Speed operation while Maintaining CMOS Low Power Dissipation.

Features

- 5 V Tolerant Inputs and Outputs
- 2.3 V–3.6 V V_{CC} Specifications Provided
- 6.0 ns t_{PD} max. (V_{CC} = 3.3 V), 10 μA I_{CC} max.
- Power Down High Impedance Inputs and Outputs
- Supports Live Insertion/Withdrawal*
- ±24 mA Output Drive (V_{CC} = 3.0 V)
- Latch−up Performance Exceeds JEDEC 78 Conditions
- ESD Performance:
  - Human body model > 2000 V
  - Machine model > 100 V
- Leadless DQFN Package

*To ensure the High−Impedance State During Power up or down, $\overline{OE}$ Should be tied to V_{CC} through a pull−up resistor: the minimum value of the resistor is determined by the current−sourcing capability of the driver.

MARKING DIAGRAM

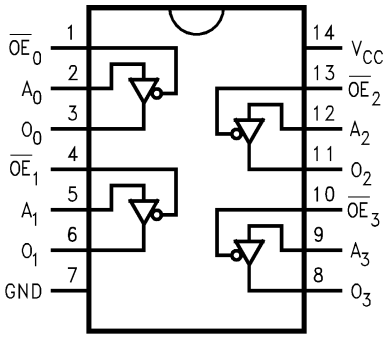
Z	= Assembly Plan Code
XY	= Date Code (Year & Week)
KK	= Lot Run Traceability Code
LCX125	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

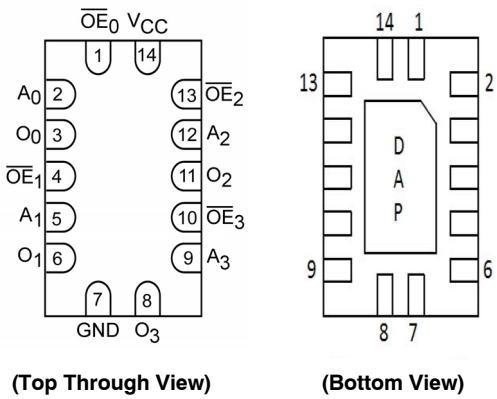
Connection Diagrams

Pin Assignments for SOIC, SOP, and TSSOP



(Top View)

Pad Assignments for DQFN



(Top Through View) **(Bottom View)**

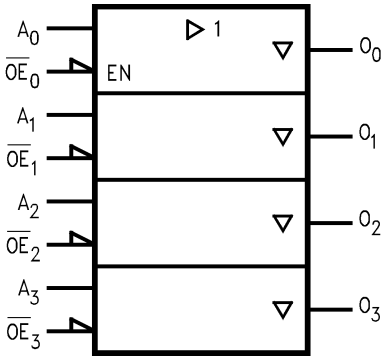
Pin Description

Pin Names	Description
A_n	Inputs
$\overline{OE}_n$	Output Enable Inputs
On	Outputs
DAP	No Connect

Note: DAP (Die Attach Pad)

Logic Symbol

IEEE/IEC



Truth Table

Inputs		Output
$\overline{OE}_n$	A_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level

L = HIGH Voltage Level

Z = HIGH Impedance

X = Immaterial

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply Voltage	−0.5 to +7.0	V
V_I	DC Input Voltage	−0.5 to +7.0	V
V_O	DC Output Voltage, − Output in 3−STATE − Output in HIGH or LOW State (Note 1)	 −0.5 V to +7.0 −0.5 V to V_{CC} + 0.5	 V V
I_{IK}	DC Input Diode Current, V_I < GND	−50	mA
I_{OK}	DC Input Diode Current − VO < GND − VO > V_{CC}	 −50 +50	 mA mA
I_O	DC Output Source/Sink Current	±50	mA
I_{CC}	DC Supply Current per Supply Pin	±50	mA
I_{GND}	DC Ground Current per Ground Pin	±100	mA
T_{STG}	Storage Temperature	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. I_O Absolute Maximum Rating must be observed.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage − Operating − Data Retention	 2.0 1.5	 3.6 3.6	V
V_I	Input Voltage	0	5.5	V
V_O	Output Voltage − HIGH or LOW State − 3−STATE	 0 0	 V_{CC} 5.5	V
I_{OH} / I_{OL}	Common−mode Input Voltage − V_{CC} = 3.0 V − 3.6 V − V_{CC} = 2.7 V − 3.0 V − V_{CC} = 2.3 V − 2.7 V		 ±24 ±12 ±8	mA
T_A	Free−Air Operating Temperature	−40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, V_{IN} = 0.8 V − 2.0 V, V_{CC} = 3.0 V	0	10	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
2. Unused inputs must be held HIGH or LOW. They may not float..

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Test Conditions	T_A = −40°C to +85°C		Unit
				Min.	Max.	
V_{IH}	HIGH Level Input Voltage	2.3–2.7		1.7		V
		2.7–3.6		2.0		
V_{IL}	LOW Level Input Voltage	2.3–2.7		−	0.7	V
		2.7–3.6		−	0.8	
V_{OH}	HIGH Level Output Voltage	2.3–3.6	I_{OH} = −100 μA	V_{CC} − 0.2	−	V
		2.3	I_{OH} = −8 mA	1.8	−	
		2.7	I_{OH} = −12 mA	2.2	−	
		3.0	I_{OH} = −18mA	2.4	−	
			I_{OH} = −24 mA	2.2	−	

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	V_{CC} (V)	Test Conditions	T_A = –40°C to +85°C		Unit
				Min.	Max.	
V_{OL}	LOW Level Output Voltage	2.3–3.6	I_{OL} = 100 μA	–	0.2	V
		2.3	I_{OL} = 8 mA	–	0.6	
		2.7	I_{OL} = 12 mA	–	0.4	
		3.0	I_{OL} = 16 mA	–	0.4	
			I_{OL} = 24 mA	–	0.55	
I_I	Input Leakage Current	2.3–3.6	0 ≤ V_I ≤ 5.5 V	–	±5.0	μA
I_{OZ}	3–STATE Output Leakage	2.3–3.6	0 ≤ V_O ≤ 5.5 V, V_I = V_{IH} or VIL	–	±5.0	μA
IO_{FF}	Power–Off Leakage Current	0	V_I or V_O = 5.5 V	–	10	μA
I_{CC}	Quiescent Supply Current	2.3–3.6	VI = V_{CC} or GND	–	10	μA
			3.6 V ≤ V_I, V_O ≤ 5.5 V (Note 3)	–	±10	
ΔI_{CC}	Increase in I_{CC} per Input	2.3–3.6	V_{IH} = V_{CC} – 0.6 V	–	500	μA

3. Outputs disabled or 3–STATE only.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	TA = –40°C to +85°C, R_L = 500 Ω						Unit
		V_{CC} = 3.3 V ± 0.3 V, C_L = 50 pF		V_{CC} = 2.7 V, C_L = 50 pF		V_{CC} = 2.5 V ± 0.2 V, C_L = 30 pF		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay	1.5	6.0	1.5	6.5	1.5	7.2	ns
t_{PZL}, t_{PZH}	Output Enable Time	1.5	7.0	1.5	8.0	1.5	9.1	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	1.5	6.0	1.5	7.0	1.5	7.2	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 4)	–	1.0	–	–	–	–	ns

4. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}).

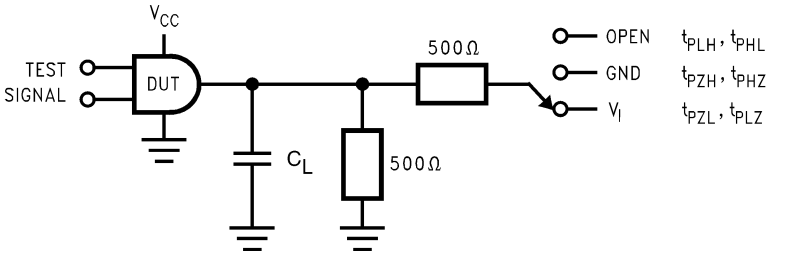
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Test Conditions	T_A = 25°C	Unit
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	3.3	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	0.8	V
		2.5	C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	0.6	
V_{OLV}	Quiet Output Dynamic Peak V_{OL}	3.3	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	–0.8	V
		2.5	C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	–0.6	

CAPACITANCE

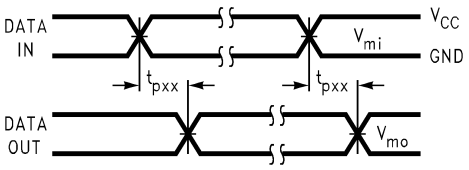
Symbol	Parameter	Test Conditions	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0 V or V_{CC}	7.0	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8.0	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}, f = 10 MHz	25.0	pF

AC LOADING AND WAVEFORMS (GENERIC FOR LCX FAMILY)

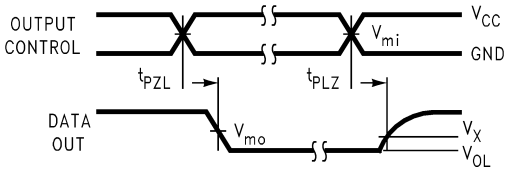


Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3 V V_{CC} x 2 at V_{CC} = 2.5 ± 0.2 V
t_{PZH}, t_{PHZ}	GND

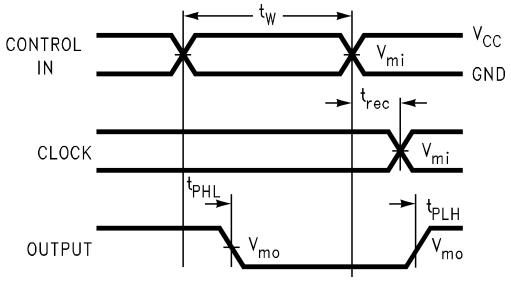
Figure 1. AC Test Circuit (C_L includes probe and jig capacitance)



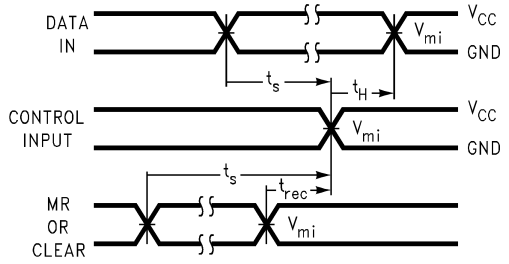
Waveform for Inverting and Non−Inverting Functions



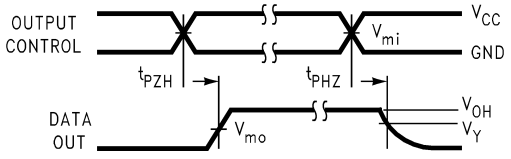
3−STATE Output High Enable and Disable Times for Logic



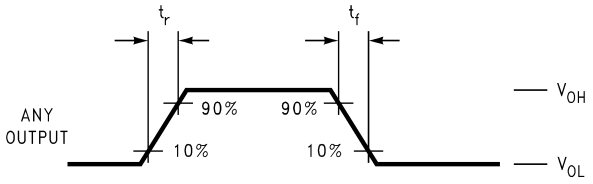
Propagation Delay. Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3−STATE Output Low Enable and Disable Times for Logic



t_{rise} and t_{fall}

Symbol	V_{CC}		
	3.3 V + 0.3 V	2.7 V	2.5 V + 0.2 V
V_{mi}	1.5 V	1.5 V	$V_{CC}/2$
V_{mo}	1.5 V	1.5 V	$V_{CC}/2$
V_x	V_{OL} + 0.3 V	V_{OL} + 0.3 V	V_{OL} + 0.15 V
V_y	V_{OH} − 0.3 V	V_{OH} − 0.3 V	V_{OH} − 0.15 V

Figure 2. Waveforms (Input Characteristics; f = 1 MHz, t_r = t_f = 3 ns)

SCHEMATIC DIAGRAM (GENERIC FOR LCX FAMILY)

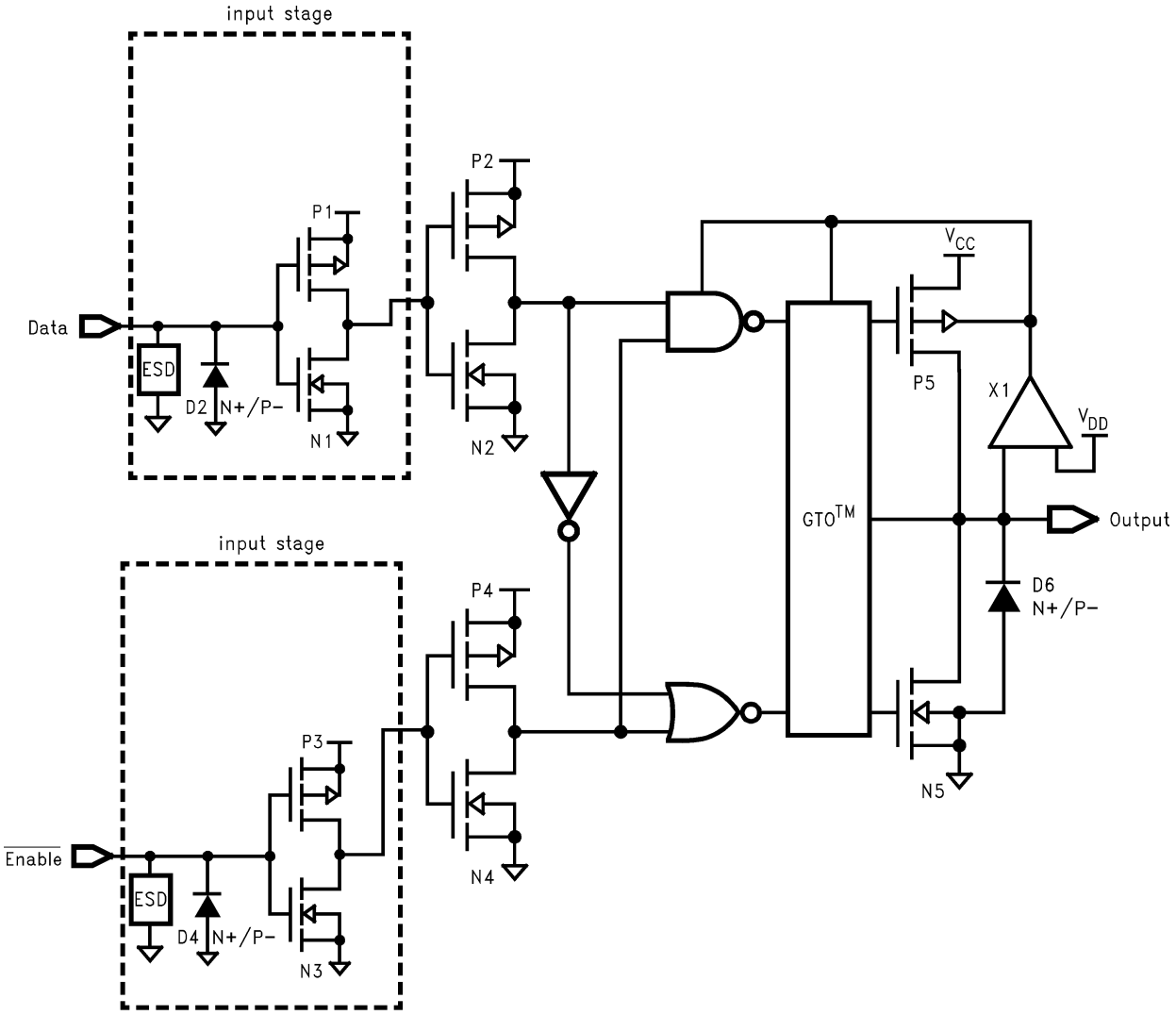


Figure 3. Schematic Diagram

ORDERING INFORMATION

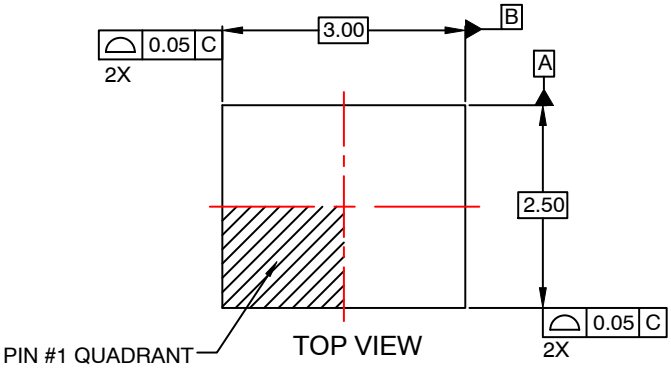
Product Number	Package	Shipping†
74LCX125M	SOIC−14 (Pb−Free/Halide Free)	1150 Units / Tube
74LCX125MX	SOIC−14 (Pb−Free/Halide Free)	2500 / Tape and Reel
74LCX125MTCX	TSSOP−14 WB (Pb−Free/Halide Free)	2500 / Tape and Reel
74LCX125BQX (Note 5)	QFN−14 (Pb−Free/Halide Free)	3000 / Tape and Reel
74LCX125MTC	TSSOP−14 WB (Pb−Free/Halide Free)	2350 Units / Tube

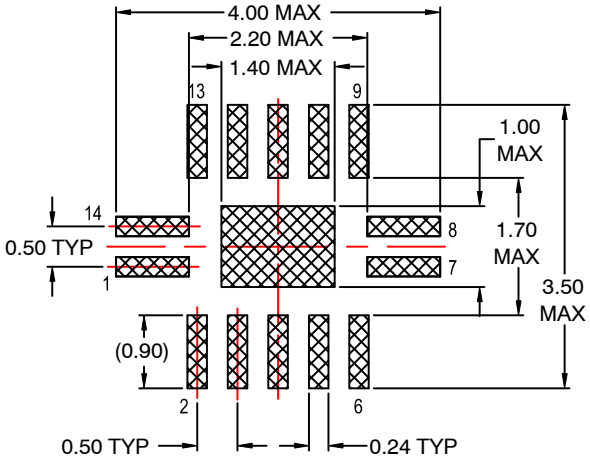
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

5. DQFN package available in Tape and Reel only.

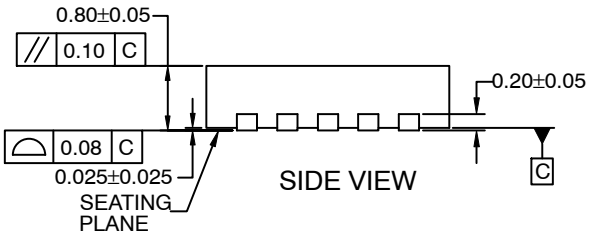
QFN14 3.0x2.5, 0.5P
CASE 510CB
ISSUE O

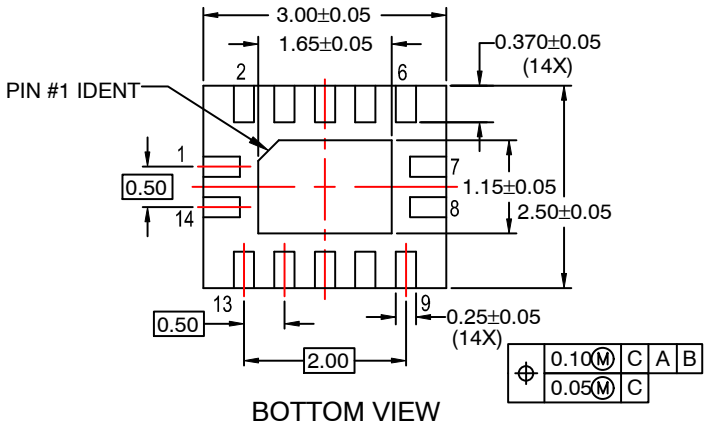
DATE 31 AUG 2016





RECOMMENDED LAND PATTERN





NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−241, VARIATION AA

B. DIMENSIONS ARE IN MILLIMETERS.

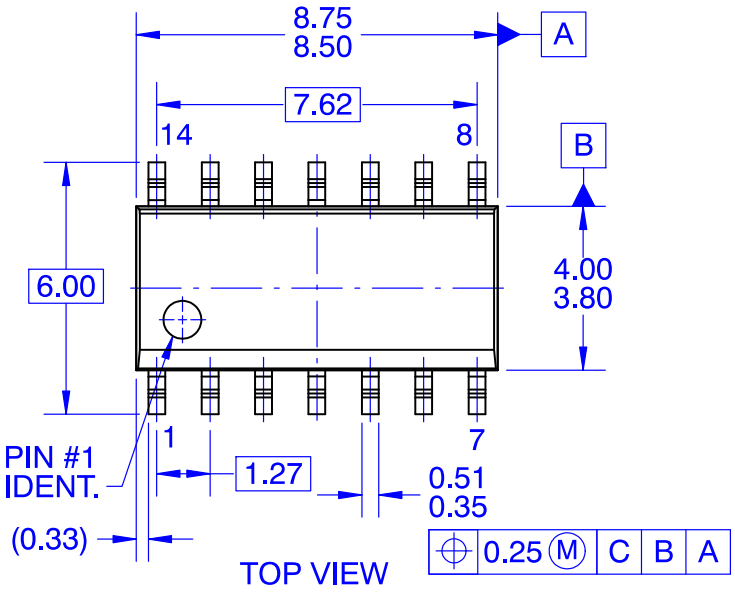
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

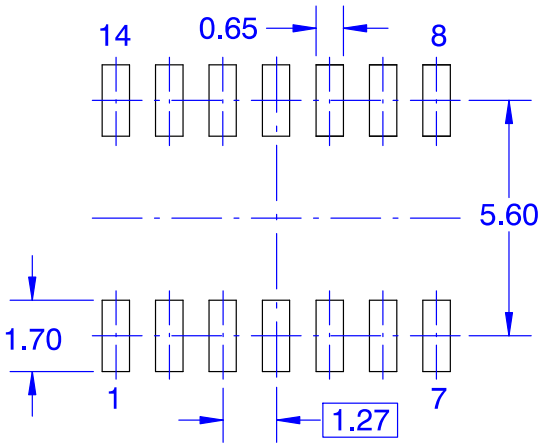
DOCUMENT NUMBER:	**98AON13643G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**QFN14 3.0X2.5, 0.5P**	**PAGE 1 OF 1**

SOIC14
CASE 751EF
ISSUE O

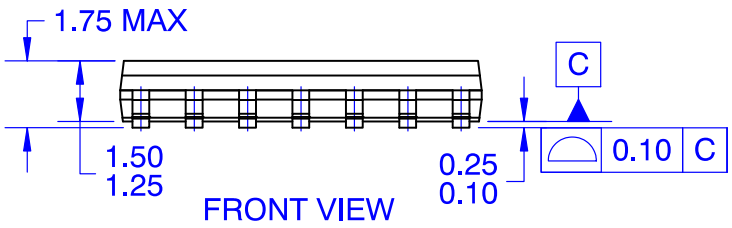
DATE 30 SEP 2016



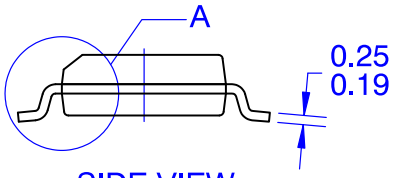
TOP VIEW



LAND PATTERN RECOMMENDATION

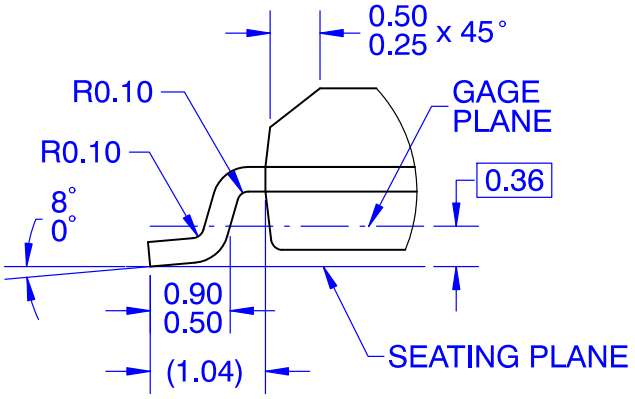


FRONT VIEW



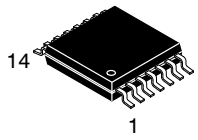
SIDE VIEW

NOTES:
A. CONFORMS TO JEDEC MS−012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145−14M
E. CONFORMS TO ASME Y14.5M, 2009



DETAIL A
SCALE 16 : 1

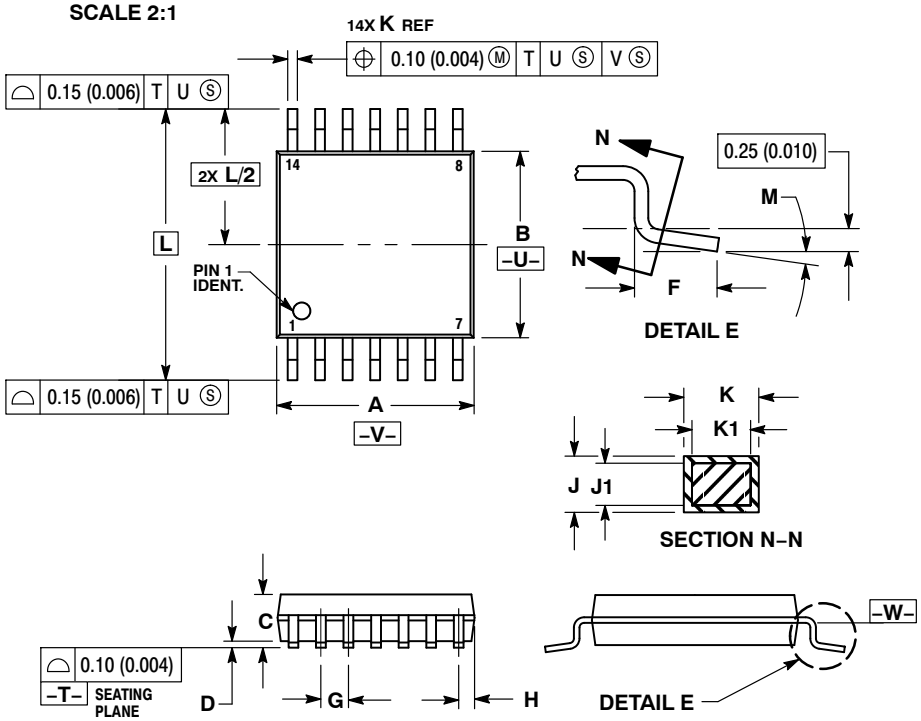
DOCUMENT NUMBER:	**98AON13739G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC14**	**PAGE 1 OF 1**



SCALE 2:1

TSSOP−14 WB
CASE 948G
ISSUE C

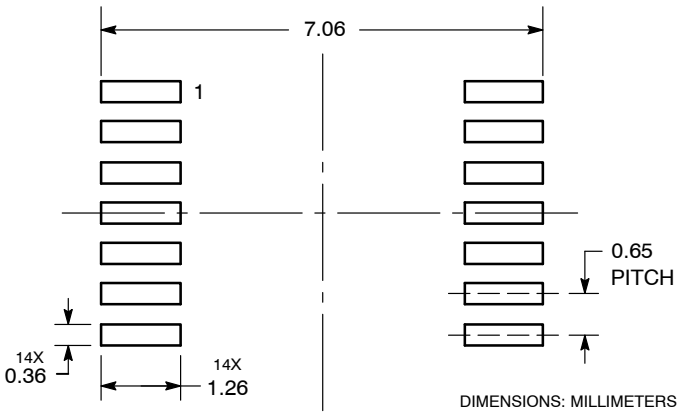
DATE 17 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

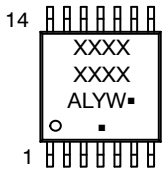
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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