PCN# : P5A3AA
Issue Date : Nov. 24, 2015

DESIGN/PROCESS CHANGE NOTIFICATION

This is to inform you that a change is being made to the products listed below.

Unless otherwise indicated in the details of this notification, the identified change will have no impact on product quality, reliability, electrical, visual or mechanical performance and affected products will remain fully compliant to all published specifications. Products incorporating this change may be shipped interchangeably with existing unchanged products.

This change is planned to take effect in 90 calendar days from the date of this notification. Please work with your local Fairchild Sales Representative to manage your inventory of unchanged product if your evaluation of this change will require more than 90 calendar days.

Please contact your local Customer Quality Engineer within 30 days of receipt of this notification if you require any additional data or samples.

Implementation of change:

Expected First Shipment Date for Changed Product :Feb. 22, 2016

Expected First Date Code of Changed Product :1609

Description of Change (From) :
5-inch wafer fabrication at Fairchild in Bucheon, South Korea

Description of Change (To) :
8 inch wafer fabrication at TowerJazz Japan with Panasonic Semiconductor

Reason for Change:
Fairchild Semiconductor is increasing wafer fabrication capacity by qualifying 8-inch wafer fabrication line in Tower Jazz, Japan. Quality and reliability remain at the highest standards already demonstrated within Fairchild's existing products. The reliability qualification results used to qualify the 8-inch wafer fabrication line are summarized below.Design, die size and layout of the affected products will remain unchanged. There are no changes in the datasheet or electrical performance.

Affected Product(s): Please refer to the list of affected products in the addendum attached in the PCN email you received. This list is based on an analysis of your companys procurement history.

Qualification Plan	Device	Package	Process	No. of Lots
Q20140076	FQP8N60C	TO220	C-FET	3

Test Description:	Condition:	Standard :	Duration:	Results:
High Temperature Reverse Bias	480V,150C	JESD22-A108	1000 hrs	0/231
High Temperature Gate Bias	30V, 150C	JESD22-A108	1000 hrs	0/231
Highly Accelerated Stress Test	85%RH, 130C,42V	JESD22-A110	96 hrs	0/231
Temperature Cycle	-65C,150C	JESD22-A104	500 cyc	0/231
Power Cycle	On/Off=2.0min, Delta Tj=100C	MIL-STD-750 M1037	6000 cyc	0/77
High Temperature Storage Life	150C	JESD22-A103	1000 hrs	0/231
Early Life Failure Rate with HTRB	600V, 150C	JESD22-A108	48 hrs	0/1040

Qualification Plan	Device	Package	Process	No. of Lots
Q20140076	FSB50550T	SPM5F	C-FET	1

Test Description:	Condition:	Standard :	Duration:	Results:
High Temperature Reverse Bias	400V,150C	JESD22-A108	1000 hrs	0/26

Qualification Plan	Device	Package	Process	No. of Lots
Q20140077	FQA24N60	TO3P	Q-FET	3

Test Description:	Condition:	Standard:	Duration:	Results:
High Temperature Reverse Bias	480V,150C	JESD22-A108	1000 hrs	0/231
High Temperature Gate Bias	30V, 150C	JESD22-A108	1000 hrs	0/231
Highly Accelerated Stress Test	130C, 85%RH, 42V	JESD22-A110	96 hrs	0/231
Temperature Cycle	-65C,150C	JESD22-A104	500 cyc	0/231
Power Cycle	On/Off=2.0min, Delta Tj=100C	MIL-STD-750 M1037	6000 cyc	0/77
High Temperature Storage Life	150C	JESD22-A103	1000 hrs	0/231

Qualification Plan	Device	Package	Process	No. of Lots
Q20140079	KA5L0380RYDTU	TO220F	OLD-FET	1

Test Description:	Condition:	Standard:	Duration:	Results:
High Temperature Reverse Bias	640V,125C	JESD22-A108	1000 hrs	0/77
Temperature Humidity Bias Test	85%RH, 85C,100V	JESD22-A101	1000 hrs	0/77
Temperature Cycle	-65C,150C	JESD22-A104	500 cyc	0/77
High Temperature Storage Life	150C	JESD22-A103	1000 hrs	0/77

Qualification Plan	Device	Package	Process	No. of Lots
Q20140079	FS7M0680YDTU	TO3P	OLD-FET	1

Test Description:	Condition:	Standard:	Duration:	Results:
High Temperature Reverse Bias	640V,125C	JESD22-A108	1000 hrs	0/77
Temperature Humidity Bias Test	85%RH, 85C,100V	JESD22-A101	1000 hrs	0/77
Temperature Cycle	-65C,150C	JESD22-A104	500 cyc	0/77
High Temperature Storage Life	150C	JESD22-A103	1000 hrs	0/77

Qualification Plan	Device	Package	Process	No. of Lots
Q20140080	FSDM0265RNB	MDIP	OLD-FET	1

Test Description:	Condition:	Standard:	Duration:	Results:
High Temperature Reverse Bias	520V,125C	JESD22-A108	1000 hrs	0/77
Highly Accelerated Stress Test	110C, 85%RH	JESD22-A110	264 hrs	0/77
Temperature Cycle	-65C,150C	JESD22-A104	500 cyc	0/77
High Temperature Storage Life	150C	JESD22-A103	1000 hrs	0/77