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Title of Change:	KAE-04471 Datasheet Updates			
Effective date:	8 January 2018			
Contact information:	Contact your local ON Semiconductor Sales Office or <john.frenett@onsemi.com></john.frenett@onsemi.com>			
Type of notification:	This Product Bulletin is for notification purposes only. ON Semiconductor will proceed with implementation of this change upon publication of this Product Bulletin.			
Change category:	Wafer Fab Change Assembly Change	Test Change I Other: Datasheet		
Change Sub-Category(s): <ul> <li>Manufacturing Site Change/A</li> <li>Manufacturing Process Change</li> </ul>	5	<ul> <li>Datasheet/Product Doc change</li> <li>Shipping/Packaging/Marking</li> <li>Other:</li> </ul>		
Sites Affected:	ON Semiconductor Sites: ON Rochester, New York	External Foundry/Subcon Sites: None		
<ul> <li>Description and Purpose:</li> <li>This Product Bulletin announces the following changes</li> <li>A number of pins in Table 3 (PIN DESCRIPTION) were mapped to incorrect labels and descriptions due to an incomplete edit of a preliminary revision. The correct mapping is as follows:</li> </ul>				
1) A number of pins in Table 3	(PIN DESCRIPTION) were mapped to incorrect labels a	and descriptions due to an incomplete edit of a		
<ol> <li>A number of pins in Table 3 preliminary revision. The co</li> </ol>	(PIN DESCRIPTION) were mapped to incorrect labels a prrect mapping is as follows:	· · ·		
<ol> <li>A number of pins in Table 3 preliminary revision. The co</li> <li>Pin Number</li> </ol>	(PIN DESCRIPTION) were mapped to incorrect labels a prrect mapping is as follows: Label	Description		
<ol> <li>A number of pins in Table 3 preliminary revision. The co</li> <li>Pin Number B19</li> </ol>	(PIN DESCRIPTION) were mapped to incorrect labels a prrect mapping is as follows: Label RG23b	Description           Amplifier 2 and 3 reset, quadrant b		
<ol> <li>A number of pins in Table 3 preliminary revision. The co</li> <li>Pin Number</li> <li>B19</li> <li>A18</li> </ol>	(PIN DESCRIPTION) were mapped to incorrect labels a prrect mapping is as follows: Label RG23b H2Lb	DescriptionAmplifier 2 and 3 reset, quadrant bHCCD last gate, outputs 1,2 and 3, quadrant b		
1) A number of pins in Table 3 preliminary revision. The co Pin Number B19 A18 C19	(PIN DESCRIPTION) were mapped to incorrect labels a prrect mapping is as follows: <b>Label</b> RG23b H2Lb H2SW2b	DescriptionAmplifier 2 and 3 reset, quadrant bHCCD last gate, outputs 1,2 and 3, quadrant bHCCD output 2 selector, quadrant b		
1) A number of pins in Table 3 preliminary revision. The co Pin Number B19 A18 C19 C18	(PIN DESCRIPTION) were mapped to incorrect labels a rrect mapping is as follows: <b>Label</b> RG23b H2Lb H2SW2b H2SW3b	DescriptionAmplifier 2 and 3 reset, quadrant bHCCD last gate, outputs 1,2 and 3, quadrant bHCCD output 2 selector, quadrant bHCCD output 3 selector, quadrant b		
1) A number of pins in Table 3 preliminary revision. The co Pin Number B19 A18 C19 C18 B18	(PIN DESCRIPTION) were mapped to incorrect labels a prrect mapping is as follows: Label RG23b H2Lb H2SW2b H2SW3b GND	DescriptionAmplifier 2 and 3 reset, quadrant bHCCD last gate, outputs 1,2 and 3, quadrant bHCCD output 2 selector, quadrant bHCCD output 3 selector, quadrant bGround		
1) A number of pins in Table 3 preliminary revision. The co Pin Number B19 A18 C19 C18 B18 A19	(PIN DESCRIPTION) were mapped to incorrect labels a prrect mapping is as follows: Label           RG23b           H2Lb           H2SW2b           H2SW3b           GND           VOUT2b	DescriptionAmplifier 2 and 3 reset, quadrant bHCCD last gate, outputs 1,2 and 3, quadrant bHCCD output 2 selector, quadrant bHCCD output 3 selector, quadrant bGroundVideo output 2, quadrant b		
1) A number of pins in Table 3 preliminary revision. The co Pin Number B19 A18 C19 C18 B18 A19 F24	(PIN DESCRIPTION) were mapped to incorrect labels a prrect mapping is as follows: Label         RG23b         H2Lb         H2SW2b         H2SW3b         GND         VOUT2b         V2B	DescriptionAmplifier 2 and 3 reset, quadrant bHCCD last gate, outputs 1,2 and 3, quadrant bHCCD output 2 selector, quadrant bHCCD output 3 selector, quadrant bGround		
1) A number of pins in Table 3 preliminary revision. The co Pin Number B19 A18 C19 C18 B18 A19 F24 F23	(PIN DESCRIPTION) were mapped to incorrect labels a prrect mapping is as follows: Label         RG23b         H2Lb         H2SW2b         H2SW3b         GND         VOUT2b         V2B         ESD	DescriptionAmplifier 2 and 3 reset, quadrant bHCCD last gate, outputs 1,2 and 3, quadrant bHCCD output 2 selector, quadrant bHCCD output 3 selector, quadrant bGroundVideo output 2, quadrant bVCCD bottom phase 2		
1) A number of pins in Table 3 preliminary revision. The co Pin Number B19 A18 C19 C18 B18 A19 F24 F23 D21	(PIN DESCRIPTION) were mapped to incorrect labels a prrect mapping is as follows: Label         RG23b         H2Lb         H2SW2b         H2SW3b         GND         VOUT2b         V2B         ESD         V1T	DescriptionAmplifier 2 and 3 reset, quadrant bHCCD last gate, outputs 1,2 and 3, quadrant bHCCD output 2 selector, quadrant bHCCD output 3 selector, quadrant bGroundVideo output 2, quadrant bVCCD bottom phase 2VCCD top phase 1		
1) A number of pins in Table 3 preliminary revision. The co Pin Number B19 A18 C19 C18 B18 A19 F24 F23 D21 D22	(PIN DESCRIPTION) were mapped to incorrect labels a prrect mapping is as follows: Label         RG23b         H2Lb         H2SW2b         H2SW3b         GND         VOUT2b         V2B         ESD         V1T         V2T	DescriptionAmplifier 2 and 3 reset, quadrant bHCCD last gate, outputs 1,2 and 3, quadrant bHCCD output 2 selector, quadrant bHCCD output 3 selector, quadrant bGroundVideo output 2, quadrant bVCCD bottom phase 2VCCD top phase 1VCCD top phase 2		
1) A number of pins in Table 3 preliminary revision. The co B19 A18 C19 C18 B18 A19 F24 F23 D21 D22 D23	(PIN DESCRIPTION) were mapped to incorrect labels a rrect mapping is as follows: Label         RG23b         H2Lb         H2SW2b         H2SW3b         GND         VOUT2b         V2B         ESD         V1T         V2T         V3T	DescriptionAmplifier 2 and 3 reset, quadrant bHCCD last gate, outputs 1,2 and 3, quadrant bHCCD output 2 selector, quadrant bHCCD output 3 selector, quadrant bGroundVideo output 2, quadrant bVCCD bottom phase 2VCCD top phase 1VCCD top phase 3		
1) A number of pins in Table 3 preliminary revision. The co B19 A18 C19 C18 B18 A19 F24 F23 D21 D22 D23 E23	(PIN DESCRIPTION) were mapped to incorrect labels a rrect mapping is as follows: Label         RG23b         H2Lb         H2SW2b         H2SW3b         GND         VOUT2b         V2B         ESD         V1T         V2T         V3T         V4T	DescriptionAmplifier 2 and 3 reset, quadrant bHCCD last gate, outputs 1,2 and 3, quadrant bHCCD output 2 selector, quadrant bHCCD output 3 selector, quadrant bGroundVideo output 2, quadrant bVCCD bottom phase 2VCCD top phase 1VCCD top phase 2VCCD top phase 3VCCD top phase 4		
1) A number of pins in Table 3 preliminary revision. The co B19 A18 C19 C18 B18 A19 F24 F23 D21 D22 D23 E23 E4	(PIN DESCRIPTION) were mapped to incorrect labels a rrect mapping is as follows: Label         RG23b         H2Lb         H2SW2b         H2SW3b         GND         VOUT2b         V2B         ESD         V1T         V2T         V3T         V4T         GND	DescriptionAmplifier 2 and 3 reset, quadrant bHCCD last gate, outputs 1,2 and 3, quadrant bHCCD output 2 selector, quadrant bHCCD output 3 selector, quadrant bGroundVideo output 2, quadrant bVCCD bottom phase 2VCCD top phase 1VCCD top phase 2VCCD top phase 3VCCD top phase 4Ground		
1) A number of pins in Table 3 preliminary revision. The co B19 A18 C19 C18 B18 A19 F24 F23 D21 D22 D23 E23 E4 F21	(PIN DESCRIPTION) were mapped to incorrect labels a rrect mapping is as follows: Label         RG23b         H2Lb         H2SW2b         H2SW3b         GND         VOUT2b         V2B         ESD         V1T         V2T         V3T         V4T         GND         VOUT1d	DescriptionAmplifier 2 and 3 reset, quadrant bHCCD last gate, outputs 1,2 and 3, quadrant bHCCD output 2 selector, quadrant bHCCD output 3 selector, quadrant bGroundVideo output 2, quadrant bVCCD bottom phase 2VCCD top phase 1VCCD top phase 2VCCD top phase 3VCCD top phase 4GroundAmplifier 1 output, quadrant d		
1) A number of pins in Table 3 preliminary revision. The co B19 A18 C19 C18 B18 A19 F24 F23 D21 D22 D23 E23 E4 F21 F22	(PIN DESCRIPTION) were mapped to incorrect labels a rrect mapping is as follows: Label         RG23b         H2Lb         H2SW2b         H2SW3b         GND         VOUT2b         V2B         ESD         V1T         V2T         V3T         V4T         GND         VOUT1d         VDUT1d	DescriptionAmplifier 2 and 3 reset, quadrant bHCCD last gate, outputs 1,2 and 3, quadrant bHCCD output 2 selector, quadrant bHCCD output 3 selector, quadrant bGroundVideo output 2, quadrant bVCCD bottom phase 2VCCD top phase 1VCCD top phase 2VCCD top phase 3VCCD top phase 4GroundAmplifier 1 output, quadrant dAmplifier 1 supply, quadrant d		
<ol> <li>A number of pins in Table 3 preliminary revision. The co</li> <li>Pin Number</li> <li>B19</li> <li>A18</li> <li>C19</li> <li>C18</li> <li>B18</li> <li>A19</li> <li>F24</li> <li>F23</li> <li>D21</li> <li>D22</li> <li>D23</li> <li>E23</li> <li>E4</li> <li>F21</li> <li>F22</li> <li>F6</li> </ol>	(PIN DESCRIPTION) were mapped to incorrect labels a rrect mapping is as follows: Label         RG23b         H2Lb         H2SW2b         H2SW3b         GND         VOUT2b         V2B         ESD         V1T         V2T         V3T         V4T         GND         VDUT1d         VDD1d         VDD2c	DescriptionAmplifier 2 and 3 reset, quadrant bHCCD last gate, outputs 1,2 and 3, quadrant bHCCD output 2 selector, quadrant bHCCD output 3 selector, quadrant bGroundVideo output 2, quadrant bVCCD bottom phase 2VCCD top phase 1VCCD top phase 2VCCD top phase 3VCCD top phase 4GroundAmplifier 1 output, quadrant dAmplifier 2 supply, quadrant c		
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<ol> <li>A number of pins in Table 3 preliminary revision. The co</li> <li>Pin Number</li> <li>B19</li> <li>A18</li> <li>C19</li> <li>C18</li> <li>B18</li> <li>A19</li> <li>F24</li> <li>F23</li> <li>D21</li> <li>D22</li> <li>D23</li> <li>E23</li> <li>E4</li> <li>F21</li> <li>F22</li> <li>F6</li> </ol>	(PIN DESCRIPTION) were mapped to incorrect labels a rrect mapping is as follows: Label         RG23b         H2Lb         H2SW2b         H2SW3b         GND         VOUT2b         V2B         ESD         V1T         V2T         V3T         V4T         GND         VOUT1d         VOUT2c         GND	DescriptionAmplifier 2 and 3 reset, quadrant bHCCD last gate, outputs 1,2 and 3, quadrant bHCCD output 2 selector, quadrant bHCCD output 3 selector, quadrant bGroundVideo output 2, quadrant bVCCD bottom phase 2VCCD top phase 1VCCD top phase 2VCCD top phase 3VCCD top phase 4GroundAmplifier 1 output, quadrant dAmplifier 2 supply, quadrant dAmplifier 2 supply, quadrant cVideo output 2, quadrant c		
<ol> <li>A number of pins in Table 3 preliminary revision. The co</li> <li>Pin Number</li> <li>B19</li> <li>A18</li> <li>C19</li> <li>C18</li> <li>B18</li> <li>A19</li> <li>F24</li> <li>F23</li> <li>D21</li> <li>D22</li> <li>D23</li> <li>E23</li> <li>E4</li> <li>F21</li> <li>F22</li> <li>F6</li> <li>F7</li> <li>E18</li> <li>D8</li> </ol>	(PIN DESCRIPTION) were mapped to incorrect labels a rrect mapping is as follows: Label         RG23b         H2Lb         H2SW2b         H2SW3b         GND         VOUT2b         V2B         ESD         V1T         V2T         V3T         V4T         GND         VOUT1d         VOUT2c         GND         VUT1	DescriptionAmplifier 2 and 3 reset, quadrant bHCCD last gate, outputs 1,2 and 3, quadrant bHCCD output 2 selector, quadrant bHCCD output 3 selector, quadrant bGroundVideo output 2, quadrant bVCCD bottom phase 2VCCD top phase 1VCCD top phase 2VCCD top phase 3VCCD top phase 4GroundAmplifier 1 output, quadrant dAmplifier 1 supply, quadrant cVideo output 2, quadrant cGround		
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2) Explicit reference is now provided for no-connect pins in Table 3 (PIN DESCRIPTION).

Pin Number	Label	Description
E1	N/C	No connect
F1	N/C	No connect
D2	N/C	No connect
D1	N/C	No connect
C24	N/C	No connect
A26	N/C	No connect
B26	N/C	No connect
C26	N/C	No connect
D26	N/C	No connect
E26	N/C	No connect
F26	N/C	No connect

3) Updated Table 3 (PIN DESCRIPTION) with missing row.

Pin Number	Label	Description
F3	ESD	

- 4) Added Figure 4 (Monochrome and Color Quantum Efficiency).
- 5) Added Figure 5 (Angled Response for Monochrome Device).
- 6) Added Figure 6 (Vertical Angled Response for Color Device).
- 7) Added Figure 7 (Horizontal Angled Response for Color Device).
- 8) Added Figure 8 (Frame Rates vs. Clock Frequency).
- 9) Table 9 (DC BIAS OPERATING CONDITIONS): The second of two original notes has been rewritten; a third note has been added.
- 10) Table 12 (ELECTRONIC SHUTTER PULSE): All rows have been eliminated, save for one. The single remaining row, dedicated to pin SUB, presents new values for Low and High electronic shutter voltages.
- 11) Table 13, previously labelled DC BIAS OPERATING CONDITIONS, is now labelled DEVICE IDENTIFICATION.
- 12) Relabeled Figure 33 (Completed Assembly 1).
- 13) Relabeled Figure 34 (Completed Assembly 2).
- 14) Relabeled Figure 35 (Completed Assembly 3).
- 15) The Table 7 (ABSOLUTE MAXIMUM RATINGS) value for Operating Temperature Minimum has been corrected to read -30 deg C (had been -70 deg C).
- 16) In Table 13 (DEVICE IDENTIFICATION VALUES), item Device Identification's MIN, NOM, and MAX have been corrected to 63,000 (was 8,000), 70,000 (was 10,000), and 84,000 (was 12,000), respectively.

## List of Affected Standard Parts:

KAE-04471-ABA-JP-FA KAE-04471-ABA-JP-EE KAE-04471-FBA-JP-FA KAE-04471-FBA-JP-EE KAE-04471-ABA-SP-FA KAE-04471-ABA-SD-FA KAE-04471-ABA-SD-FA KAE-04471-FBA-SD-FA KAE-04471-FBA-SD-FA KAE-04471-FBA-SD-FA