

DESIGN/PROCESS CHANGE NOTIFICATION -- FINAL

This is to inform you that a design and/or process change will be made to the following product(s). This notification is for your information and concurrence.

If you require data or samples to qualify this change, please contact **Fairchild Semiconductor within 30 days of receipt of this notification.**

Updated process quality documentation, such as FMEAs and Control Plans, are available for viewing upon request.

If you have any questions concerning this change, please contact:

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Implementation of change:

Expected 1st Device Shipment Date: 2011/09/23

Earliest Year/Work Week of Changed Product: 2011/WW39

Change Type Description: Alternate Fab Location

Description of Change (From): Current wafer fabrication is at Fairchild Semiconductor Salt Lake, Utah.

Description of Change (To): In addition to Fairchild Semiconductor Salt Lake, Utah, products will be manufactured using Taiwan Semiconductor Manufacturing Company Limited, Taiwan. Design, die size and layout of the affected products (see affected FSID list) remain unchanged. There are no changes in the datasheet or electrical performance between products manufactured at the Current and Alternate wafer fab locations.

Reason for Change : Fairchild Semiconductor is increasing wafer capacity by qualifying the product wafer fabrication at Taiwan Semiconductor Manufacturing Company Limited, Taiwan. Quality and reliability will remain at the highest standards already demonstrated with Fairchild's existing products. This change is planned to take effect in 90 calendar days from the date of this notification. Please work with your local Fairchild sales representative to place orders for sufficient quantities of unchanged product to support your manufacturing needs if your evaluation of this change will require more than 90 calendar days.

Qual/REL Plan Number(s): Q20110350

Qualification :

All tests outlined in QP11030879 qualification plan were successfully completed. As such, TSMC is qualified as an alternate wafer manufacturing site for the products.

Results/Discussion for Qual Plan Number(s): Q20110350

Test: (High Temperature Gate Bias) Conditions: 150C, 20V Standard: JESD22-A108					
Lot	Device	168-HOURS	500-HOURS	1000-HOURS	Failure Code
Q20110350AAHTGB	FDC655BN_G	0/79			
			0/79		
				0/79	
Q20110350ABHTGB		0/79			
			0/79		
				0/79	
Test: (High Temperature Reverse Bias) Conditions: 150C, 24V Standard: JESD22-A108					
Lot	Device	168-HOURS	500-HOURS	1000-HOURS	Failure Code
Q20110350AAHTRB		0/79			
			0/79		
				0/79	
Q20110350ABHTRB		0/79			
			0/79		
				0/79	
Test: (High Temperature Storage Life) Conditions: 175C Standard: JESD22-A103					
Lot	Device	168-HOURS	500-HOURS	Failure Code	
Q20110350AAHTSL	FDC655BN_G	0/79			
Q20110350AAHTSL	FDC655BN_G		0/79		
Q20110350ABHTSL	FDC655BN_G	0/79			
Q20110350ABHTSL	FDC655BN_G		0/79		
Test: (Highly Accelerated Stress Test) Conditions: 85%RH, 130C, 24V Standard: JESD22-A110					
Lot	Device	96-HOURS	Failure Code		
Q20110350AAHAST1	FDC655BN_G	0/79			
Q20110350ABHAST1	FDC655BN_G	0/79			
Test: (Precondition) Conditions: Standard: JESD22-A113					
Lot	Device	Results	Failure Code		
Q20110350AAPCNL1A	FDC655BN_G	0/158			
Q20110350ABPCNL1A	FDC655BN_G	0/158			
Test: (Resistance to Solder Heat) Conditions: Standard: JESD22-B106					
Lot	Device	Results	Failure Code		
Q20110350AARSDH	FDC655BN_G	0/30			
Q20110350ABRSDH	FDC655BN_G	0/30			
Test: (Temperature Cycle) Conditions: -65C, 150C Standard: JESD22-A104					
Lot	Device	100-CYCLES	500-CYCLES	Failure Code	
Q20110350AATMCL1	FDC655BN_G	0/79			
Q20110350AATMCL1	FDC655BN_G		0/79		
Q20110350ABTMCL1	FDC655BN_G	0/79			
Q20110350ABTMCL1	FDC655BN_G		0/79		

Product Id Description : Selected Fairchild Semiconductor products. For complete listing please refer to the Affected FSID section.

Affected FSIDs :

FDC655BN	FDC655BN_G	
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