FAIRCHILD SEMICONDUCTOR®

The Right Technology for Your Success

PCN# : P338A
Issue Date : May. 09, 2013

DESIGN/PROCESS CHANGE NOTIFICATION

This is to inform you that a change is being made to the products listed below.

Unless otherwise indicated in the details of this notification, the identified change will have no impact on product quality, reliability, electrical, visual or mechanical performance and affected products will remain fully compliant to all published specifications. Products incorporating this change may be shipped interchangeably with existing unchanged products.

This change is planned to take effect in 90 calendar days from the date of this notification. Please work with your local Fairchild Sales Representative to manage your inventory of unchanged product if your evaluation of this change will require more than 90 calendar days.

Please contact your local Customer Quality Engineer within 30 days of receipt of this notification if you require any additional data or samples. Alternatively, you may send an email request for data, samples or other information to PCNSupport@fairchildsemi.com.

Implementation of change:

Expected First Shipment Date for Changed Product : Aug. 07, 2013

Expected First Date Code of Changed Product :1328

Description of Change (From) :
LNDMOS transistors (Q1, Q3, Q4, and Q5 ref. page 4 of the data sheet) have a temporary higher than expected leakages due to the process variations. The leakage statistic distributions present tails going beyond the data sheet upper limits and cause yield losses. Investigations revealed the diffusions inside high voltage N well have too small guardbands between edges.

Description of Change (To) :
Four mask changes address LNDMOS transistors (Q1, Q3, Q4, and Q5) leakages. The guardband will be increased by 0.7um between the edges of the diffusions inside N well.

Reason for Change:
Reduces the LNDMOS leakages reflected in a yield loss and meanwhile allows the Data Sheet battery leakage currents upper limit to be decreased from 20 to 10 uA.

Affected Product(s):

FAN54300UCX		

Qualification Plan	Device	Package	Process	No. of Lots
Q20100392	FAN54300	UCBBU030	FS35 5_40S	3

Test Description:	Condition:	Standard :	Duration:	Results:
Charged Device Model ESD	1.5 kV	JESD22-C101	-	0/3
Dynamic Op Life	125C, 3.6V	JESD22-A108	1000 hrs	0/77
Dynamic Op Life	125C, 3.6V	JESD22-A108	168 hrs	0/154
High Temperature Storage Life	150C	JESD22-A103	1000 hrs	0/231
Human Body Model ESD	2.0 kV	JESD22-A114	-	0/3
Latch Up	6.75V, +300, -200mA	JESD 78	-	0/6
Temperature Cycle	-40C, 125C	JESD22-A104	1000 Cycles	0/77
Temperature Cycle	-40C, 125C	JESD22-A104	100 Cycles	0/154