ON Semiconductor®

Product Bulletin

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Title of Change:	AR0330CM Datasheet Update
Effective date:	13 Feb 2020
Contact information:	Contact your local ON Semiconductor Sales Office or Sonya.Yip@onsemi.com
Type of notification:	This Product Bulletin is for notification purposes only. ON Semiconductor will proceed with implementation of this change upon publication of this Product Bulletin.
Change Category:	Documentation Change
Change Sub-Category(s):	Datasheet/Product Doc change

Sites Affected:

ON Semiconductor Sites	**External Foundry/Subcon Sites**
None	None

Description and Purpose:

Updated the AR0330CM datasheet with new information.

1. Updated “Table 2, Available Part Numbers”.

Old Table 2:

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
AR0330CM1C00SHAA0−DP	3 MP 1/3″ CIS	Dry Pack with Protective Film
AR0330CM1C00SHAA0−DR	3 MP 1/3″ CIS	Dry Pack without Protective Film
AR0330CM1C00SHAA0−TP	3 MP 1/3″ CIS	Tape & Reel with Protective Film
AR0330CM1C00SHKA0−CP	3 MP 1/3″ CIS	Chip Tray with Protective Film
AR0330CM1C00SHKA0−CR	3 MP 1/3″ CIS	Chip Tray without Protective Film
AR0330CM1C12SHAA0−DP	3 MP 1/3″ CIS	Dry Pack with Protective Film
AR0330CM1C12SHAA0−DR	3 MP 1/3″ CIS	Dry Pack without Protective Film
AR0330CM1C12SHKA0−CP	3 MP 1/3″ CIS	Chip Tray with Protective Film
AR0330CM1C12SHKA0−CR	3 MP 1/3″ CIS	Chip Tray without Protective Film
AR0330CM1C21SHKA0−CP	3 MP 1/3″ CIS	Chip Tray with Protective Film
AR0330CM1C21SHKA0−CR	3 MP 1/3″ CIS	Chip Tray without Protective Film

New Table 2:

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
AR0330CM1C00SHAA0−DP	3.5MP, 1/3−inch, 0 Deg CRA, HiSpi, MIPI, CLCC	Tray, Protective Film
AR0330CM1C00SHAA0−DP1	3.5MP, 1/3−inch, 0 Deg CRA, HiSpi, MIPI, CLCC	Tray, Protective Film Low MOQ
AR0330CM1C00SHAA0−DR	3.5MP, 1/3−inch, 0 Deg CRA, HiSpi, MIPI, CLCC	Tray, No Protective Film
AR0330CM1C00SHAA0−DR1	3.5MP, 1/3−inch, 0 Deg CRA, HiSpi, MIPI, CLCC	Tray, No Protective Film Low MOQ
AR0330CM1C00SHAA0−TP	3.5MP, 1/3−inch, 0 Deg CRA, HiSpi, MIPI, CLCC	Tape & Reel, Protective Film
AR0330CM1C00SHKA0−CP	3.5MP, 1/3−inch, 0 Deg CRA, HiSpi, MIPI, CSP	Tray, Protective Film
AR0330CM1C00SHKA0−CR	3.5MP, 1/3−inch, 0 Deg CRA, HiSpi, MIPI, CSP	Tray, No Protective Film
AR0330CM1C12SHAA0−DP	3.5MP, 1/3−inch, 12 Deg CRA, HiSpi, MIPI, CLCC	Tray, Protective Film
AR0330CM1C12SHAA0−DP1	3.5MP, 1/3−inch, 12 Deg CRA, HiSpi, MIPI, CLCC	Tray, Protective Film Low MOQ
AR0330CM1C12SHAA0−DR	3.5MP, 1/3−inch, 12 Deg CRA, HiSpi, MIPI, CLCC	Tray, No Protective Film
AR0330CM1C12SHAA0−DR1	3.5MP, 1/3−inch, 12 Deg CRA, HiSpi, MIPI, CLCC	Tray, No Protective Film Low MOQ
AR0330CM1C12SHKA0−CP	3.5MP, 1/3−inch, 12 Deg CRA, HiSpi, MIPI, CSP	Tray, Protective Film
AR0330CM1C12SHKA0−CR	3.5MP, 1/3−inch, 12 Deg CRA, HiSpi, MIPI, CSP	Tray, No Protective Film
AR0330CM1C12SUD20	3.5MP, 1/3−inch, 12 Deg CRA, HiSpi, MIPI, Parallel	Recon Die
AR0330CM1C21SHKA0−CP	3.5MP, 1/3−inch, 21 Deg CRA, HiSpi, MIPI, CSP	Tray, Protective Film
AR0330CM1C21SHKA0−CR	3.5MP, 1/3−inch, 21 Deg CRA, HiSpi, MIPI, CSP	Tray, No Protective Film
AR0330CM1C21SUD20	3.5MP, 1/3−inch, 21 Deg CRA, HiSpi, MIPI, Parallel	Recon Die
AR0330CM1C25SUD20	3.5MP, 1/3−inch, 25 Deg CRA, HiSpi, MIPI, Parallel	Recon Die
AR0330CM1C00SHAAH3−GEVB	3.5MP, 1/3−inch, 0 Deg CRA, HiSpi, MIPI, CLCC	Demo Headboard

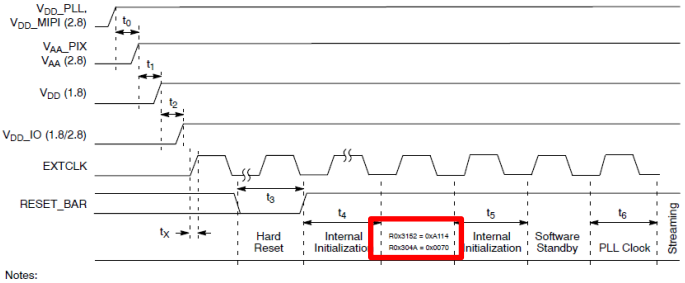
2. Updated “Power -Up Sequence” section and “Figure 6, Power-Up”.

Old Power-Up Sequence:

Power-Up Sequence

The recommended power-up sequence for the AR0330CS is shown in Figure 6. The available power supplies (V_{DD}_IO, V_{DD}_PLL, V_{DD}_MIPI, V_{AA}, V_{AA}_PIX) must have the separation specified below.

1. Turn on V_{DD}_PLL and V_{DD}_MIPI power supplies.
2. After 100 µs, turn on V_{AA} and V_{AA}_PIX power supply.
3. After 100 µs, turn on V_{DD} power supply.
4. After 100 µs, turn on V_{DD}_IO power supply.
5. After the last power supply is stable, enable EXTCLK.
6. Assert RESET_BAR for at least 1 ms.
7. Wait 150,000 EXTCLK periods (for internal initialization into software standby.
8. Write R0x3152 = 0xA114 to configure the internal register initialization process.
9. Write R0x304A = 0x0070 to start the internal register initialization process.
10. Wait 150,000 EXTCLK periods.
11. Configure PLL, output, and image settings to desired values.
12. Wait 1ms for the PLL to lock.
13. Set streaming mode (R0x301A[2] = 1).



Notes:
1. A software reset (R0x301A[0] = 1) is not necessary after the procedure described above since a Hard Reset will automatically triggers a software reset. Independently executing a software reset, should be followed by steps seven through thirteen above.
2. The sensor must be receiving the external input clock (EXTCLK) before the reset pin is toggled. The sensor will begin an internal initialization sequence when the reset pin toggle from LOW to HIGH. This initialization sequence will run using the external input clock. Power on default state is software standby state, need to apply two-wire serial commands to start streaming. Above power up sequence is a general power up sequence. For different interface configurations, MIPI, and Parallel, some power rails are not needed. Those not needed power rails should be ignored in the general power up sequence.

Figure 6. Power Up

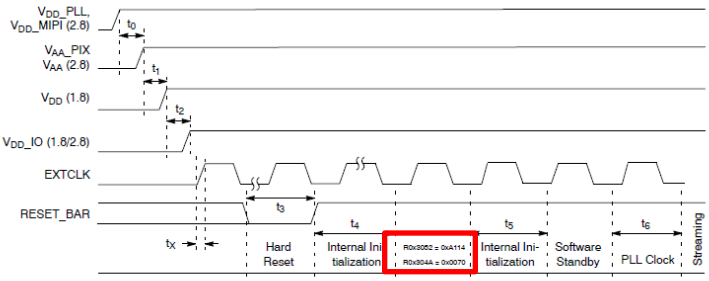
New Power-Up Sequence:

SENSOR INITIALIZATION

Power-Up Sequence

The recommended power-up sequence for the AR0330CS is shown in Figure 6. The available power supplies (V_{DD}_IO, V_{DD}_PLL, V_{DD}_MIPI, V_{AA}, V_{AA}_PIX) must have the separation specified below.

1. Turn on V_{DD}_PLL and V_{DD}_MIPI power supplies.
2. After 100 µs, turn on V_{AA} and V_{AA}_PIX power supply.
3. After 100 µs, turn on V_{DD} power supply.
4. After 100 µs, turn on V_{DD}_IO power supply.
5. After the last power supply is stable, enable EXTCLK.
6. Assert RESET_BAR for at least 1 ms.
7. Wait 150,000 EXTCLK periods (for internal initialization into software standby.
8. Write R0x3052 = 0xA114 to configure the internal register initialization process.
9. Write R0x304A = 0x0070 to start the internal register initialization process.
10. Wait 150,000 EXTCLK periods.
11. Configure PLL, output, and image settings to desired values.
12. Wait 1 ms for the PLL to lock.
13. Set streaming mode (R0x301A[2] = 1).



Notes:
1. A software reset (R0x301A[0] = 1) is not necessary after the procedure described above since a Hard Reset will automatically triggers a software reset. Independently executing a software reset, should be followed by steps seven through thirteen above.
2. The sensor must be receiving the external input clock (EXTCLK) before the reset pin is toggled. The sensor will begin an internal initialization sequence when the reset pin toggle from LOW to HIGH. This initialization sequence will run using the external input clock. Power on default state is software standby state, need to apply two-wire serial commands to start streaming. Above power up sequence is a general power up sequence. For different interface configurations, MIPI, and Parallel, some power rails are not needed. Those not needed power rails should be ignored in the general power up sequence.

Figure 6. Power Up

3. Updated “Table 7, Power-Up Sequence”.

Old Table 7:

Table 7. POWER-UP SEQUENCE

Symbol	Definition	Min	Typ	Max	Unit
t_0	V_{DD}_PLL, V_{DD}_MIPI to V_{AA}/V_{AA}_PIX (Note 3)	0	100	–	μs
t_1	V_{AA}/V_{AA}_PIX to V_{DD}	0	100	–	μs
t_2	V_{DD} to V_{DD}_IO	0	100	–	μs
t_X	External Clock Settling Time (Note 1)	–	30	–	ms
t_3	Hard Reset (Note 2)	1	–	–	ms
t_4	Internal Initialization	150000	–	–	EXTCLKs
t_5	Internal Initialization	150000	–	–	EXTCLKs
t_6	PLL Lock Time	1	–	–	ms

1. External clock settling time is component-dependent, usually taking about 10–100 ms.
2. Hard reset time is the minimum time required after power rails are settled. In a circuit where Hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.
3. It is critical that V_{DD}_PLL is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that V_{DD}_PLL is powered after other supplies then sensor may have functionality issues and will experience high current draw on this supply.
4. V_{DD}_MIPI is tied to V_{DD}_PLL in the both the CLCC and CSP packages and must be powered to 2.8 V. The V_{DD}_HiSPi and V_{DD}_HiSPi_TX supplies do not need to be turned on if the sensor is configured to use the MIPI or parallel interface.

New Table 7:

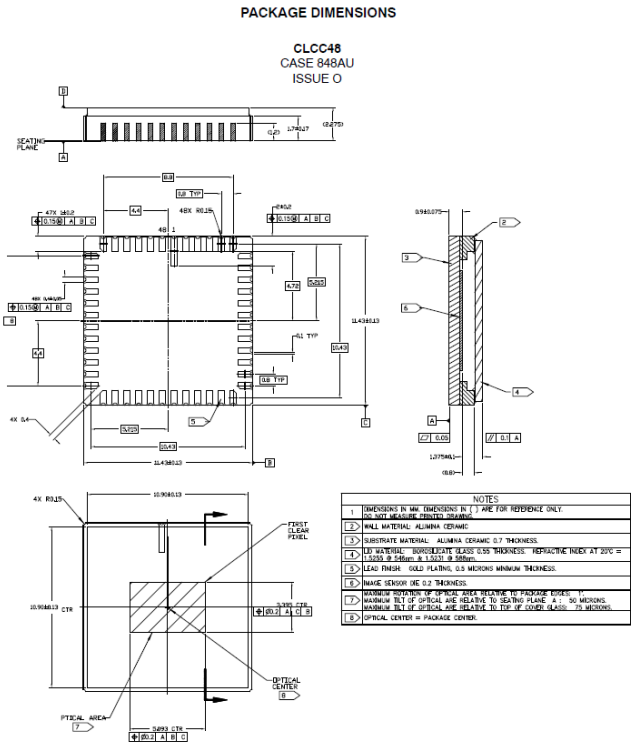
Table 7. POWER-UP SEQUENCE

Symbol	Definition	Min	Typ	Max	Unit
t_0	V_{DD}_PLL, V_{DD}_MIPI to V_{AA}/V_{AA}_PIX (Note 5)	0	100	–	μs
t_1	V_{AA}/V_{AA}_PIX to V_{DD}	0	100	–	μs
t_2	V_{DD} to V_{DD}_IO	0	100	–	μs
t_X	External Clock Settling Time (Note 3)	–	30	–	ms
t_3	Hard Reset (Note 4)	1	–	–	ms
t_4	Internal Initialization	317500	–	–	EXTCLKs
t_5	Internal Initialization	317500	–	–	EXTCLKs
t_6	PLL Lock Time	1	–	–	ms

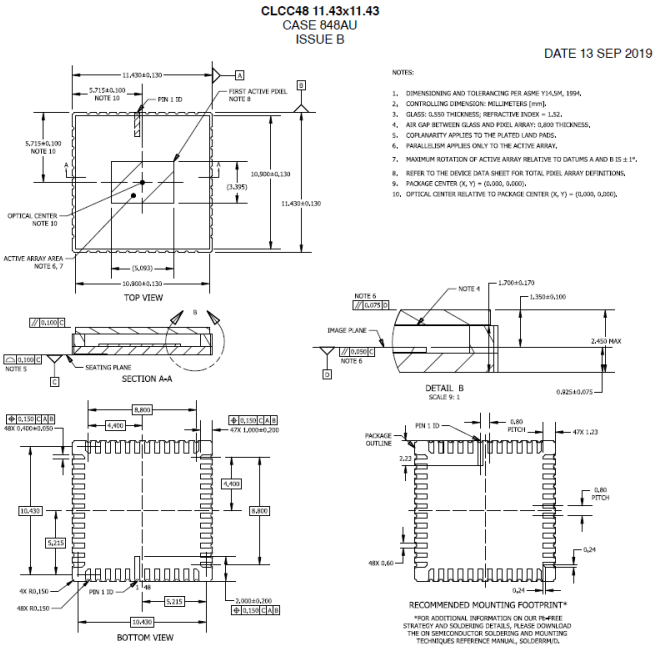
3. External clock settling time is component-dependent, usually taking about 10–100 ms.
4. Hard reset time is the minimum time required after power rails are settled. In a circuit where Hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.
5. It is critical that V_{DD}_PLL is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that V_{DD}_PLL is powered after other supplies then sensor may have functionality issues and will experience high current draw on this supply.
6. V_{DD}_MIPI is tied to V_{DD}_PLL in the both the CLCC and CSP packages and must be powered to 2.8 V. The V_{DD}_HiSPi and V_{DD}_HiSPi_TX supplies do not need to be turned on if the sensor is configured to use the MIPI or parallel interface.
7. T4 and T5 use CLOCK unit, for example if EXCLK is 24MHz, 317500 clocks cycle equal to 13.23ms.

4. pdated CASE 848AU with latest revision of package drawing.

Old CASE 848AU:

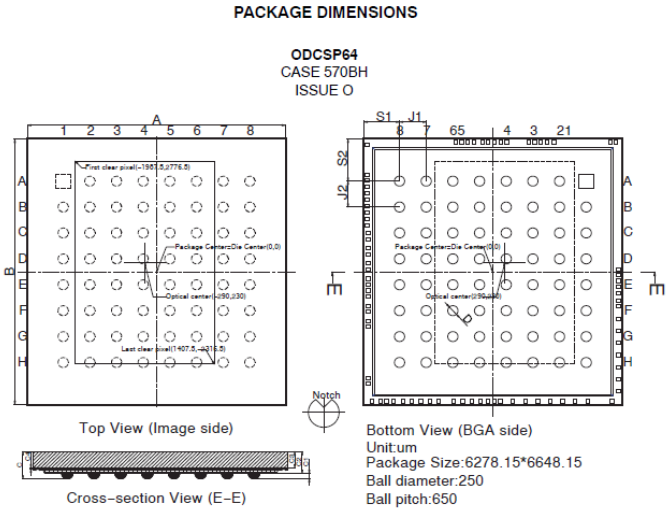


New CASE 848AU:

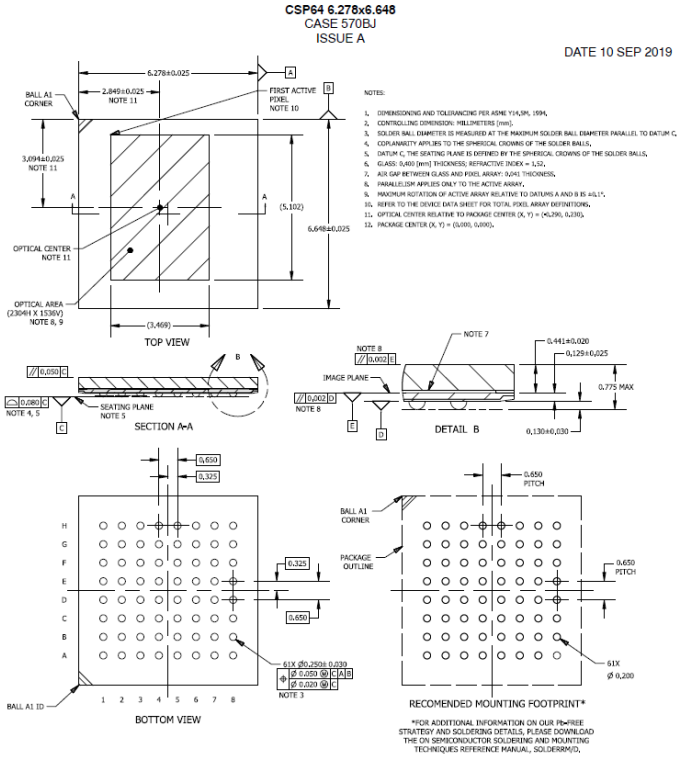


5. Replaced CASE 570BH with new CASE 570BJ.

Old CASE 570BH:



New CASE 570BJ:



List of Affected Standard Parts:

***Note**: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal**.*

AR0330CM1C00SHKA0-CR	AR0330CM1C12SHAA0-DP1	AR0330CM1C12SUD20
AR0330CM1C21SHKA0-CP	AR0330CM1C21SHKA0-CR	AR0330CM1C21SUD20
AR0330CM1C25SUD20	AR0330CM1C00SHAA0-DP	AR0330CM1C00SHAA0-DP1
AR0330CM1C00SHAA0-DR	AR0330CM1C00SHAA0-DR1	AR0330CM1C00SHAA0-TP
AR0330CM1C00SHKA0-CP	AR0330CM1C12SHAA0-DP	AR0330CM1C12SHAA0-DR
AR0330CM1C12SHAA0-DR1	AR0330CM1C12SHKA0-CP	AR0330CM1C12SHKA0-CR