ON Semiconductor

FINAL PRODUCT/PROCESS CHANGE NOTIFICATION #16449

Generic Copy

05-Apr-2010

TITLE: Trench Die Transfer to ON Semiconductor in Aizu, Japan

PROPOSED FIRST SHIP DATE: 05-Jul-2010

AFFECTED CHANGE CATEGORY(S):

FOR ANY QUESTIONS CONCERNING THIS NOTIFICATION:
Contact your local ON Semiconductor Sales Office or Wes Reid < wes.reid@onsemi.com >

SAMPLES: Contact your local ON Semiconductor Sales Office

ADDITIONAL RELIABILITY DATA: Available
Contact your local ON Semiconductor Sales Office or Matt Kas< Matt.Kas@onsemi.com >

NOTIFICATION TYPE:

Final Product/Process Change Notification (FPCN)

Final change notification sent to customers. FPCNs are issued at least 90 days prior to implementation of the change.

ON Semiconductor will consider this change approved unless specific conditions of acceptance are provided in writing within 30 days of receipt of this notice. To do so, contact <quality@onsemi.com>.

DESCRIPTION AND PURPOSE:

This Process Change Notice is the final version to Process Change Notice #16249. PCN #16249 announced that the ON Semiconductor's Wafer Fab facilities in Aizu, Japan, along with the current Wafer Foundry will both be sources for Trench MOSFET Die.

The Aizu Wafer Fab facility is fully certified, and has been a continuous source for MOSFET Die for over 20-years. The Trench MOSFET Die platform was qualified at the Aizu facility in May 2007.

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RELIABILITY DATA SUMMARY:

Reliability Test Results:

NTMS4107NR2G, N-Ch, 30Vds, 20Vgs, SO8 Package
Test: High Temperature Reverse Bias (HTRB)
Conditions: Vds= 24V, Ta=150'C, Duration= 1008Hrs
Results: 0/231
Test: High Temperature Gate Bias (HTGB)
Conditions: Vgs= 20V, Ta=150'C, Duration= 504Hrs
Results: 0/231
Test: Highly Accelerated Stress Test (HAST)
Conditions: Ta=130'C, P= 18.8psi, RH= 85%, Duration= 96Hrs
Results: 0/231
Test: Intermittent Operating Life (IOL-PC)
Conditions: Ta=25'C, delta Tj=100'C, 2-min on/off, 15K-cycles
Results: 0/231
Test: Temperature Cycling (TC-PC)
Conditions: Ta=-65'C/150'C, Air-to-Air, Dwell >=10-min, 500-cy
Results: 0/231
Test: Autoclave Test (AC-PC)
Conditions: Ta=121'C, P=15psi, RH=100%, 96-Hrs
Results: 0/231
Test: Resistance to Solder Heat
Conditions: Ta=260'C, Dwell Time=10-Seconds,
Results: 0/135

NTZD3154NT1G, N-Ch, 20Vds, 6Vgs, SOT563 Package
Test: High Temperature Reverse Bias (HTRB)
Conditions: Vgs= 12V, Ta=150'C, Duration= 1008Hrs, 3-Lots
Results: 0/231
Test: High Temperature Gate Bias (HTGB)
Conditions: Vgs= 6V, Ta=150'C, Duration= 1008Hrs, 3-Lots
Results: 0/231

P-Ch, 30Vds, 8Vgs, ChipFET Package
Test: High Temperature Reverse Bias (HTRB)
Conditions: Vds= 24V, Ta=150'C, Duration= 504Hrs, 3-Lots
Results: 0/231
Test: High Temperature Gate Bias (HTGB)
Conditions: Vgs= 8V, Ta=150'C, Duration= 504Hrs, 3-Lots
Results: 0/231

NTJD4152PT1G, P-Ch, 20Vds, 12Vgs, SC88 Package
Test: High Temperature Gate Bias (HTGB)
Conditions: Vgs= 12V, Ta=150'C, Duration= 1008Hrs, 2-Lots
Results: 0/154

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ELECTRICAL CHARACTERISTIC SUMMARY:

There is no significant change in electrical parametric performance.
Characterization data is available upon request.

CHANGED PART IDENTIFICATION:

Products (listed on this FPCN) assembled with either MagnaChip or ON Semiconductor Die will have a Finish Good Date Code representing Work Week 26, 2010 or newer.

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List of affected General Parts:

NUS3065MUTAG
NUS3055MUTAG
NUS3045MNT1G
NUS3046MNT1G