PCN# : P57JAA
Issue Date : Aug. 04, 2015

DESIGN/PROCESS CHANGE NOTIFICATION

This is to inform you that a change is being made to the products listed below.

Unless otherwise indicated in the details of this notification, the identified change will have no impact on product quality, reliability, electrical, visual or mechanical performance and affected products will remain fully compliant to all published specifications. Products incorporating this change may be shipped interchangeably with existing unchanged products.

This change is planned to take effect in 90 calendar days from the date of this notification. Please work with your local Fairchild Sales Representative to manage your inventory of unchanged product if your evaluation of this change will require more than 90 calendar days.

Please contact your local Customer Quality Engineer within 30 days of receipt of this notification if you require any additional data or samples. Alternatively, you may send an email request for data, samples or other information to PCNSupport@fairchildsemi.com.

Implementation of change:

Expected First Shipment Date for Changed Product : Nov. 02, 2015

Expected First Date Code of Changed Product :1545

Description of Change (From) :
Front-end Wafer Fabrication site Fairchild Salt Lake Utah, 6-inch wafers

Description of Change (To) :
Front-end Wafer Fabrication site Tower Jazz Israel Foundry, 8-inch wafers

Reason for Change:
Improve supply flexibility.
Better quality and yields through equipment and facility upgrades.
- Increased automation in handling and inspection in assembly.
Fairchild partners with foundries and assembly subcontractors.
- Best manufacturing practices, access to many customers methods and practices.
- Advanced technology for fast ramp of future new products and technologies.

Affected Product(s): Please refer to the list of affected products in the addendum attached in the PCN email you received. This list is based on an analysis of your company’s procurement history.

Qualification Plan	Device	Package	Process	No. of Lots
Q20140372	FDC6303N	SSOT6 Duals	5.0 M Cells NZ	2

Test Description:	Condition:	Standard:	Duration:	Results:
MSL1 Precondition	260°C, 3 cycles	JESD22-A113	NA	0/154
Highly Accelerated Stress Test	130°C, 85%RH, Vr = 20V	JESD22-A110	96 hrs	0/154
High Temperature Gate Bias	150°C, Vgs = 8V	JESD22-A108	1000 hrs	0/154
High Temperature Reverse Bias	150°C, Vr = 20V	JESD22-A108	1000 hrs	0/154

Qualification Plan	Device	Package	Process	No. of Lots
Q20140105A	BSS138_SB9G001	SOT23	3.8M Cells Nch	3

Test Description:	Condition:	Standard:	Duration:	Results:
MSL1 Precondition	260°C, 3 cycles	JESD22-A113	NA	0/1155
Highly Accelerated Stress Test	130°C, 85%RH, Vr = 40V	JESD22-A110	96 hrs	0/231
High Temperature Gate Bias	150°C, Vgs = 20V	JESD22-A108	1000 hrs	0/231
High Temperature Reverse Bias	150°C, Vr = 50V	JESD22-A108	1000 hrs	0/231
High Temperature Storage Life	150°C	JESD22-A103	1000 hrs	0/231
Power Cycle	T on/off = 2min, Delta Tj = 100°C	MIL- STD-750-1036	15000 cycles	0/231
Temperature Cycle	-55°C to 150°C	JESD22-A104	1000 cycles	0/231
Unbiased Highly Accelerated Stress Test	130°C, 85%RH	JESD22-A118	96 hrs	0/231
Resistance to Solder Heat	260°C	JESD22-B106	10 sec	0/90

Qualification Plan	Device	Package	Process	No. of Lots
Q20140105A	NDB6030PL	TO263	5.0 M Cells Pch	2

Test Description:	Condition:	Standard:	Duration:	Results:
MSL1 Precondition	245°C, 3 cycles	JESD22-A113	NA	0/616
Highly Accelerated Stress Test	130°C, 85%RH, Vr = -24V	JESD22-A110	96 hrs	0/154
High Temperature Gate Bias	175°C, Vgs = -16V	JESD22-A108	1000 hrs	0/154
High Temperature Reverse Bias	175°C, Vr = -24V	JESD22-A108	1000 hrs	0/154
High Temperature Storage Life	175°C	JESD22-A103	1000 hrs	0/154
Power Cycle	Delta 100CC, 3.5 Min cycle	JESD22-A105	8572 cycles	0/154
Temperature Cycle	-65°C, 150°C	JESD22-A104	500 cycles	0/154
Resistance to Solder Heat	260°C	JESD22-B106	10 sec	0/60

Qualification Plan	Device	Package	Process	No. of Lots
Q20140105A	NDP7060	TO220	3.8M Cells Nch	3

Test Description:	Condition:	Standard :	Duration:	Results:
Temperature Cycle	-65C, 150C	JESD22-A104	500 cycles	0/231
High Temperature Storage Life	175C	JESD22-A103	1000 hrs	0/231
Power Cycle	Delta 100C, 3.5 Min On/Off	JESD22-A122	8572 cycles	0/231
Highly Accelerated Stress Test	130C, 85%RH, 42V	JESD22-A110	96 hrs	0/231
High Temperature Gate Bias	175C, 20V	JESD22-A108	1000 hrs	0/231
High Temperature Reverse Bias	175C, 48V	JESD22-A108	1000 hrs	0/231
Resistance to Solder Heat	270C	JESD22-B106	15 sec	0/90

Qualification Plan	Device	Package	Process	No. of Lots
Q20140168	FDB8030L	TO263	PT1 N	3

Test Description:	Condition:	Standard:	Duration:	Results:
MSL1 Precondition	260°C, 3 cycles	JESD22-A113	NA	0/948
Highly Accelerated Stress Test	130°C, 85%RH, Vr = 24V	JESD22-A110	96 hrs	0/237
High Temperature Gate Bias	175°C, Vgs = 20V	JESD22-A108	1000 hrs	0/237
High Temperature Reverse Bias	175°C, Vr = 24V	JESD22-A108	1000 hrs	0/237
High Temperature Storage Life	175°C	JESD22-A103	1000 hrs	0/237
Power Cycle	Delta 100°C, 3.5 Min cycle	JESD22-A105	8572 cycles	0/237
Temperature Cycle	-65°C, 150°C	JESD22-A104	500 cycles	0/237
Resistance to Solder Heat	260°C	JESD22-B106	10 sec	0/90

Qualification Plan	Device	Package	Process	No. of Lots
Q20140168	FDS6975_SBAM003	SO8	PT1 P	1

Test Description:	Condition:	Standard:	Duration:	Results:
MSL1 Precondition	260°C, 3 cycles	JESD22-A113	NA	0/395
Highly Accelerated Stress Test	130°C, 85%RH, Vr = -24V	JESD22-A110	96 hrs	0/79
High Temperature Gate Bias	150°C, Vgs = -20V	JESD22-A108	1000 hrs	0/79
High Temperature Reverse Bias	150°C, Vr = -30V	JESD22-A108	1000 hrs	0/79
High Temperature Storage Life	150°C	JESD22-A103	1000 hrs	0/79
Power Cycle	Delta 100°C, 2 Min cycle	JESD22-A105	15000 cycles	0/79
Temperature Cycle	-55°C, 150°C	JESD22-A104	1000 cycles	0/79
Unbiased Highly Accelerated Stress Test	130°C, 85%RH	JESD22-A118	96 hrs	0/79
Resistance to Solder Heat	260°C	JESD22-B106	10 sec	0/30

Qualification Plan	Device	Package	Process	No. of Lots
Q20140168	FDD3510H	D-PAK	PT1 N and PT1 P	2

Test Description:	Condition:	Standard:	Duration:	Results:
MSL1 Precondition	260°C, 3 cycles	JESD22A-113	NA	0/800
Temperature Cycle	-55°C, 150°C	JESD22-A104	1000 cycles	0/154
High Temperature Storage Life	150°C	JESD22-A103	1000 hrs	0/154
Power Cycle	Delta 100°C, 2 Min On/Off	JESD22-A122	10000 cycles	0/154
Highly Accelerated Stress Test	130°C, 85%RH, 42V	JESD22-A110	96 hrs	0/154
Unbiased Highly Accelerated Stres	130°C, 85%RH,	JESD22-A118	96 hrs	0/154
High Temperature Gate Bias	150°C, 20V	JESD22-A108	1000 hrs	0/154
High Temperature Reverse Bias	150°C, 80V	JESD22-A108	1000 hrs	0/154
Resistance to Solder Heat	270°C	JESD22-B106	15 sec	0/10

Qualification Plan	Device	Package	Process	No. of Lots
Q20140168	FDC2612	SSOT6	PT1 N	2

Test Description:	Condition:	Standard:	Duration:	Results:
MSL1 Precondition	260°C, 3 cycles	JESD22-A113	NA	0/616
Highly Accelerated Stress Test	130°C, 85%RH, Vr = 42V	JESD22-A110	96 hrs	0/154
High Temperature Gate Bias	150°C, Vgs = 20V	JESD22-A108	1000 hrs	0/154
High Temperature Reverse Bias	150°C, Vr = 160V	JESD22-A108	1000 hrs	0/154
High Temperature Storage Life	150°C	JESD22-A103	1000 hrs	0/154
Power Cycle	Delta 100CC, 2.0 Min cycle	JESD22-A105	10000 cycles	0/154
Temperature Cycle	-65°C, 150°C	JESD22-A104	500 cycles	0/154
Resistance to Solder Heat	260°C	JESD22-B106	10 sec	0/60

Qualification Plan	Device	Package	Process	No. of Lots
Q20140111C	FDS4675	SOIC 8L	PT2 P	3

Test Description:	Condition:	Standard:	Duration:	Results:
MSL1 Precondition	260C, 3 cycles	JESD22-A113	NA	0/924
MSL1	260C, 3 cycles	J-STD_020	NA	0/66
Highly Accelerated Stress Test	130C, 85%RH, -32V	JESD22-A110	96 hrs	0/231
High Temperature Storage Life Test	150C	JESD22-A103	500 hrs	0/231
Unbias Highly Accelerated Stress Test	130C, 85%RH	JESD22-A118	96 hrs	0/231
Temperature Cycle	-65C, 150C	JESD22-A104	1000 cycles	0/231
High Temperature Gate Bias	150C, -20V	JESD22-A108	1000 hrs	0/231
High Temperature Reverse Bias	150C, -40V	JESD22-A108	1000 hrs	0/231
Power Cycle	Delta 100CC, 2 Min cycle	MIL-STD-750-1036	15000 cycles	0/231
Lead Fatigue	15Degree, 3X	JESD22-B105		0/90
Resistance to Solder Heat	Solder Dip = 260C	JESD22-B106	10 sec	0/30
Solderability	Condition C steam aging (8hrs), Condition A solder Dip (245 for 5 sec)	JESD22-B102	NA	0/30

Qualification Plan	Device	Package	Process	No. of Lots
Q20140111C	SI4467DY	SOIC 8L	PT2 P	2

Test Description:	Condition:	Standard:	Duration:	Results:
MSL3 Precondition	260C, 3 cycles	JESD22-A113	NA	0/616
MSL3	260C, 3 cycles	J-STD_020	NA	0/44
Highly Accelerated Stress Test	130C, 85%RH, -16V	JESD22-A110	96 hrs	0/154
High Temperature Storage Life Test	150C	JESD22-A103	500 hrs	0/154
Unbias Highly Accelerated Stress Test	130C, 85%RH	JESD22-A118	96 hrs	0/154
Temperature Cycle	-65C, 150C	JESD22-A104	1000 cycles	0/154
High Temperature Gate Bias	150C, -8V	JESD22-A108	1000 hrs	0/154
High Temperature Reverse Bias	150C, -20V	JESD22-A108	1000 hrs	0/154
Power Cycle	Delta 100CC, 2 Min cycle	MIL-STD-750-1036	15000 cycles	0/154
Lead Fatigue	15Degree, 3X	JESD22-B105		0/60
Resistance to Solder Heat	Solder Dip = 260C	JESD22-B106	10 sec	0/20
Solderability	Condition C steam aging (8hrs), Condition A solder Dip (245 for 5 sec)	JESD22-B102	NA	0/20