Product Bulletin

Document #:PB24260Z
Issue Date:08 Sep 2021

Title of Change:	ASX344AT Datasheet Update
Effective date:	08 Sep 2021
Contact information:	Contact your local onsemi Sales Office or Tom.Humphrey@onsemi.com
Type of notification:	This Product Bulletin is for notification purposes only. onsemi will proceed with implementation of this change upon publication of this Product Bulletin.
Change Category:	Documentation Change
Change Sub-Category(s):	Datasheet/Product Doc change

Sites Affected:

onsemi Sites	**External Foundry/Subcon Sites**
None	None

Description and Purpose:

ASX344AT Datasheet was updated with correct information. This change reduces the maximum EXTCLK frequency to 27Mhz (From 54Mhz) and maximum rise and fall time.

1. Updated Table 5, Corrected EXTCLK limit to recommended 27Mhz.

Old Table 5:

Table 5. PARALLEL DIGITAL OUTPUT I/O TIMING
(f_{EXTCLK} = 27 MHz; VDD = 1.8 V; VDD_IO = 2.8 V; VAA = 2.8 V; VAA_PIX = 2.8 V; VDD_PLL = 2.8 V; VDD_DAC = 2.8 V; Default slew rate)

Signal	Parameter	Conditions	Min	Typ	Max	Unit
EXTCLK	f_{extclk}		6	27	54	MHz
	t_{extclk_period}		18.52	37	166.67	ns
	Duty cycle		45	50	55	%
PIXCLK	f_{pixclk}		6	27	54	MHz
	t_{pixclk_period}		18.52	37.04	166.67	ns
	Duty cycle		45	50	55	%
DATA[7:0]	$t_{pixclkf\_dout}$		1.55	–	3.5	ns
	t_{dout_su}		18	–	20	ns
	t_{dout_ho}		18	–	20	ns
FV / LV	$t_{pixclkf\_fvlv}$		1.6	–	3.05	ns
	t_{fvlv_su}		16	–	19	ns
	t_{fvlv_ho}		16	–	19	ns

14. PIXCLK can be inverted from the default by programming R0x0016[14].

New Table 5 :

Table 5. PARALLEL DIGITAL OUTPUT I/O TIMING
(f_{EXTCLK} = 27 MHz; VDD = 1.8 V; VDD_IO = 2.8 V; VAA = 2.8 V; VAA_PIX = 2.8 V; VDD_PLL = 2.8 V; VDD_DAC = 2.8 V; Default slew rate)

Signal	Parameter	Conditions	Min	Typ	Max	Unit
EXTCLK	f_{extclk}		6	27	27	MHz
	Duty cycle		45	50	55	%
	t_{rise_time}	10% to 90% V_{DDIO}	–	–	3	ns
	t_{fall_time}	90% to 10% V_{DDIO}	–	–	3	ns
PIXCLK	f_{pixclk}		6	27	54	MHz
	Duty cycle		45	50	55	%
DATA[7:0]	$t_{pixclkf\_dout}$		1.55	–	3.5	ns
	t_{dout_su}		18	–	20	ns
	t_{dout_ho}		18	–	20	ns
FV / LV	$t_{pixclkf\_fvlv}$		1.6	–	3.05	ns
	t_{fvlv_su}		16	–	19	ns
	t_{fvlv_ho}		16	–	19	ns

14. PIXCLK can be inverted from the default by programming R0x0016[14].

There is no form, fit, or function change to the physical part.

List of Affected Standard Parts:

***Note**: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal**.*

ASX344ATSC00XUEA0-TRBR	ASX344ATSC00XUEA0-TPBR	ASX344ATSC00XUEA0-DRBR
ASX344ATSC00XUEA0-DPBR		