ON Semiconductor®

Product Bulletin

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Title of Change:	AR0141CS Datasheet Update.
Effective date:	20 Mar 2020
Contact information:	Contact your local ON Semiconductor Sales Office or Sonya.Yip@onsemi.com
Type of notification:	This Product Bulletin is for notification purposes only. ON Semiconductor will proceed with implementation of this change upon publication of this Product Bulletin.
Change Category:	Documentation Change
Change Sub-Category(s):	Datasheet/Product Doc change

Sites Affected:

ON Semiconductor Sites	External Foundry/Subcon Sites
None	None

Description and Purpose:

The AR0141CS Datasheet has been updated. These changes do not affect form, fit, or function of the product.

AR0141CS Datasheet Changes

1. Updated Table 2, "Available Part Numbers"

2. Updated Power-Up Sequence

Old Power-Up Sequence:

Power−Up Sequence

The recommended power−up sequence for the AR0141CS is shown in Figure 49. The available power supplies (VDD_IO, VDD, VDD_SLVS, VDD_PLL, VAA, VAA_PIX) must have the separation specified below.

1. Turn on VDD_PLL power supply
2. After 100 µs, turn on VAA and VAA_PIX power supply
3. After 100 µs, turn on VDD_IO power supply
4. After 100 µs, turn on VDD power supply
5. After 100 µs, turn on VDD_SLVS power supply
6. After the last power supply is stable, enable EXTCLK
7. Assert RESET_BAR for at least 1 ms. The parallel interface will be tri−stated during this time
8. Wait 1800 EXTCLKs for internal initialization into software standby
9. Initiate load of OTPM data by setting R0x304A = 0x0010
10. Wait for 185135 EXTCLKs for a full OTPM loading
11. Configure PLL, output, and image settings to desired values
12. Wait 1ms for the PLL to lock
13. Set streaming mode (R0x301A[2] = 1)

New Power-Up Sequence:

Power−Up Sequence

The recommended power−up sequence for the AR0141CS is shown in Figure 49. The available power supplies (VDD_IO, VDD, VDD_SLVS, VDD_PLL, VAA, VAA_PIX) must have the separation specified below.

1. Turn on VDD_PLL power supply
2. After 100 µs, turn on VAA and VAA_PIX power supply
3. After 100 µs, turn on VDD_IO power supply
4. After 100 µs, turn on VDD power supply
5. After 100 µs, turn on VDD_SLVS power supply
6. After the last power supply is stable, enable EXTCLK
7. Assert RESET_BAR for at least 1 ms. The parallel interface will be tri−stated during this time
8. Wait 1800 EXTCLKs for internal initialization into software standby
9. Initiate load of OTPM data by setting R0x304A = 0x0010
10. Wait for 200000 EXTCLKs for a full OTPM loading
11. Configure PLL, output, and image settings to desired values
12. Wait 1ms for the PLL to lock
13. Set streaming mode (R0x301A[2] = 1)

3. Updated Table 36, "Power-Up Sequence"

Old Table 36:

Table 36. POWER−UP SEQUENCE

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_PLL to VAA/VAA_PIX (Note 3)	t0	0	100	–	μs
VAA/VAA_PIX to VDD_IO	t1	0	100	–	μs
VDD_IO to VDD	t2	0	100	–	μs
VDD to VDD_SLVS	t3	0	100	–	μs
Xtal Settle Time	tx	–	30 (Note 1)	–	ms
Hard Reset	t4	1 (Note 2)	–	–	ms
Internal Initialization	t5	1800	–	–	EXTCLK
OTPM Loading	t6	185135	–	–	EXTCLK
PLL Lock Time	t7	1	–	–	ms

1. Xtal settling time is component−dependent, usually taking about 10 – 100 ms.
2. Hard reset time is the minimum time required after power rails are settled. In a circuit where Hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.
3. It is critical that VDD_PLL is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that VDD_PLL is powered after other supplies then sensor may have functionality issues and will experience high current draw on this supply.

New Table 36:

Table 36. POWER−UP SEQUENCE

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_PLL to VAA/VAA_PIX (Note 31)	t0	0	100	–	μs
VAA/VAA_PIX to VDD_IO	t1	0	100	–	μs
VDD_IO to VDD	t2	0	100	–	μs
VDD to VDD_SLVS	t3	0	100	–	μs
Xtal Settle Time	tx	–	30 (Note 29)	–	ms
Hard Reset	t4	1 (Note 30)	–	–	ms
Internal Initialization	t5	1800	–	–	EXTCLK
OTPM Loading	t6	200000	–	–	EXTCLK
PLL Lock Time	t7	1	–	–	ms

29. Xtal settling time is component−dependent, usually taking about 10 – 100 ms.
30. Hard reset time is the minimum time required after power rails are settled. In a circuit where Hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.
31. It is critical that VDD_PLL is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that VDD_PLL is powered after other supplies then sensor may have functionality issues and will experience high current draw on this supply.

List of Affected Standard Parts:

***Note**: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal**.*

AR0141CS2C00SUEA0-DR	AR0141CS2C00SUEA0-DP	AR0141CS2M00SUEA0-DPBR
AR0141CSSM21SUEA0-DPBR	AR0141CSSM21SUEA0-TPBR	AR0141CS2M00SUEA0-TPBR
AR0141IRSH00SUEA0-DR		