ON Semiconductor

Update Notification

Document # : FPCN20828Z1
Issue Date: 16 December 2015

Title of Change:	Update to FPCN20828Z - Change Lead frame from N03503D003 to N03503D005 For TSOP6 – NLVAS4599DTT1G. Change to Proposed First Ship Date.
Proposed first ship date:	2 December 2016
Contact information:	Contact your local ON Semiconductor Sales Office or <ricardo.avila@onsemi.com>
Samples:	Contact your local ON Semiconductor Sales Office
Additional Reliability Data:	Contact your local ON Semiconductor Sales Office or <jose.aguilar@onsemi.com>
Type of notification:	ON Semiconductor will consider this change accepted, unless an inquiry is made in writing within 30 days of delivery of this notice. To do so, contact <PCN.Support@onsemi.com>.
Change category:	☐ Wafer Fab Change ☒ Assembly Change ☐ Test Change ☐ Other _____

Change Sub-Category(s):

☐ Manufacturing Site Change/Addition
☐ Manufacturing Process Change
☒ Material Change
☐ Product specific change
☐ Datasheet/Product Doc change
☐ Shipping/Packaging/Marking
☐ Other: _____

Sites Affected:

☐ All site(s) ☐ not applicable
☒ ON Semiconductor site(s) : ON Seremban, Malaysia
☐ External Foundry/Subcon site(s)

Description and Purpose:

FPCN20828Z was published in March 2015 announcing the Change in Lead frame For TSOP6 – NLVAS4599DTT1G from N03503D003 to Lead frame N03503D005.

ON Semiconductor is issuing this UN to announce the new Proposed First Ship date due to the completion of additional reliability testing for TC and HAST to fulfill AEC-100 and PPAP requirements.

For the introduction of a new lead frame for the products listed using the TSOP-6 Package Case Outline 318G-02, the flag and Pin 3 are connected on this lead frame, setting the die bond pad, the substrate, flag and pin at the same potential (Gnd).
There are no changes to Electrical performance, Case outline or Foot print.

#	Test	Name	Test Conditions	End Point Req's	Test Results (rej/ss)		
					Read Point	Lot A	Lot B
1	PC	MSL1 preconditioning	3 IR @ 260 °C	c = 0, Room		all	all
2	TC-PC	Temperature Cycle	-65/+150 C	c = 0, Room, Hot	1000cyc	0/84	0/84
3	HAST-PC	Highly Accelerated Stress Test	Temp= +130°C, RH=85% , p = 18.8 psig, bias	c = 0, Room, Hot	96hrs	0/84	0/84
4	UHAST-PC	Unbiased Highly Accelerated Stress Test	Temp= +130°C, RH=85% , p = 18.8 psig, unbiased	c = 0, Room	96hrs	0/84	0/84

Based on the results presented here, device NLAS4599DTT1G housed in package TSOP6 with lead frame N03503D005, using technology TS60, assembled and tested at Seremban, Malaysia has met and exceeded the requirements and it is considered qualified per ON Semiconductor's Product Qualification Specifications, 12MSB17722C.

NOTE: Attached AEC Q100 Qual

1. Download pdf copy of the PCN to your computer
2. Open the downloaded pdf copy of the PCN
3. Click on the paper clip icon available on the menu provided in the left/bottom portion of the screen to reveal the Attachment field
4. Then click on the attached file/s

List of affected Standard Parts:

NLVAS4599DTT1G