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PCN# :P221A
Issue Date : Mar. 01, 2012

DESIGN/PROCESS CHANGE NOTIFICATION

This is to inform you that a change is being made to the products listed below.

Unless otherwise indicated in the details of this notification, the identified change will have no impact on product quality, reliability, electrical, visual or mechanical performance and affected products will remain fully compliant to all published specifications. Products incorporating this change may be shipped interchangeably with existing unchanged products.

This change is planned to take effect in 90 calendar days from the date of this notification. Please work with your local Fairchild Sales Representative to manage your inventory of unchanged product if your evaluation of this change will require more than 90 calendar days.

Please contact your local Customer Quality Engineer within 30 days of receipt of this notification if you require any additional data or samples. Alternatively, you may send an email request for data, samples or other information to PCNSupport@fairchildsemi.com.

Implementation of change:

Expected First Shipment Date for Changed Product :May. 30, 2012

Expected First Date Code of Changed Product :2412

Last Date for Shipment of Unchanged Product :May. 30, 2012

Description of Change (From) :
Current devices built on 6inch wafer line at Salt Lake Fab.

Description of Change (To) :
Devices will also be built on 8inch wafer line at foundry TSMC.

Reason for Change:

Fairchild Semiconductor is increasing wafer capacity by qualifying the process for the affected FSIDs at Taiwan Semiconductor Manufacturing Company Limited, Taiwan. Quality and reliability will remain at the highest standards already demonstrated with Fairchild's existing products. The reliability qualification results used to qualify the wafer fabrication line is summarized below. The specific groups of products/MOSFET technologies are listed in the affected FSIDs list. Design, die size, and layout of the affected products will remain unchanged. There are no changes in the datasheet or electrical performance between products manufactured at the current or the alternative wafer fabrication lines. Products from the two fabrication lines may be shipped interchangeably.

Affected Product(s):

FDMA0100	FDMA0102	FDMA7630
FDMA7632	FDMA7670	FDMA7672
FDMC0223	FDMC0223S	FDMC0224
FDMC0225	FDMC0225S	FDMC7200
FDMC7200S	FDMC7200_F073	FDMC7200_F128
FDMC7664	FDMC7672	FDMC7672S
FDMC7672S_F125	FDMC7672S_F126	FDMC7672S_F127
FDMC7672_F073	FDMC7672_F125	FDMC7680
FDMC7692	FDMC7692S	FDMC7692S_F125
FDMC7692S_F126	FDMC7692S_F127	FDMC7692_F073
FDMC7692_F126	FDMC7692_F127	FDMC7692_SN00195
FDMC7692_SN00203	FDMC7696	FDMC8200
FDMC8200S	FDMC8200_F128	FDML7610AS
FDML7610S	FDMS0308S_SN00174	FDMS0312S_SN00177
FDMS0346	FDMS0347	FDMS0349
FDMS0352S	FDMS0353S	FDMS0354S
FDMS0355S	FDMS7578	FDMS7580
FDMS7600AS	FDMS7602S	FDMS7603S
FDMS7608S	FDMS7620S	FDMS7621S
FDMS7656AS	FDMS7658AS	FDMS7658AS_SN00232
FDMS7660	FDMS7660AS	FDMS7670
FDMS7670AS	FDMS7672	FDMS7672AS
FDMS7676	FDMS7680	FDMS7681
FDMS7682	FDMS7692	FDMS7692A
FDMS7694	FDMS7694_SN00176	FDMS7696A
FDMS7698	FDMS7700S	FDMS8020

Qualification Plan	Device	Package	Process	No. of Lots
Q20120019	FDMC7672	MLP 3.3x3.3 In 8-lead	PT7	3

Test Description:	Condition:	Standard :	Duration:	Results:
MSL1 Precondition	260C, 3 cycles	**JESD22-A113**		0/474
MSL1	260C, 3 cycles	**J-STD_020**		0/66
Highly Accelerated Stress Test	130C, 85%RH,24V	**JESD22-A110**	96 hrs	0/237
High Temperature Storage Life	150C	**JESD22-A103**	1000 hrs	0/237
High Temperature Gate Bias	150C,20V	**JESD22-A108**	1000 hrs	0/237
High Temperature Reverse Bias	150C,24V	**JESD22-A108**	1000 hrs	0/237
Temperature Cycle	-65C, 150C	**JESD22-A104**	500 cycles	0/237
PRCL	Delta 100CC, 2 Min cycle	**JESD22-A122**	10000 cycles	0/79
Bond Pull	9.0g	**JESD22-C100**		0/66
Bond Shear	90g	**AEC-Q100-001**		0/66
Die Shear	0.4g/mil sq	**MIL-STD-883-2019**		0/15
Resistance to Solder Heat	260°C	**JESD22-B106**		0/22

Qualification Plan	Device	Package	Process	No. of Lots
QP10330840-I	FDMS0302S	PQFN 5x6	PT7 SyncFET	3

Test Description:	Condition:	Standard :	Duration:	Results:
MSL1 Precondition	260°C, 3 pass	**JESD22-A113**		0/474
Highly Accelerated Stress Test	130°C, 85%RH, Vr = 24V	**JESD22-A110**	96 hrs	0/237
High Temperature Storage Life	175°C	**JESD22-A103**	500 hrs	0/237
Power Cycle	T on/off = 2min, Delta Tj = 100°C	**JESD22-A105**	10000 cycles	0/237
Temperature Cycle	-65°C to 150°C, 30min/cycle	**JESD22-A104**	500 cycles	0/237
High Temperature Reverse Bias	125°C, Vr = 24V	**JESD22-A108**	1000 hrs	0/237
High Temperature Gate Bias	150°C, Vgs = 20V	**JESD22-A108-B**	1000 hrs	0/237
Resistance to Solder Heat	260°C	**JESD22-B106**	10 sec	0/90