PCN# : P555AAB
Issue Date : May. 14, 2015

Information Only Notification

This is to inform you that a change is being made to the following products.

This is a minor change that has no impact on product quality, reliability, electrical or mechanical performance. Affected products will remain fully compliant to all published specifications. Notification is being made for informational purposes only and there is no approval required. Products incorporating this change may be shipped interchangeably with existing unchanged products.

Please contact your local Customer Quality Engineer if you have any questions regarding this notification. Alternatively, you may send an email request for information to PCNSupport@fairchildsemi.com.

Implementation of change:

Expected First Shipment Date for Changed Product : May. 15, 2015

Expected First Date Code of Changed Product :1520

Description of Change (From) :
Datasheet Change Only:

EN signal operation description and truth tables (Table 1 & 2) on page 11 and EN (Input) on page 17
Currently stated as:
EN (Enable)
The driver can be disabled by pulling V_{CC} under the UVLO-falling threshold regardless of the PWM and EN input states. The driver can be enabled by raising V_{CC} above the UVLO-rising threshold. The driver IC has less than 2 mA shutdown current when it is disabled. Once the driver is re-enabled, it takes a typical of 25 ns startup time.

Table 1. UVLO and Enable Logic

UVLO	EN	Driver State
0	X	Disabled (GH & GL = 0)
1	X	Enabled (*see Table 2*)

Table 2. EN / PWM / 3-State Logic States

EN	PWM	GH	GL
0	3-State	0	0
0	0	0	0
0	1	1	0
1	3-State	0	0
1	0	0	1
1	1	1	0

EN (Input)
The EN pin has internal 1 k and 250 k pull-down resistors, so it needs to be pulled-up to V_{CC} with an external resistor or connected to the controller or system to follow up the command from them. When the EN is HIGH and the PWM is LOW, the driver outputs GL HIGH. When the PWM is HIGH and the EN is HIGH or LOW, the driver outputs GH HIGH.

Description of Change (To) :

1. Updated table 1 to add additional Disabled state
2. Update table 2 on 3rd row to reference when EN is LOW, both GH & GL are LOW regardless of UVLO/PWM HIGH or LOW.
3. Updated the EN (Enable) Description on page 11 and EN (Input) on page 17

EN (Enable)
When the VCC is over than UVLO, the driver can be enabled by pulling EN pin over high threshold. The driver is disabled by pulling EN pin under low threshold. The driver IC commands off the high side and low side MOSFETs when the driver is disabled. The driver IC has less than 2 mA shutdown current when it is disabled. Once the driver is re-enabled, it takes a typical of 25 ns startup time.

Table 1. UVLO and Enable Logic

UVLO	EN	Driver State
0	X	Disabled (GH & GL = 0)
1	0	Disabled (GH & GL = 0)
1	1	Enabled (*see Table 2*)

Table 2. EN / PWM / 3-State Logic States

EN	PWM	GH	GL
0	3-State	0	0
0	0	0	0
0	1	0	0
1	3-State	0	0
1	0	0	1
1	1	1	0

EN (Input)
The EN pin has internal 1 k and 250 k pull-down resistors, so it needs to be pulled-up to V_{CC} with an external resistor or connected to the controller or system to follow up the command from them. When the EN is HIGH and the PWM is LOW, the driver outputs GL HIGH. When the PWM is HIGH and the EN is HIGH, the driver outputs GH HIGH.

Reason for Change:
Correction to Datasheet description for EN signal operation and Truth Tables Logic States

Affected Product(s): Please refer to the list of affected products in the addendum attached in the PCN email you received. This list is based on an analysis of your company's procurement history.