

FINAL PRODUCT/PROCESS CHANGE NOTIFICATION #16923

Generic Copy

Issue Date: 25-Oct-2012

<u>TITLE</u>: Phase 1 Copper Wire for VHVIC Products in SOIC and TSSOP packages in Carmona, Philippines

PROPOSED FIRST SHIP DATE: 25-Jan-2013

AFFECTED CHANGE CATEGORY(S): Assembly Process

FOR ANY QUESTIONS CONCERNING THIS NOTIFICATION:

Contact your local ON Semiconductor Sales Office or <Scott.Brow@onsemi.com>

SAMPLES: Contact your local ON Semiconductor Sales Office

ADDITIONAL RELIABILITY DATA: Available

Contact your local ON Semiconductor Sales Office or <Ken.Fergus@onsemi.com>

NOTIFICATION TYPE:

Final Product/Process Change Notification (FPCN)

Final change notification sent to customers. FPCNs are issued at least 90 days prior to implementation of the change.

ON Semiconductor will consider this change approved unless specific conditions of acceptance are provided in writing within 30 days of receipt of this notice. To do so, contact <quality@onsemi.com>.

DESCRIPTION AND PURPOSE:

A General Announcement (GA#16200) was published on 1-29-09 regarding the ongoing Copper Wirebond conversion program at ON Semiconductor. This is a FPCN to notify customers of its plan to qualify Copper Wire (in place of Gold Wire) on SOIC and TSSOP packages assembled at the Carmona, Philippine assembly location for the VHVIC products listed in this announcement.

Reliability Qualification and full electrical characterization over temperature has now been completed on the designated package qualification vehicles.





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RELIABILITY DATA SUMMARY:

Reliability Test Results:

# Test Page Test (n/) (n	NCP12000									
Note Note <t< th=""><th></th><th></th><th>Name</th><th>Test Conditions</th><th>End Point Req's</th><th></th><th>(rej/ss)</th><th>(rej/ss)</th><th>(rej/ss)</th><th>(rej/ss)</th></t<>			Name	Test Conditions	End Point Req's		(rej/ss)	(rej/ss)	(rej/ss)	(rej/ss)
1 Prep testing Various Electrical Done Done Done Done A1 PC MSL1Preconditioning MSL120C c-0, Room Pol PC 0/240							Lot A	Lot B	Lot C	Control
Al. PC MSL 1 Preconditioning MSL 3 26C c=0, Room Post PC 0/240 0/280 0/80			Sample preparation and initial part			Initial				
A3 PC-TC Preconditioned Temperature Cycle -55C/+150C c-0, Room 500 cycles 0/80 <t< td=""><td>1</td><td>Prep</td><td>testing</td><td>Various</td><td></td><td>Electrical</td><td>Done</td><td>Done</td><td>Done</td><td>Done</td></t<>	1	Prep	testing	Various		Electrical	Done	Done	Done	Done
A3 PC-TC Preconditioned Temperature Cycle -55C/+150C c-0, Room 500 cycles 0/80 <t< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<>										
A2 PC-HAST Precond Highly Accelerated Stress Test $T_n = 130C/85KHH, 18.8psig, with bias c=0, Room 96 hours 0/80$	A1	PC	MSL 1 Preconditioning	MSL1 260C	c=0, Room	Post PC	0/240	0/240	0/240	0/240
A2 PC-HAST Precond Highly Accelerated Stress Test $T_n = 130C/85KHH, 18.8psig, with bias c=0, Room 96 hours 0/80$										
A2 PC-HAST Precond Highly Accelerated Stress Test $T_n = 130C/855KH, 18.8prig, with bias Ced, Room 96 hours 0/80$	A3	PC-TC	Preconditioned Temperature Cycle	-65C/+150C	c=0, Room	500 cycles	0/80	0/80	0/80	0/80
A2 PC-HAST Precond Highly Accelerated Stress Test with bias c=0, Room 66 hours 0/80<						1000 cycles	0/80	0/80	0/80	0/80
A2 PC-HAST Precond Highly Accelerated Stress Test with bias c=0, Room 66 hours 0/80<		-					-			
A4 PC-UHAST Precond Highly Accelerated Stress Test T _A = 130C/85%RH; 18.8psig, no bias C=0, Room 96 hours 0/80				T _A = 130C/85%RH, 18.8psig,						
A4 PC: UHAST Precend Highly Accelerated Stress Test bias c=0, Room 96 hours 0/80 0/80 0/80 0/80 A6 HTSL High Temperature Storage Life $T_A = 150C$ c=0, Room 504 hours 0/80 <td>A2</td> <td>PC-HAST</td> <td>Precond Highly Accelerated Stress Test</td> <td>with bias</td> <td>c=0, Room</td> <td>96 hours</td> <td>0/80</td> <td>0/80</td> <td>0/80</td> <td>0/80</td>	A2	PC-HAST	Precond Highly Accelerated Stress Test	with bias	c=0, Room	96 hours	0/80	0/80	0/80	0/80
A4 PC: UHAST Precend Highly Accelerated Stress Test bias c=0, Room 96 hours 0/80 0/80 0/80 0/80 A6 HTSL High Temperature Storage Life $T_A = 150C$ c=0, Room 504 hours 0/80 <td></td>										
A6 HTSL High Temperature Storage Life T _n = 150C c=0, Room Softwar 0/80				T _A = 130C/85%RH, 18.8psig, no						
A6 HTSL High Temperature Storage Life T_n = 150C c=0, Room Software V/R0 0/80	A4	PC-UHAST	Precond Highly Accelerated Stress Test	bias	c=0, Room	96 hours	0/80	0/80	0/80	0/80
Interpret in the second sec										
Interpret in the second sec	A6	HTSL	High Temperature Storage Life	T _A = 150C	c=0, Room	504 hours	0/80	0/80	0/80	0/80
B1 HTOL High Temp Op Life $T_{a} = 150C$ for 1008hrs with bias c=0, Room 504 hours 0/80 0/10						1008 hours	0/80	0/80	0/80	0/80
C3 Solderability (>95% coverage) 1008 hours 0/80 0/80 0/80 0/80 C3 SD Solderability (>95% coverage) 10 units period Pass 0/10 <td></td>										
C3 Solderability (>95% coverage) 1008 hours 0/80 0/80 0/80 0/80 C3 SD Solderability (>95% coverage) 10 units period Pass 0/10 <td>B1</td> <td>HTOL</td> <td>High Temp Op Life</td> <td>$T_{A} = 150C$ for 1008hrs with bias</td> <td>c=0. Room</td> <td>504 hours</td> <td>0/80</td> <td>0/80</td> <td>0/80</td> <td>0/80</td>	B1	HTOL	High Temp Op Life	$T_{A} = 150C$ for 1008hrs with bias	c=0. Room	504 hours	0/80	0/80	0/80	0/80
C3 Solderability (>95% coverage) Interpretation Pass 0/10				· A	,					
RSH Resistance to solder heat JESD22 - B106 260C Immersion C=0, Room Pass 0/10 0/10 0/10 C4 BPS Wire Bond Pull Test Cpk>1.33 5 parts minumum 30 bonds 0/30 0/30 0/30 0/30 C5 WBS Wire Bond Shear Test Cpk>1.33 5 parts minumum 30 bonds 0/30 0/						1000 110 013	0,00	0/00	0,00	0,00
RSH Resistance to solder heat JESD22 - B106 260C Immersion C=0, Room Pass 0/10 0/10 0/10 C4 BPS Wire Bond Pull Test Cpk>1.33 5 parts minumum 30 bonds 0/30 0/30 0/30 0/30 C5 WBS Wire Bond Shear Test Cpk>1.33 5 parts minumum 30 bonds 0/30 0/	C3	SD	Solderability (>95% coverage)		10 units per lot	Pass	0/10	0/10	0/10	0/10
C4 BPS Wire Bond Pull Test Cpk>1.33 5 parts minumum 30 bonds 0/30 0/30 0/30 0/30 C5 WBS Wire Bond Shear Test Cpk>1.33 5 parts minumum 30 bonds 0/30		30			10 units per lot	1 435	0/10	0/10	0/10	0/10
C4 BPS Wire Bond Pull Test Cpk>1.33 5 parts minumum 30 bonds 0/30 0/30 0/30 0/30 C5 WBS Wire Bond Shear Test Cpk>1.33 5 parts minumum 30 bonds 0/30		RSH	Resistance to solder heat	JESD22 - B106 260C Immersion	c=0. Room	Pass	0/10	0/10	0/10	0/10
CSWBSWire Bond Shear TestC pk>1.33S parts minumum30 bonds0/30 <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td><i>c, _c</i></td> <td><i>, </i></td> <td><i>•,</i> _•</td> <td>0, =0</td>							<i>c, _c</i>	<i>, </i>	<i>•,</i> _•	0, =0
CSWBSWire Bond Shear TestC pk>1.33S parts minumum30 bonds0/30 <td>C4</td> <td>BPS</td> <td>Wire Bond Pull Test</td> <td>Cpk>1.33</td> <td>5 parts minumum</td> <td>30 bonds</td> <td>0/30</td> <td>0/30</td> <td>0/30</td> <td>0/30</td>	C4	BPS	Wire Bond Pull Test	Cpk>1.33	5 parts minumum	30 bonds	0/30	0/30	0/30	0/30
NCP1217bGFR2GNameTest ConditionsEnd Point Req's ResultsTest Results(rej/ss) (rej/ss)(rej/ss) 								.,	-,	.,
NCP1217bGFR2GNameTest ConditionsEnd Point Req's ResultsTest Results(rej/ss) (rej/ss)(rej/ss)(rej/ss)(rej/ss)(rej/ss) (rej/ss) <t< td=""><td>C5</td><td>WBS</td><td>Wire Bond Shear Test</td><td>Cpk>1.33</td><td>5 parts minumum</td><td>30 bonds</td><td>0/30</td><td>0/30</td><td>0/30</td><td>0/30</td></t<>	C5	WBS	Wire Bond Shear Test	Cpk>1.33	5 parts minumum	30 bonds	0/30	0/30	0/30	0/30
#Test ResultsNameTest ConditionsEnd Point Reg's ResultsTest Results(rej/ss)(rej/s)(rej/ss) </td <td></td> <td></td> <td></td> <td>·</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>				·						
Image: Constraint of the second se	NCP12170	D65R2G								
Image: constraint of the second se	#	Test	Name	Test Conditions	End Point Req's	Test	(rej/ss)	(rej/ss)	(rej/ss)	(rej/ss)
NoteSample preparation and initial part testingVariousInitial $$ Initial ElectricalDoneDon						Results				
1PreptestingVariousElectricalDone </th <th></th> <th></th> <th></th> <th></th> <th></th> <th>Read Point</th> <th>Lot A</th> <th>Lot B</th> <th>Lot C</th> <th>Control</th>						Read Point	Lot A	Lot B	Lot C	Control
A1 PC MSL 1 Preconditioning MSL 1 260C c=0, Room Post PC 0/240			Sample preparation and initial part			Initial				
A3 PC-TC Preconditioned Temperature Cycle -65C/+150C c=0, Room 500 cycles 0/80	1	Prep	testing	Various		Electrical	Done	Done	Done	Done
A3 PC-TC Preconditioned Temperature Cycle -65C/+150C c=0, Room 500 cycles 0/80	-									
Image: Constraint of the second se	A1	PC	MSL 1 Preconditioning	MSL1 260C	c=0, Room	Post PC	0/240	0/240	0/240	0/240
Image: Constraint of the second se										
Image: series of the	A3	PC-TC	Preconditioned Temperature Cycle	-65C/+150C	c=0, Room					
A5 PC-UHAST Precond Highly Accelerated Stress Test T _A = 130C/85%RH, 18.8psig, no bias C=0, Room 96 hours 0/80 <t< td=""><td></td><td>-</td><td></td><td></td><td></td><td>1000 cycles</td><td>0/80</td><td>0/80</td><td>0/80</td><td>0/80</td></t<>		-				1000 cycles	0/80	0/80	0/80	0/80
A5 PC-UHAST Precond Highly Accelerated Stress Test T _A = 130C/85%RH, 18.8psig, no bias C=0, Room 96 hours 0/80 <t< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<>										
A5 PC-UHAST Precond Highly Accelerated Stress Test bias c=0, Room 96 hours 0/80 <	A4	PC-AC	Preconditioned Autoclave	T _A = 121C/100%RH, 15psig	c=0, Room	96 hours	0/80	0/80	0/80	0/80
A5 PC-UHAST Precond Highly Accelerated Stress Test bias c=0, Room 96 hours 0/80 <										
A6 HTSL High Temperature Storage Life $T_A = 150C$ c=0, Room 504 hours 0/80 0/10 0/10 0/10 0/10 0/10 0/10 0/10 0/10 0/10 0/10 0				T _A = 130C/85%RH, 18.8psig, no						
No. Open of the constraint	A5	PC-UHAST	Precond Highly Accelerated Stress Test	bias	c=0, Room	96 hours	0/80	0/80	0/80	0/80
No. Open of the constraint										
Image: Space state stat	A6	HTSL	High Temperature Storage Life	T _A = 150C	c=0, Room	504 hours	0/80	0/80	0/80	0/80
Image: Space state stat						1008 hours	0/80	0/80	0/80	0/80
RSH Resistance to solder heat JESD22 - B106 260C Immersion c=0, Room Pass 0/10										
C4 BPS Wire Bond Pull Test Cpk>1.33 5 parts minumum 30 bonds 0/30	C3	SD	Solderability (>95% coverage)		10 units per lot	Pass	0/10	0/10	0/10	0/10
		RSH	Resistance to solder heat	JESD22 - B106 260C Immersion	c=0, Room	Pass	0/10	0/10	0/10	0/10
C5 WBS Wire Bond Shear Test Cpk>1.33 5 parts minumum 30 bonds 0/30 0/30 0/30 0/30	C4	BPS	Wire Bond Pull Test	Cpk>1.33	5 parts minumum	30 bonds	0/30	0/30	0/30	0/30
C5 WBS Wire Bond Shear Test Cpk>1.33 5 parts minumum 30 bonds 0/30 0/30 0/30 0/30										
	C5	WBS	Wire Bond Shear Test	Cpk>1.33	5 parts minumum	30 bonds	0/30	0/30	0/30	0/30

ON Semiconductor



FINAL PRODUCT/PROCESS CHANGE NOTIFICATION #16923

ELECTRICAL CHARACTERISTIC SUMMARY:

There is no electrical characterization difference in products assembled with copper wire. Electrical data is available upon request.

CHANGED PART IDENTIFICATION:

Products affected on this FPCN will have part number date codes greater than WW03 2013.

List of affected General Parts:

NCP1207BDR2G	NCP1338DR2G
NCP1216AD100R2G	NCP1351ADR2G
NCP1216AD133R2G	NCP1351BDR2G
NCP1216AD65R2G	NCP1351CDR2G
NCP1216D100R2G	NCP1351DDR2G
NCP1216D133R2G	NCP1377BD1R2G
NCP1216D65R2G	NCP1377BDR2G
NCP1217AD100R2G	NCP1377D1R2G
NCP1217AD133R2G	NCP1377DR2G
NCP1217AD65R2G	NCP1395ADR2G
NCP1217D100R2G	NCP1395BDR2G
NCP1217D133R2G	NCP1605ADR2G
NCP1217D65R2G	NCP1605BDR2G
NCP1230D100R2G	NCP1605DR2G
NCP1230D133R2G	NCP1650DR2G
NCP1230D165R2G	NCP1651DR2G
NCP1230D65R2G	NCP1653ADR2G
NCP1308DR2G	NCP1653DR2G
NCP1337DR2G	NCP5181DR2G
	NCP1216AD100R2G NCP1216AD133R2G NCP1216AD65R2G NCP1216D100R2G NCP1216D133R2G NCP1216D133R2G NCP1216D65R2G NCP1217AD100R2G NCP1217AD133R2G NCP1217AD133R2G NCP1217D100R2G NCP1217D100R2G NCP1217D133R2G NCP1217D133R2G NCP1217D133R2G NCP1230D100R2G NCP1230D103R2G NCP1230D165R2G NCP1230D65R2G NCP1308DR2G

List of affected Customer Specific Parts:

SCY99006AR2G	SCY99008BR2G	SCY99058ADR2G		
SCY99006BR2G	SCY99008CR2G	SCY99062D100R2G		
SCY99007AR2G	SCY99008DR2G	SCY99062D133R2G		
SCY99007BR2G	SCY99008ER2G	SCY99062D65R2G		
SCY99007R2G	SCY99008R2G	SCY99063D65R2G		
SCY99008AR2G	SCY99056DR2G	SCY99100D100R2G		