Product Bulletin

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Issue Date:09 Aug 2022

Title of Change:	AR0820AT Datasheet Update
Effective date:	09 Aug 2022
Contact information:	Contact your local onsemi Sales Office or Joe.Faris@onsemi.com
Type of notification:	This Product Bulletin is for notification purposes only. onsemi will proceed with implementation of this change upon publication of this Product Bulletin.
Change Category:	Technical Documentation
Change Sub-Category(s):	Datasheet/Product Doc change

Sites Affected:

onsemi Sites	**External Foundry/Subcon Sites**
None	None

Description and Purpose:

1. In the old AR0820AT datasheet, the definition of the power-up sequence is ambiguous in the text description. The updated datasheet addresses this ambiguity by defining the time between supplies from the point of stability for the first supply, to the power supply enablement on the second supply. This also accounts for the possibility of different slew rates on different supplies.

Old

Power Up/Down Timing

Power Up

The available power supplies (VAA, VAA_PIX, VAA_OTPM, VDD, VDD_IO, VDD_PLL, VDD_PHY) must have the separation specified below.

1. Turn on VDD_IO and VDD_PLL (1.8 V or 2.8 V) power supply.
2. After 0 to 100 µs, turn on VAA, VAA_PIX and VAA_OTPM (2.8 V) power supply.
3. After 0 to 100 µs, turn on VDD and VDD_PHY (1.2V) power supply.
4. As the last power supply stabilizes, enable EXTCLK.
5. Assert RESET_BAR for at least 1ms.
6. After de−asserting RESET_BAR, wait for 222k clock cycles.
7. Configure part as desired and set streaming mode (Mode_Select or R0x301A[2]) = 1).
8. Wait for 1 ms for PLL lock to complete.

The AR0820 is now in streaming mode.

New

Power Up/Down Timing

Power Up

The available power supplies (VAA, VAA_PIX, VAA_OTPM, VDD, VDD_IO, VDD_PLL, VDD_PHY) must have the separation specified below.

1. Turn on VDD_IO and VDD_PLL (1.8 V or 2.8 V) power supply.
2. Power on VAA, VAA_PIX and VAA_OTPM (2.8 V) power supply such that VAA, VAA_PIX and VAA_OTPM reaches nominal voltage at the same time or after VDD_IO and VDD_PLL.
3. Power on VDD and VDD_PHY (1.2 V) power supply such that VDD and VDD_PHY reaches nominal voltage at the same time or after VAA, VAA_PIX and VAA_OPTM.
4. As the last power supply stabilizes, enable EXTCLK.
5. Assert RESET_BAR for at least 1ms.
6. After de−asserting RESET_BAR, wait for 222k clock cycles.
7. Configure part as desired and set streaming mode (Mode_Select or R0x301A[2]) = 1).
8. Wait for 1 ms for PLL lock to complete.

The AR0820 is now in streaming mode.

2. Updated Spectral Characteristics section with the latest quantum efficiency curves.

Old Figure 19

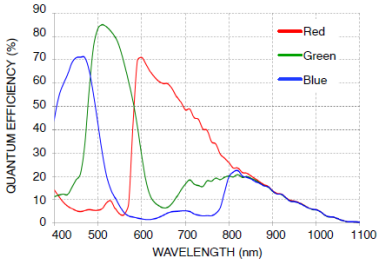

Figure 19. Quantum Efficiency – RGB Bayer

New Figure 19

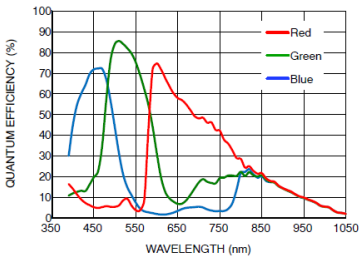

Figure 19. Quantum Efficiency – RGB Bayer

Old Figure 20

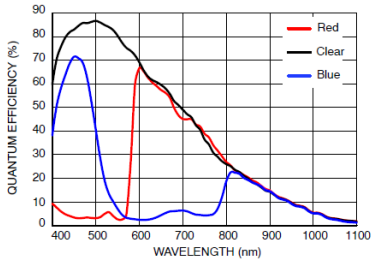

Figure 20. Quantum Efficiency – RCCB

New Figure 20

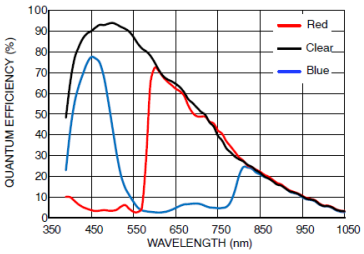

Figure 20. Quantum Efficiency – RCCB

Old Figure 21

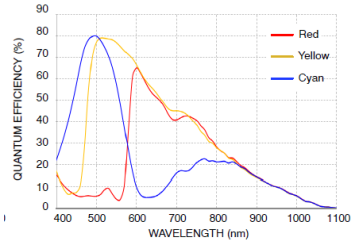

Figure 21. Quantum Efficiency – RYYCy

New Figure 21

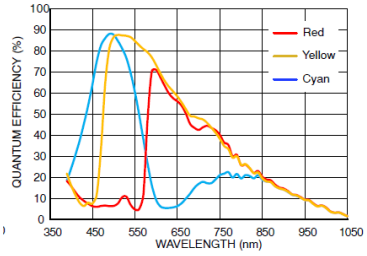

Figure 21. Quantum Efficiency – RYYCy

List of Affected Standard Parts:

***Note**: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal**.*

AR0820ATSB18XMEA0-DPBR	AR0820ATSB18XMEA0-DRBR	AR0820ATSC18XMEA0-DPBR
AR0820ATSC18XMEA0-TRBR	AR0820ATSC18XMEA0-TPBR	AR0820ATSC18XMEA0-DRBR
AR0820ATSB18XMEA0-TRBR	AR0820ATSB18XMEA0-TPBR	