



FINAL PRODUCT/PROCESS CHANGE NOTIFICATION #16446

Generic Copy

Issue Date: 03-Nov-2010

TITLE: Qualification of Gresham Fab to Source Kionix C4 Devices

PROPOSED FIRST SHIP DATE: 03-Feb-2011, or earlier at customer request.

AFFECTED CHANGE CATEGORY(S): Wafer Fab

FOR ANY QUESTIONS CONCERNING THIS NOTIFICATION:

Contact your local ON Semiconductor Sales Office or Richard Tan<Richard.tan@onsemi.com>

SAMPLES: Contact your local ON Semiconductor Sales Office or John Wollen<John.Wollen@onsemi.com>

ADDITIONAL RELIABILITY DATA: Available

Contact your local ON Semiconductor Sales Office or Richard Tan<Richard.tan@onsemi.com>

NOTIFICATION TYPE:

Final Product/Process Change Notification (FPCN)

Final change notification sent to customers. FPCNs are issued at least 90 days prior to implementation of the change.

ON Semiconductor will consider this change approved unless specific conditions of acceptance are provided in writing within 30 days of receipt of this notice. To do so, contact <quality@onsemi.com>.

DESCRIPTION AND PURPOSE:

Qualification of ON Semiconductor wafer fab (USGR1) at Gresham, Oregon to source Kionix C4 devices.



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RELIABILITY DATA SUMMARY:

Reliability Test Results:

ON Semiconductor®  **Intrinsic Reliability Qualification Plan**
 (Qualification per 12MON20866, 4150066, JEDEC JP001.01)

Process & Waferfab : C4, USGR1
 Process Status, notes: Transfer from Fab 10

Date : 10, Feb, 2010
 Prepared by : Eddie Glines
 Approved by : Bruce Greenwood, Matt Dickey

ACCELERATED COMPONENT STRESS TESTS

Test	Reference	Test Conditions	Applicable Device or structure	Sample Size per lot	Accept Criteria	# of Lots	Results
Electromigration or ISEM	JESD61, JESD87, JESD33A, JESD37, JESD63, ASTM: F1260-96, EIAJ-986	Isothermal EM test Test to calculate Ea. Assume N=2.0.	All unique structures among: Contacts, Metals, Vias, Stacked Vias.	min 12 samples per test	<0.01% fails in 10 years at use conditions	3	Passed
Stress Migration	JEP139, JESD87	High temperature storage: 150C, 175C, 200C, 225C, 250C; 1000hrs	SM structures	At least 40 samples per wafer, 1 wf per condition	dR/R<20%, <0.1% defective	3	Passed
DC Hot Carrier Injection	JESD28, JESD60, EIAJ-987	1.1*Vd accelerated stress test at Isubmax or Vgmax	nom gate N & P, long gate N; thin & thick	3 samples per condition, min 4 xtors per voltage	nom gate: <10% shift >0.2yr DC, 7yr AC 100ppm lifetime	3	Passed
Voltage Ramp Dielectric Breakdown (VRDB / charge to Breakdown (QBD))	JESD35	Vramp to at least 8MV/cm, or calculate VBD from breakdown distribution	N & P, thin & thick. Gate caps on Nwell, Pwell, and Bulk. PIP, MIM	Sample size sufficient to resolve D0 criteria	Beta D0 <10 Defect/cm2, P1 D0 < 2 Defect/cm2, P2 D0 < 1 Defect/cm2	3	Passed
Time-Dependent Dielectric Breakdown	EIAJ-988	Vg accelerated stress test; multiple Temps and Voltages. Calculate Ea.	N & P, thin & thick. Gate caps on Nwell, Pwell, and Bulk, PIP, MIM	Min 20 caps per stress condition	0.01% cum fails for 10yrs at 1.1*Vc @ 125C	3	Passed
Negative Bias Temperature Instability (NBTI)		1.1*Vduse 168hrs, 3 Temps, 3 Voltages, DC & multiple frequencies	P, thin and thick (N, thin and thick for PBTI)	min 8 per xtor type	Vth<10% shift	3	Passed

ELECTRICAL CHARACTERISTIC SUMMARY:

N.A. Wafer Sales



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CHANGED PART IDENTIFICATION:

Fab10 device number	Process	Gr Device number
19947-006	C4R	20999-006
20274-006	C4R	20959-006
20686-005	C4T	20971-005

**FINAL PRODUCT/PROCESS CHANGE NOTIFICATION #16446****List of affected Customer Specific Parts:**

PartNumber (MPN)	PTI2 Code
19947-003-XWF	AE
19947-004-XWF	AE
19947-006-XWF	AE
19947-007-XWF	AE
20274-004-XWF	AE
20274-005-XWF	AE
20274-006-XWF	AE
20686-001-XWF	AE
20686-002-XWF	AE
20686-005-XWF	AE