Product Bulletin

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Title of Change:	NCV78343 datasheet update
Effective date:	06 Jun 2023
Contact information:	Contact your local onsemi Sales Office or Dalibor.Bartos@onsemi.com
Type of notification:	This Product Bulletin is for notification purposes only. onsemi will proceed with implementation of this change upon publication of this Product Bulletin.
Change Category:	Datasheet update
Change Sub-Category(s):	Datasheet/Product Doc change

Sites Affected:

onsemi Sites	**External Foundry/Subcon Sites**
None	None

Description and Purpose:

Datasheet update from NCV78343/D Rev. 2 to NCV78343/D Rev. 3

Correction of datasheet

- Typographical error corrections
- Additional information about device behaviour
- Correction of descriptions

The change will not impact form, fit, or function of product(s).

List of changes:

Page 12 – New paragraph describing VLED Supply

Old

VLED not described.

VDD Supply

The VDD supply is the low voltage digital and analog supply for the chip, which is powered from VBB. VDD is supplying the internal analog and digital circuits as well as external components like I2C EEPROM and resistor divider on ADC inputs. The POR−circuit is monitoring both the VBB and VDD voltages.

INTERNAL CLOCK GENERATION

The clocks are fully internally generated without the need for any trimming by the user. The accuracy is guaranteed under all operating conditions and independent of external component selection.

New

VLED Supply

When the device is running but the LED current source is disconnected, the LEDs can light up because of the bias currents flowing through pins of the switches. Up to 180 µA (typical) from switch current source may cause the bottom-most LED to shine. If needed, resistors can be connected in parallel to the switches to avoid undesired LED lighting (typically 10 kΩ).

Page 13 – Behavior corrected

Old

consecutive activation of those switches (which need to be changed to 100% duty cycle). When overlapping multiple switch ON events are invoked this despite, the <DIMERR> error is raised and processing of invalid pattern is stopped. When overlapping switch OFF events occur, the

New

When overlapping multiple switch ON events are invoked despite this, the <DIMERR>error is raised.

Page 16 – Figure link corrected

Old

PXN Frame

A message is transferred over PXN bus in a form of PXN frame, which is depicted in Figure 16. PXN frame. The PXN protocol for communication over PXN is based on UART communication standard, i.e. one start bit, 8 data bits (LSB first), one stop bit, no parity bit.

New

..., which is depicted in Figure 16. The PXN protocol for communication ...

Page 16 – Additional information about minimal delay between commands

Old

The header consists of a BREAK field (logic 0 for a certain time), a SYNC field (0x55 byte) and two protected identifiers PID1 and PID2. The response consists of an arbitrary number of DATA bytes within a range from 1 to 12 followed by CRC. The particular bytes are separated by inter−byte space. The minimum length for the BREAK field is 13 Tbits (52 μs for the default communication speed 250 kbps). The BREAK field stop bit (BREAK field

New

... separated by inter-byte space. Minimal delay of 1 Tbit is required before starting new PXN frame. The minimum length for ...

Page 17 – Additional information about minimal delay between commands

Old

delimiter) is minimum 1 Tbit and maximum according to the selected watchdog time. If the device is not responding through the repeater−slave, the extended break can be required (26 Tbits). In case of only M−LVDS slave cluster, the DE pin on the M−LVDS transceiver must be set LOW within 1 Tbit after the Header part.

New

If the device is not responding through the repeater−slave, the extended break (26 Tbits) can be required to recover communication to slave devices. Such case can occur when Read frame is addressed non assigned address. In case of only M−LVDS slave cluster, the DE pin on the M−LVDS transceiver (e.g., NBA3N206S) must be set LOW within 1 Tbit after the Header part to allow device response.

Page 17 – Figure changed to improve clarity

Old

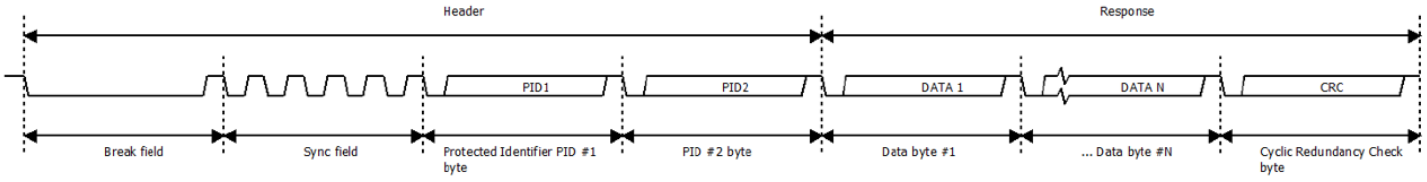
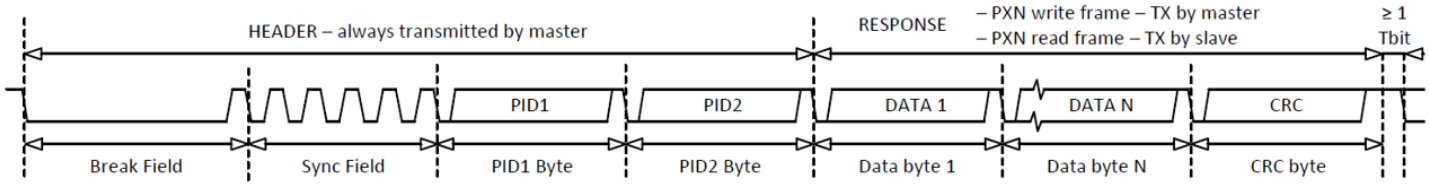


Figure 16. PXN Frame

New



Page 17 – Additional information

Old

The NCV78343 supports only the TYPE1 register bank organization, since each register bank consists of 3 bytes. This means, it is possible to read/write up to 4 registers in one frame.

New

The NCV78343 supports only the TYPE1 register bank organization, since each register bank consists of 3 bytes. This means that it is possible to read/write up to 4 registers in one frame, which can be for example used to write ON/OFF times for all 12 switches in only 3 PXN frames.

Page 18 – Additional information

Old

Addressing Options

It is possible to set a device address in 3 different ways:
– Multi−level address pin
– Auto−addressing procedure
– OTP node address bits

New

Addressing Options

It is possible to set a device address in 3 different ways:

– Multi−level address pin

– Auto−addressing procedure

– OTP node address bits

Addressing using OTP memory is recommended for final application. Some of the other device parameters are saved in memory as well, which speeds up device setup after each power-on.

Page 19 – Additional information

Old

OTP Node Address

The OTP node address can be zapped by customer at EoL (End of Line) after the PXN node address was determined either by means of multi−level address pin measurement or by means of auto−addressing procedure. The value of OTP node address and OTP bank lock bit is obtained each time the PXN node is powered up and the custom OTP bank is read out.

New

OTP Node Address

The OTP node address can be zapped by customer at EoL (End of Line) after the PXN node address was determined either by means of multi−level address pin measurement or by means of auto−addressing procedure. The value of OTP node address and OTP bank lock bit is obtained each time the PXN node is powered up and the custom OTP bank is read out. Loading of other device settings from OTP memory speeds up device setup after power-on. OTP memory zapping is necessary to fulfil ASIL B safety requirements.

Page 19 – Device behavior correction

Old

<FAIL_SAFE_STATE_LED_STRINGx> − state of the LED string x, x={1,2,3,4}, in case one of the following conditions is detected:

- NORMAL mode is entered or
- Timeout error occurred or
- DIMERR recovered or

The bits set directly the switch state. The fail safe state is taken into account only when

New

<FAIL_SAFE_STATE_LED_STRINGx> – state of the LED string x, x={1,2,3,4}, in case one of the following conditions is detected:

- NORMAL mode is entered or
- Timeout error occurred

The bits set directly the switch state. …

Page 20 – New paragraph with additional information

Old

process cannot be undone. The OTP zapping is possible only in the OTP config mode. To ensure correct OTP zapping, the VBB voltage must be in range of 16 to 30 V with the current capability at least 85 mA during the OTP zapping process. The OTP memory zapping should be done at the EoL to fulfil the ASIL B requirements.

New

…fulfil the ASIL B requirements.

External MCU can read content of OTP memory. To do this, device must first receive CF10 PXN configuration frame followed by CF11 PXN configuration frame. This process is similar to reading from external I2C EEPROM.

Page 20 – Clarification of operating modes

Old

Operating Modes

The PXN node can operate in following modes:

– OTP Config mode
– Auto–addressing mode
– Normal Direct mode
– Normal PWM mode
– NO_CRC Direct mode
– NO_CRC PWM mode
– Fail–safe OTP mode
– Fail–safe OPEN mode

New

– OTP Config mode
– Auto–addressing mode
– Normal Direct mode
– Normal PWM mode
– Normal Fail–safe OTP mode
– Normal Fail–safe OPEN mode
– NO_CRC Direct mode
– NO_CRC PWM mode
– Fail–safe OTP mode
– Fail–safe OPEN mode

Page 20 – Additional information about OTP Config mode

Old

OTP Config mode – the chip enters this mode under the following circumstances: when the OTPs are not zapped and the voltage divider at ADR pin is in a valid range or the OTPs are zapped but the OTP CRC BANK2 is wrong or after successful auto–addressing process. Please see the following flow diagram 'Flow chart after POR' in the Application notes.

New

OTP Config mode – the chip enters this mode under the following circumstances: when the OTPs are not zapped and the voltage divider at ADR pin is in a valid range, or the OTPs are zapped but the OTP CRC BANK2 is wrong, or after successful auto–addressing process. Please see the following flow diagram 'Flow chart after POR' in the Application notes.

Chip with non-zapped OTP memory starts with both UART and M-LVDS interfaces enabled. To determine which one will be used, there is a 60 ms timer (typical) that starts once device enters OTP Config mode. After timer elapses, chip reads state of UART RX pin to determine if UART bus should remain enabled (RX pulled high) or disabled (RX pulled low). During this period, M-LVDS devices might be unable to communicate if their UART RX pin is pulled low. Timer can be stopped before elapsing by leaving OTP Config mode, typically by receiving CF13.

Page 20 – Additional information about NO_CRC and Normal modes

Old

NO_CRC Direct/PWM mode – the device enters the NO_CRC mode after receiving CF13 (see Table 62) in the OTP Config mode. The meaning of Direct and PWM is same as in the previous mode. The device should not operate in the NO_CRC mode.

New

NO_CRC Direct/PWM mode – the device enters the NO_CRC mode after receiving CF13 (see Table 62) in the OTP Config mode. The functionality of NO_CRC Direct and PWM modes is same as Normal Direct and Normal PWM modes. NO_CRC prefix means that the device detected invalid CRC in OTP memory bank 2 during power on, most likely because OTP memory is not written.

Please note that only device with written OTP memory achieves ASIL B safety rating.

Page 20 – Corrected device behavior in Fail-safe OTP mode

Old

Fail−safe OTP mode – this is the fail−safe state when the OTP fail−safe data are loaded and applied on switches. The chip enters this mode under the following circumstances: watchdog timeout or DIMERR. To leave this mode, please read out register 0x10.

New

Fail−safe OTP mode – when this fail−safe state is entered after watchdog timeout, OTP fail−safe data are loaded and applied on switches. Chip also enters this mode after DIMERR. To leave this mode, clear TIMEOUT or DIMERR flags set in register 0x10.

Page 20 – Additional information about M-LVDS transceiver

Old

<M−LVDS_OFF> − M−LVDS interface disable. The <M−LVDS_OFF> selection is taken into account only when the <PXN_LOCK_BIT> is set and the CRC is correct.

New

<M−LVDS_OFF> − M−LVDS interface disable. The <M−LVDS_OFF> selection is taken into account only when the <PXN_LOCK_BIT> is set and the CRC is correct. Unused M-LVDS transceiver can be disabled to reduce current consumption by 12.5 mA (typical).

Page 23 – Register 0x00 description clarified

Old

SW[11:0] – Direct control of the switches ON/OFF or OPEN clear request:
SERVICE = “00”: direct control of the switches ON/OFF; valid SW[11:0], others are “0”.
SERVICE = “01”: OPEN clear request; valid SW_SEL[3:0] from “0001” to “1100”, others are “0”.

New

SERVICE = “01”: OPEN clear request; Switch is chosen by valid SW_SEL[3:0] from “0001” to “1100” (Switch 1 to 12), others are “0”.

Page 28 – Additional information about SW SLOT

Old

SW SLOT – recommended distance between two switch ON events.

New

SW SLOT – recommended distance (in ticks of dimming clock) between two switch ON events

Page 28 – T1_CONF bit behavior corrected

Old

T1_CONF – The bit defines the switch ON time (switching slope), where the "0" means steeper slope. For better EMC results it is recommended to set this value to "1".

New

T1_CONF – The bit defines the switch ON time (switching slope), where the "1" means steeper slope. For better EMC results it is recommended to set this value to "0".

Page 29 – DIMWARN flag behavior corrected

Old

DIMWARN – Dimming warning indicator. The bit is set high in case of an overlapping switch OFF sequences are detected. When the flag is set, the device enters FAIL status mode and LED's are switched ON/OFF following the OTP memory bits 8–11 in Table 24. OTP Bank. The bit is cleared upon a successful readout over PXN (clear by read bit).

New

DIMWARN – Dimming warning indicator. The bit is set high in case of an overlapping switch OFF sequences are detected. The bit is cleared upon a successful readout over PXN (clear by read bit).

Page 29 – DIMERR flag behavior corrected

Old

DIMERR - Dimming error indicator. The bit is set high in case an overlapping switch ON sequences are detected. When the flag is set, the device enters the FAIL status mode and LED's are switched OFF. The bit is cleared upon a successful readout over PXN (clear by read bit). When the flag is cleared, the device enters NORMAL_DIRECT mode and LED String OTP data are loaded.

New

DIMERR - Dimming error indicator. The bit is set high in case an overlapping switch ON sequences are detected. When the flag is set, the device enters the FAIL status mode. The bit is cleared upon a successful readout over PXN (clear by read bit).

Page 30 – Typographical error correction

Old

TIMEOUT – The PXN timeout error is detected in case neither MAPENA nor MAENA_DIR is activated within a TIMEOUT period.

New

TIMEOUT – The PXN timeout error is detected in case neither MAPENA nor MAPENA_DIR is activated within a TIMEOUT period.

Page 41 – Additional information about TSD_CODE

Old

The <TSD_CODE> is trimmed in production to 170 °C. Whenever a measurement result is available, it is immediately checked against both TSD and TW thresholds.

New

The <TSD_CODE> is trimmed in production to 170 °C (TSDTEMPERATURE). Typical value of <TSD_CODE> is 186 and exact trimmed value can be read from Register 0x12.

Page 41 – Overlapping ON events behavior correction

Old

When overlapping switch ON events are despite this invoked, the NCV78343 incorporates protective feature, in which the <DIMERR> error is raised causing that all switches are switched OFF and processing of invalid pattern is stopped.

New

When overlapping switch ON events are despite this invoked, the NCV78343 incorporates protective feature, in which the <DIMERR> error is raised.

Page 41 – Remove reference to non existing chapter

Old

With the help of these two comparators a several fail situations can be detected and distinguished on each switch individually, for more detail description see chapter PIXEL SWITCHES.

New

With the help of these two comparators a several fail situations can be detected and distinguished on each switch individually.

Page 41 – Additional information about OPEN clear request

Old

Dedicated OPEN clear request

When the OPEN state or overvoltage is detected, the switch is automatically closed and the status is shown in the SWx.STATUS register 0x0F. The switch is released upon a successful OPEN clear request frame.

In direct mode, the switches are updated upon a successful write to register 0x00 with service "00".

In PWM mode, the switches are updated according to the ON/OFF values.

New

Dedicated OPEN clear request

When the OPEN state or overvoltage is detected, the switch is automatically closed and the status is shown in the SWx.STATUS register 0x0F. Further attempts to control this switch using PWM or DIRECT mode don't have any effect. The switch is released upon a successful OPEN clear request frame.

In direct mode, the released switch is updated upon a successful write to register 0x00 with service "00". In PWM mode, the released switch is updated according to the ON/OFF values.

Page 53 – Correction of described behavior in FAIL-SAFE mode

Old

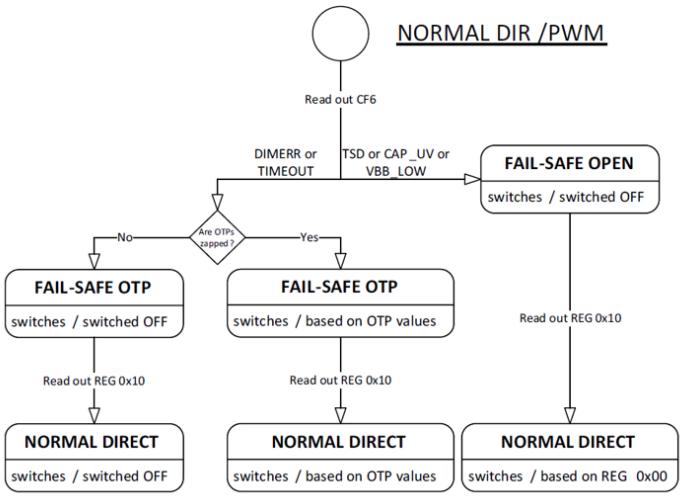
The device enters FAIL−SAFE OTP mode when DIMERR or TIMEOUT appears. In this mode, the switches are set according to the OTP memory values. If the OTP memory is not zapped, the switches are switched OFF. Once the error status bit is cleared, the switches remain unchanged.

New

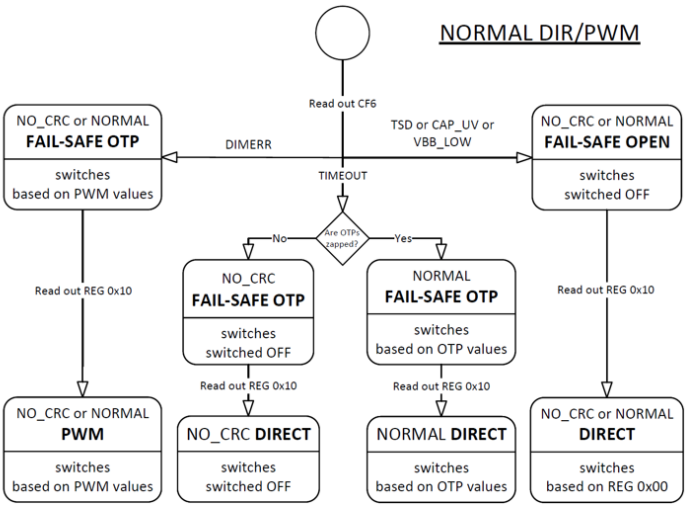
The device enters FAIL−SAFE OTP mode when DIMERR or TIMEOUT appears. When TIMEOUT is set and this mode is entered, switches are set according to the OTP memory values. If the OTP memory is not zapped, the switches are switched OFF. Once the error status bit is cleared, the switches remain unchanged. When DIMERR is set and this mode is entered, switches operation is unaffected.

Page 53 – Figure updated with additional information

Old

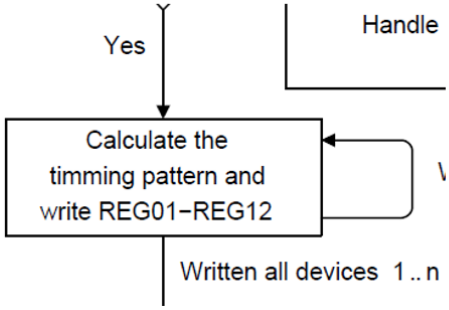


New



Page 55 – Typographical error correction

Old



New

Calculate the dimming pattern and write REG01 – REG12

List of Affected Standard Parts:

***Note**: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal**.*

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