

DESIGN/PROCESS CHANGE NOTIFICATION

This is to inform you that a change is being made to the products listed below.

Unless otherwise indicated in the details of this notification, the identified change will have no impact on product quality, reliability, electrical, visual or mechanical performance and affected products will remain fully compliant to all published specifications. Products incorporating this change may be shipped interchangeably with existing unchanged products.

This change is planned to take effect in 90 calendar days from the date of this notification. Please work with your local Fairchild Sales Representative to manage your inventory of unchanged product if your evaluation of this change will require more than 90 calendar days.

Please contact your local Customer Quality Engineer within 30 days of receipt of this notification if you require any additional data or samples. Alternatively, you may send an email request for data, samples or other information to PCNSupport@fairchildsemi.com.

Implementation of change:

Expected First Shipment Date for Changed Product : Feb. 18, 2013

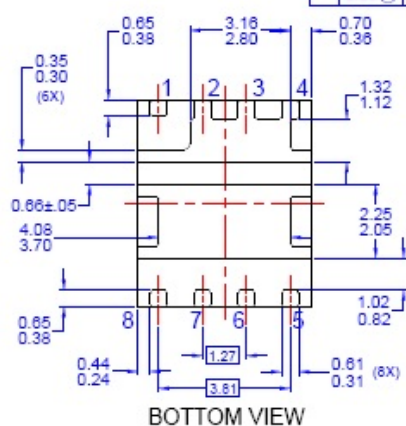
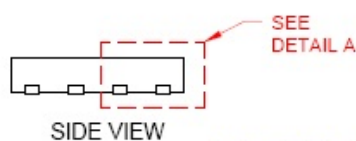
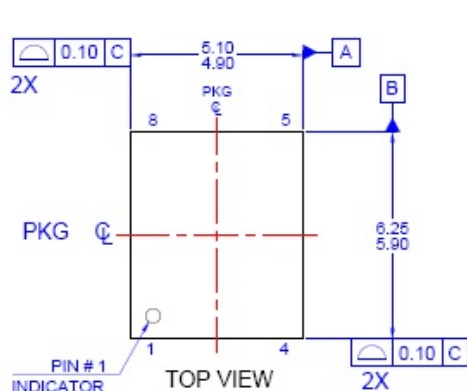
Expected First Date Code of Changed Product :1306

Description of Change (From) :

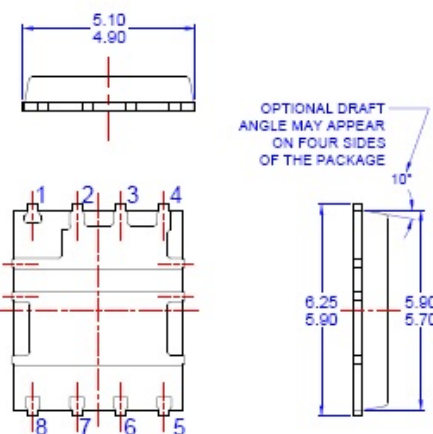
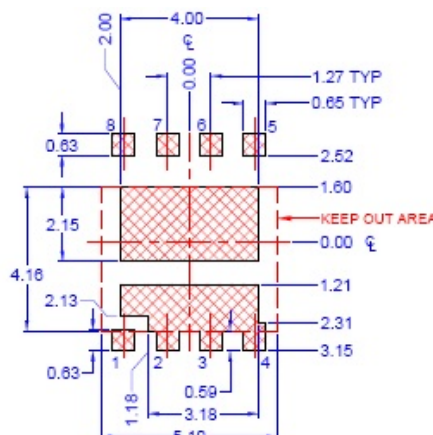
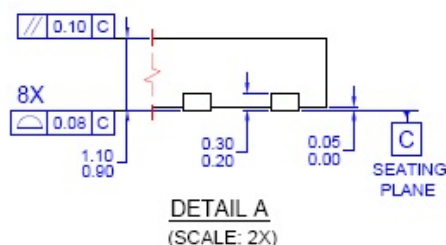
Selected MOSFET products assembled in our Power 56 dual asymmetric clip package. Current singulation method is saw-singulation, lead frame is etched with a pre-molded clip bonding method. For the package dimensional out line please refer to the drawing below.

Description of Change (To) :

An alternate singulation method will be a punch-singulation with a stamped lead frame and flat metal clip bonding method for the source. Low Side FET (Q2) gate will be wire Bonded vs Clip bonded. Refer to the dimensional outline drawing below.



OPTION - A (SAWN TYPE)



OPTION - B (PUNCHED TYPE)

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE:
JEDEC REGISTRATION, MO-240, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
 - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN
THE KEEP OUT AREA.
 - F) DRAWING FILE NAME: PQN08EREV4.

Reason for Change:

In addition to the current qualified Saw-singulated Power 56 package, Fairchild Semiconductor has qualified the Punch-singulated Power 56 to support volume ramp. There will be no change to the part numbers as the Punch and Saw-singulated Power 56 share common land pattern dimensions and are interchangeable. This change will not affect the devices' specifications in the data sheets nor the functional performance. Product quality, reliability and MSL performance will be maintained.

Affected Product(s):

FDMS3600AS	FDMS3602AS	FDMS3604AS
FDMS3604S	FDMS3606S	FDMS3610S
FDMS3622S	FDMS3623S	FDMS3625S
FDMS3626S	FDMS3627S	FDMS3629S
FDMS3660S	FDMS3664S	FDMS3668S
FDMS3686S		

Qualification Plan	Device	Package	Process	No. of Lots
QP12100983E	FDMS3668S	PQFN56DA	Q22CF RY21CD	1

Test Description:	Condition:	Standard :	Duration:	Results:
MSL1 Precondition	260°C, 3 pass	JESD22-A113	NA	0/231
Temperature Cycle	-65°C to 150°C, 15min dwell	JESD22-A104	500 cycles	0/77
Highly Accelerated Stress Test	130°C, 85%RH, Vr = 24V	JESD22-A110	96 hrs	0/154
Power Cycle	T on/off = 2min, Delta Tj = 100°C	JESD22-A105	10000 cycles	0/154
High Temperature Storage Life	175°C	JESD22-A103	500 hrs	0/77
Resistance to Solder Heat	260°C	JESD22-B106	10 sec	0/30

Qualification Plan	Device	Package	Process	No. of Lots
QP12100983E	FDMS3664S	PQFN56DA	Q22CF RW31CD	1

Test Description:	Condition:	Standard :	Duration:	Results:
MSL1 Precondition	260°C, 3 pass	JESD22-A113	NA	0/231
Temperature Cycle	-65°C to 150°C, 15min dwell	JESD22-A104	500 cycles	0/77
Highly Accelerated Stress Test	130°C, 85%RH, Vr = 24V	JESD22-A110	96 hrs	0/154
Power Cycle	T on/off = 2min, Delta Tj = 100°C	JESD22-A105	10000 cycles	0/154
High Temperature Storage Life	175°C	JESD22-A103	500 hrs	0/77
Resistance to Solder Heat	260°C	JESD22-B106	10 sec	0/30

Qualification Plan	Device	Package	Process	No. of Lots
QP12100983E	FDMS3622S	PQFN56DA	RX08OD RS33OD	1

Test Description:	Condition:	Standard :	Duration:	Results:
MSL1 Precondition	260°C, 3 pass	JESD22-A113	NA	0/231
Temperature Cycle	-65°C to 150°C, 15min dwell	JESD22-A104	500 cycles	0/77
Highly Accelerated Stress Test	130°C, 85%RH, Vr = 20V	JESD22-A110	96 hrs	0/154
Power Cycle	T on/off = 2min, Delta Tj = 100°C	JESD22-A105	10000 cycles	0/154
High Temperature Storage Life	175°C	JESD22-A103	500 hrs	0/77
Resistance to Solder Heat	260°C	JESD22-B106	10 sec	0/30