ON Semiconductor®

Product Bulletin

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Title of Change:	Typo corrections in the datasheet for better datasheet integrity
Effective date:	19 Feb 2020
Contact information:	Contact your local ON Semiconductor Sales Office or Ladislav.Bazant@onsemi.com
Type of notification:	This Product Bulletin is for notification purposes only. ON Semiconductor will proceed with implementation of this change upon publication of this Product Bulletin.
Change Category:	Datasheet change
Change Sub-Category(s):	Datasheet/Product Doc change

Sites Affected:

ON Semiconductor Sites	**External Foundry/Subcon Sites**
None	None

Description and Purpose:

- **Marking diagram correction**
  - Adding ON logo, specify Specific Device Code.

MARKING DIAGRAM

Adding ON logo

~~XXXX~~ = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

Specific Device Code = NCV7685 instead of XXXX

- **Block Diagram**
  - SCL arrow change
  - Internal ESD diodes added

SCL read direction

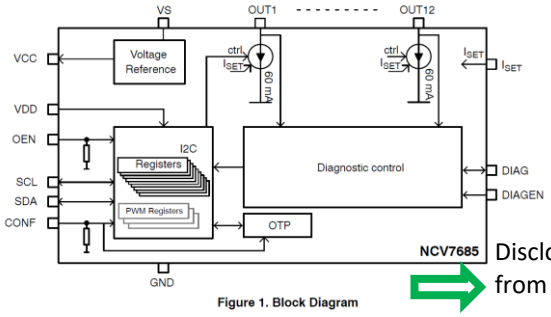


Figure 1. Block Diagram

Disclose the internal ESD diodes from SCL SDA to VDD

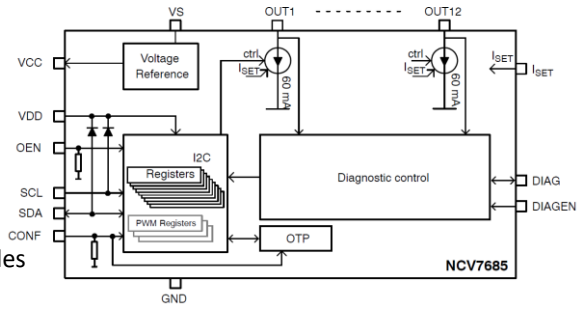
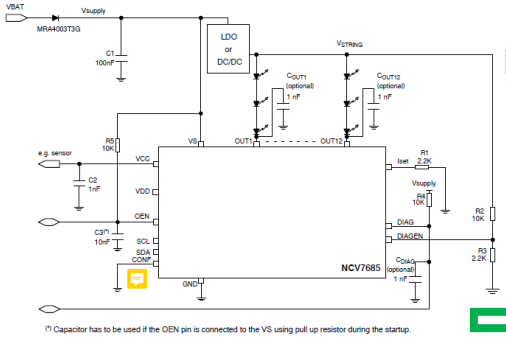


Figure 1. Block Diagram

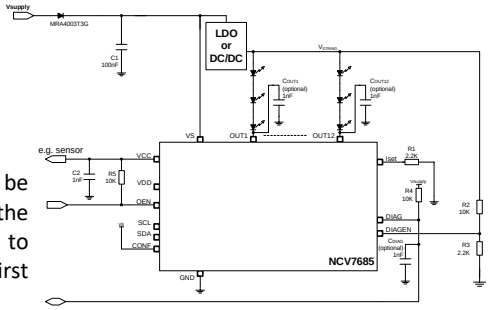
- **Application Diagram**
  - CONF and OEN pin connection



(*) Capacitor has to be used if the OEN pin is connected to the VS using pull up resistor during the startup.

Figure 4. Application Diagram without Micro−controller (Stand Alone Mode)

If the CONF pin is put to High, the LEDs are automatically activated in the standalone mode.



RC filter for OEN pin may not be sufficient. It is better to activate the OEN pin via VCC output reference to have 0 V during the VS startup for first 10µs.

- **ABSOLUTE MAXIMUM RATINGS**
  - Adding Tazap temperature for OTP zapping

TJMAX	Junction Temperature, TJ	-40	150	°C
TAZAP	OTP zap Ambient Temperature	10	30	°C

- **Correction and adding parameters in the Attributtes and Electrical characteristic table**
  - Junction to Ambient, $R_{\theta JA}$. Typo correction from 48 to 45.8 °C/W

board	Tj	Ta	T top	T solder	delta T	P	Theta-JA	Psi-JT	Psi-JB
1SOP - 71um	137.76	85	129.47	131.32	52.8	0.72	73.3	11.5	8.9
1SOP - 35um	154.63	85	144.77	148.27	69.6	0.72	96.7	13.7	8.8
2S0P - 35um	145.30	85	135.96	139.04	60.3	0.72	83.8	13.0	8.7
2S2P - 35um	123.40	85	115.27	117.23	38.4	0.72	53.3	11.3	8.6
2S2P - 35 + 71um	120.36	85	112.35	114.17	35.4	0.72	49.1	11.1	8.6
2S2P - 71 + 35um	117.97	85	110.73	111.61	33.0	0.72	45.8	10.1	8.8

Table 3. ATTRIBUTES

Parameter	Value	Unit
ESD Capability (Note 2) ESD Voltage, HBM (Human Body Model); (100 pF, 1500 Ω) – All pins – Output pins OUTx to GND ESD according to CDM (Charge Device Model) – All pins – Corner pins ESD according to MM (Machine Mode) – All pins	 ±2 ±4 ±500 ±750 ±150	 kV kV V V V
Moisture sensitivity (SSOP24–EP) (Note 3)	MSL2	
Storage Temperature	−55 to 150	°C
Package Thermal Resistance (SSOP24–EP) (Note 4) – Junction to Ambient, $R_{\theta JA}$ – Junction to Board, $R_{\theta JB}$ – Junction to Case (Top), $R_{\theta JC}$	 48 8.8 10.1	 °C/W °C/W °C/W

  - Adding VS supply voltage and current during OTP zapping parameter

GENERAL						
Supply Voltage	VS_EXT	Functional extended range (limited temperature)	5	-	28	V
	VS_OP	Parametric operation	5	-	18	V
	VS_OTPzap	Supply range during OTP zapping; 2.5 V ≤ ISET ≤ 3.3V; VS current peak capability ≥ 70 mA	13	-	18	V
Supply Under-Voltage	VSUV	VS rising	3.8	4.1	4.4	V

  - Digital supply current typical value correction

Digital supply current	IDD	I²C mode, VS = 12 V	–	1.5	2	mA

⇩

Digital supply current	IDD	I²C mode, VS = 12 V	–	**0.24**	2	mA

- **General description - better clarification**
  - Unused VCC output, remark for no need of the VCC capacitor

Power Supply and Voltage Reference (VS, V_{CC}, V_{DD})

VS is the analog power supply input of the device. VS supply is monitored with respect to the crossing of VSUV level (typ. 4.1 V). When VS rises above VSUV, the device starts the power−up state. When VS is above the VS_OP minimum level (typ. 5 V), the device can work properly.

VCC is a voltage reference providing 3.3 V derived from the VS main supply. It is able to deliver up to 1 mA and is primarily intended to supply 3.3 V loads.

VDD is the digital power supply input of the device.

⇨

Insert:
If VCC output reference is not used, then the VCC capacitor can be omitted.

Adding Power-on Sequence figure

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VDD is the digital power supply input of the device.

Ground Connections (GND: Pin 13 and Pin 19)

The device ground connection is split to two pins called GND. Both pins have to be connected on the application PCB.

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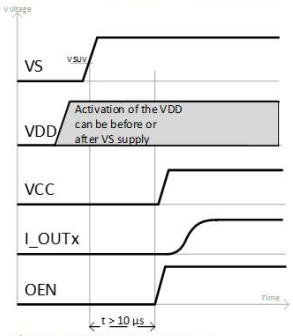

Figure 6. Power-up sequence

Ground Connections (GND: Pin 13 and Pin 19)

The device ground connection is split to two pins called GND. Both pins have to be connected on the application PCB.

- Clarification of the OEN input voltage during the startup

Output Enable (OEN)

When the OEN input voltage is high, all output channels are programmed according to the I2C or SAM configuration. When OEN voltage is below 0.7 V, all outputs are disabled in the SAM or I2C mode regardless on the registers setting. If the OEN pin is left floating, the internal pull down resistor will cause switching off all channels. The OEN pin has to be ~~low~~ during the startup.

Replace to:
The OEN pin has to be 0V during the startup for at least 10 µs

- Adding following clarification about the time delay which is needed for the OTP zapping

Required Time Delay for OTP Zapping

As soon as the ID_LOCK_OTP message is received, the I^2C acknowledge is immediately send out to the MCU. However, the internal circuitries still requires 500 µs time delay to complete the OTP zapping of one OTP bit. Therefore, no I^2C confirmation is send. The number of OTP bits that are zapped corresponds with each change from the default values. It is needed 16.5 ms in total to successfully finish the zapping sequence of all 32 customer bits + one internal bit. The verification of the OTP banks can be done by power reset of both supplies (VS and VDD together) after zapping delay followed by readout of the ID_READ_OTP I^2C message.

- **Typo in the Format of the I2C Write Access Frames**
  - The acknowledge is missing at the end of the write frame.

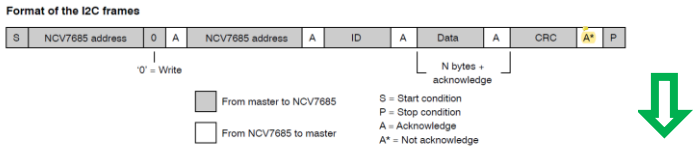

Figure 6. Format of I2C Write Access Frames

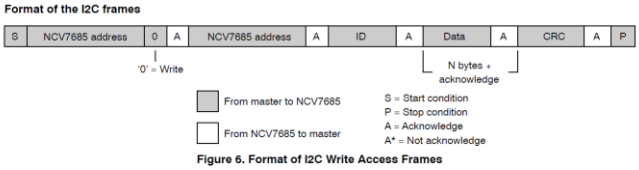

Figure 6. Format of I2C Write Access Frames

- **Adding CRC clarification**
  - For better description of the CRC check sum the following paragraph is added into text:

CRC ERROR DETECTION ALGORITHM

The CRC protection is turned off by default. It can be enabled by activation of the OTP ERREN bit (ERREN = 1). The every I^2C byte including both addresses with R/W flag are calculated using CRC8 algorithms. The CRC polynomial is following: $x^8 + x^5 + x^3 + x^2 + x + 1$.

Example of the CRC used in the I^2C message with I2C_CONF byte = 0xCFFF and with I^2C address 0x60 (0xC0) is 0x2E.

- **Graphical restyling**
  - Underscore is missing in the I2C STATUS register name.

Table 13. I2C STATUS

Bit	D7	D6	D5	D4
Access type	R	R	R	R
Bit name	SC_Iset	I2Cerr	UV	diagRange
Reset value	0	0	0	0

Table 13. I2C_STATUS

Bit	D7	D6	D5	D4
Access type	R	R	R	R
Bit name	SC_Iset	I2Cerr	UV	diagRange
Reset value	0	0	0	0

The change will not impact form, fit, or function of product.

List of Affected Standard Parts:

***Note**: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal**.*

NCV7685DQR2G		