



Title of Change:	AR0237 Register Reference Changes	
Effective date:	24 Feb 2020	
Contact information:	Contact your local ON Semiconductor Sales Office or Sonya.Yip@onsemi.com	
Type of notification:	This Product Bulletin is for notification purposes only. ON Semiconductor will proceed with implementation of this change upon publication of this Product Bulletin.	
Change Category:	Documentation Change	
Change Sub-Category(s):	Datasheet/Product Doc change	
Sites Affected:		
ON Semiconductor Sites		External Foundry/Subcon Sites
None		None
Description and Purpose:		
The AR0237CS Register Reference has been updated with new information. These changes do not affect form, fit, or function of the product.		
AR0237CS Register Reference Changes		
1. Updated Introduction section with information about register attributes being added		
Old Introduction Section:		
<div><div><div>Bad Frames</div><p>A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame. Many changes to the sensor register settings can cause a bad frame. For example, when <code>line_length_pck</code> (R0x0342–3) is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.</p><div>Register Map</div><p>The tables in this section show which locations are used within the 16–bit address space. Locations that are not shown in the table are reserved for future use; to maintain compatibility with future designs they should not be read from or written to. Locations that are shown as “Reserved” should not be accessed. The default read values of registers are subject to change.</p></div><div><p>By default, bad frames are not masked. In the register tables, the “Bad Frame” column shows where changing a register or register field will cause a bad frame. This notation is used:</p><ul style="list-style-type: none">• <i>N</i>—No. Changing the register value will not produce a bad frame.• <i>Y</i>—Yes. Changing the register value might produce a bad frame.• <i>YM</i>—Yes; but the bad frame will be masked out when <code>mask_corrupted_frames</code> (R0x0105) is set to “1.”<div>CAUTION: The effect of writing to reserved registers is undefined and may include the possibility of causing permanent electrical damage to the sensor.</div><p>Table 1 below lists registers and their default values. Register addresses are shown as 16– bit values in both decimal and hexadecimal. Table 2 lists registers and their descriptions.</p></div></div>		



New Introduction Section:

Buffering

In register tables, buffering shows the timing with which a newly-written register value takes effect. The notation used is:

Blank – Unbuffered. By default register update takes effect immediately.

S – Single frame sync'd. Register update in frame N takes effect in frame N+1.

D – Double frame sync'd. Register update in frame N takes effect in frame N+2.

Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame.

Many changes to the sensor register settings can cause a bad frame. For example, when `line_length_pck` is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

By default, bad frames are not masked. If the masked bad frame option is enabled, both LV and FV are inhibited for these frames so that the vertical blanking time between frames is extended by the frame time.

In the register tables, the "Bad Frame" column shows where changing a register or register field will cause a bad frame. This notation is used:

Blank – No. Changing the register value will not produce a bad frame.

Y – Yes. Changing the register value might produce a bad frame.

YM – Yes. But the bad frame will be masked out when `mask_corrupted_frames` (`R0x301A[9]`) is set to "1".

Embedded

In register tables, the embedded column notes whether or not the register is present in the per_frame embedded data.

The notation used is:

Blank – By default, a register is not present in the embedded data

E – The register is present in the embedded data.

Locked

In register tables, locked notes whether writes to the register are protected by `R0x3010`. The notation used is

Blank – By default, writes to a register are not protected by `R0x3010`

L – Writes to the register are protected by `R0x3010`

2. Replaced Frame Syn'd and Bad Frame columns with new attribute columns for all registers in the Register Reference

Old Register Description Column Example:

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12288 R0x3000	15:0	0x0356	CHIP_VERSION_REG (R/W)	N	N
			Model ID. Read-only. Can be made read/write by clearing <code>R0x301A-B[3]</code> .		
R12290 R0x3002	15:0	0x0004	Y_ADDR_START (R/W)	Y	YM
			The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value.		

New Register Description Column Example:

Attributes Columns; Usage and Values, left to right

Column 1: Buffering <blank> = Unbuffered S = Single Frame Synced D = Double Frame Synced	Column 2: Bad Frame <blank> = No bad frame Y = Causes a bad frame YM = Maskable bad frame	Column 3: Embedded <blank> = Not embedded E = embedded	Column 4: Locked <blank> = Not locked L = locked
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Y: 0x0000 to 0x0003, 0x0004 to 0x0007, 0x0008 to 0x000B, 0x000C to 0x000F, 0x0010 to 0x0013, 0x0014 to 0x0017, 0x0018 to 0x001B, 0x001C to 0x001F, 0x0020 to 0x0023, 0x0024 to 0x0027, 0x0028 to 0x002B, 0x002C to 0x002F, 0x0030 to 0x0033, 0x0034 to 0x0037, 0x0038 to 0x003B, 0x003C to 0x003F, 0x0040 to 0x0043, 0x0044 to 0x0047, 0x0048 to 0x004B, 0x004C to 0x004F, 0x0050 to 0x0053, 0x0054 to 0x0057, 0x0058 to 0x005B, 0x005C to 0x005F, 0x0060 to 0x0063, 0x0064 to 0x0067, 0x0068 to 0x006B, 0x006C to 0x006F, 0x0070 to 0x0073, 0x0074 to 0x0077, 0x0078 to 0x007B, 0x007C to 0x007F, 0x0080 to 0x0083, 0x0084 to 0x0087, 0x0088 to 0x008B, 0x008C to 0x008F, 0x0090 to 0x0093, 0x0094 to 0x0097, 0x0098 to 0x009B, 0x009C to 0x009F, 0x00A0 to 0x00A3, 0x00A4 to 0x00A7, 0x00A8 to 0x00AB, 0x00AC to 0x00AF, 0x00B0 to 0x00B3, 0x00B4 to 0x00B7, 0x00B8 to 0x00BB, 0x00BC to 0x00BF, 0x00C0 to 0x00C3, 0x00C4 to 0x00C7, 0x00C8 to 0x00CB, 0x00CC to 0x00CF, 0x00D0 to 0x00D3, 0x00D4 to 0x00D7, 0x00D8 to 0x00DB, 0x00DC to 0x00DF, 0x00E0 to 0x00E3, 0x00E4 to 0x00E7, 0x00E8 to 0x00EB, 0x00EC to 0x00EF, 0x00F0 to 0x00F3, 0x00F4 to 0x00F7, 0x00F8 to 0x00FB, 0x00FC to 0x00FF, 0x0100 to 0x0103, 0x0104 to 0x0107, 0x0108 to 0x010B, 0x010C to 0x010F, 0x0110 to 0x0113, 0x0114 to 0x0117, 0x0118 to 0x011B, 0x011C to 0x011F, 0x0120 to 0x0123, 0x0124 to 0x0127, 0x0128 to 0x012B, 0x012C to 0x012F, 0x0130 to 0x0133, 0x0134 to 0x0137, 0x0138 to 0x013B, 0x013C to 0x013F, 0x0140 to 0x0143, 0x0144 to 0x0147, 0x0148 to 0x014B, 0x014C to 0x014F, 0x0150 to 0x0153, 0x0154 to 0x0157, 0x0158 to 0x015B, 0x015C to 0x015F, 0x0160 to 0x0163, 0x0164 to 0x0167, 0x0168 to 0x016B, 0x016C to 0x016F, 0x0170 to 0x0173, 0x0174 to 0x0177, 0x0178 to 0x017B, 0x017C to 0x017F, 0x0180 to 0x0183, 0x0184 to 0x0187, 0x0188 to 0x018B, 0x018C to 0x018F, 0x0190 to 0x0193, 0x0194 to 0x0197, 0x0198 to 0x019B, 0x019C to 0x019F, 0x01A0 to 0x01A3, 0x01A4 to 0x01A7, 0x01A8 to 0x01AB, 0x01AC to 0x01AF, 0x01B0 to 0x01B3, 0x01B4 to 0x01B7, 0x01B8 to 0x01BB, 0x01BC to 0x01BF, 0x01C0 to 0x01C3, 0x01C4 to 0x01C7, 0x01C8 to 0x01CB, 0x01CC to 0x01CF, 0x01D0 to 0x01D3, 0x01D4 to 0x01D7, 0x01D8 to 0x01DB, 0x01DC to 0x01DF, 0x01E0 to 0x01E3, 0x01E4 to 0x01E7, 0x01E8 to 0x01EB, 0x01EC to 0x01EF, 0x01F0 to 0x01F3, 0x01F4 to 0x01F7, 0x01F8 to 0x01FB, 0x01FC to 0x01FF, 0x0200 to 0x0203, 0x0204 to 0x0207, 0x0208 to 0x020B, 0x020C to 0x020F, 0x0210 to 0x0213, 0x0214 to 0x0217, 0x0218 to 0x021B, 0x021C to 0x021F, 0x0220 to 0x0223, 0x0224 to 0x0227, 0x0228 to 0x022B, 0x022C to 0x022F, 0x0230 to 0x0233, 0x0234 to 0x0237, 0x0238 to 0x023B, 0x023C to 0x023F, 0x0240 to 0x0243, 0x0244 to 0x0247, 0x0248 to 0x024B, 0x024C to 0x024F, 0x0250 to 0x0253, 0x0254 to 0x0257, 0x0258 to 0x025B, 0x025C to 0x025F, 0x0260 to 0x0263, 0x0264 to 0x0267, 0x0268 to 0x026B, 0x026C to 0x026F, 0x0270 to 0x0273, 0x0274 to 0x0277, 0x0278 to 0x027B, 0x027C to 0x027F, 0x0280 to 0x0283, 0x0284 to 0x0287, 0x0288 to 0x028B, 0x028C to 0x028F, 0x0290 to 0x0293, 0x0294 to 0x0297, 0x0298 to 0x029B, 0x029C to 0x029F, 0x02A0 to 0x02A3, 0x02A4 to 0x02A7, 0x02A8 to 0x02AB, 0x02AC to 0x02AF, 0x02B0 to 0x02B3, 0x02B4 to 0x02B7, 0x02B8 to 0x02BB, 0x02BC to 0x02BF, 0x02C0 to 0x02C3, 0x02C4 to 0x02C7, 0x02C8 to 0x02CB, 0x02CC to 0x02CF, 0x02D0 to 0x02D3, 0x02D4 to 0x02D7, 0x02D8 to 0x02DB, 0x02DC to 0x02DF, 0x02E0 to 0x02E3, 0x02E4 to 0x02E7, 0x02E8 to 0x02EB, 0x02EC to 0x02EF, 0x02F0 to 0x02F3, 0x02F4 to 0x02F7, 0x02F8 to 0x02FB, 0x02FC to 0x02FF, 0x0300 to 0x0303, 0x0304 to 0x0307, 0x0308 to 0x030B, 0x030C to 0x030F, 0x0310 to 0x0313, 0x0314 to 0x0317, 0x0318 to 0x031B, 0x031C to 0x031F, 0x0320 to 0x0323, 0x0324 to 0x0327, 0x0328 to 0x032B, 0x032C to 0x032F, 0x0330 to 0x0333, 0x0334 to 0x0337, 0x0338 to 0x033B, 0x033C to 0x033F, 0x0340 to 0x0343, 0x0344 to 0x0347, 0x0348 to 0x034B, 0x034C to 0x034F, 0x0350 to 0x0353, 0x0354 to 0x0357, 0x0358 to 0x035B, 0x035C to 0x035F, 0x0360 to 0x0363, 0x0364 to 0x0367, 0x0368 to 0x036B, 0x036C to 0x036F, 0x0370 to 0x0373, 0x0374 to 0x0377, 0x0378 to 0x037B, 0x037C to 0x037F, 0x0380 to 0x0383, 0x0384 to 0x0387, 0x0388 to 0x038B, 0x038C to 0x038F, 0x0390 to 0x0393, 0x0394 to 0x0397, 0x0398 to 0x039B, 0x039C to 0x039F, 0x03A0 to 0x03A3, 0x03A4 to 0x03A7, 0x03A8 to 0x03AB, 0x03AC to 0x03AF, 0x03B0 to 0x03B3, 0x03B4 to 0x03B7, 0x03B8 to 0x03BB, 0x03BC to 0x03BF, 0x03C0 to 0x03C3, 0x03C4 to 0x03C7, 0x03C8 to 0x03CB, 0x03CC to 0x03CF, 0x03D0 to 0x03D3, 0x03D4 to 0x03D7, 0x03D8 to 0x03DB, 0x03DC to 0x03DF, 0x03E0 to 0x03E3, 0x03E4 to 0x03E7, 0x03E8 to 0x03EB, 0x03EC to 0x03EF, 0x03F0 to 0x03F3, 0x03F4 to 0x03F7, 0x03F8 to 0x03FB, 0x03FC to 0x03FF, 0x0400 to 0x0403, 0x0404 to 0x0407, 0x0408 to 0x040B, 0x040C to 0x040F, 0x0410 to 0x0413, 0x0414 to 0x0417, 0x0418 to 0x041B, 0x041C to 0x041F, 0x0420 to 0x0423, 0x0424 to 0x0427, 0x0428 to 0x042B, 0x042C to 0x042F, 0x0430 to 0x0433, 0x0434 to 0x0437, 0x0438 to 0x043B, 0x043C to 0x043F, 0x0440 to 0x0443, 0x0444 to 0x0447, 0x0448 to 0x044B, 0x044C to 0x044F, 0x0450 to 0x0453, 0x0454 to 0x0457, 0x0458 to 0x045B, 0x045C to 0x045F, 0x0460 to 0x0463, 0x0464 to 0x0467, 0x0468 to 0x046B, 0x046C to 0x046F, 0x0470 to 0x0473, 0x0474 to 0x0477, 0x0478 to 0x047B, 0x047C to 0x047F, 0x0480 to 0x0483, 0x0484 to 0x0487, 0x0488 to 0x048B, 0x048C to 0x048F, 0x0490 to 0x0493, 0x0494 to 0x0497, 0x0498 to 0x049B, 0x049C to 0x049F, 0x04A0 to 0x04A3, 0x04A4 to 0x04A7, 0x04A8 to 0x04AB, 0x04AC to 0x04AF, 0x04B0 to 0x04B3, 0x04B4 to 0x04B7, 0x04B8 to 0x04BB, 0x04BC to 0x04BF, 0x04C0 to 0x04C3, 0x04C4 to 0x04C7, 0x04C8 to 0x04CB, 0x04CC to 0x04CF, 0x04D0 to 0x04D3, 0x04D4 to 0x04D7, 0x04D8 to 0x04DB, 0x04DC to 0x04DF, 0x04E0 to 0x04E3, 0x04E4 to 0x04E7, 0x04E8 to 0x04EB, 0x04EC to 0x04EF, 0x04F0 to 0x04F3, 0x04F4 to 0x04F7, 0x04F8 to 0x04FB, 0x04FC to 0x04FF, 0x0500 to 0x0503, 0x0504 to 0x0507, 0x0508 to 0x050B, 0x050C to 0x050F, 0x0510 to 0x0513, 0x0514 to 0x0517, 0x0518 to 0x051B, 0x051C to 0x051F, 0x0520 to 0x0523, 0x0524 to 0x0527, 0x0528 to 0x052B, 0x052C to 0x052F, 0x0530 to 0x0533, 0x0534 to 0x0537, 0x0538 to 0x053B, 0x053C to 0x053F, 0x0540 to 0x0543, 0x0544 to 0x0547, 0x0548 to 0x054B, 0x054C to 0x054F, 0x0550 to 0x0553, 0x0554 to 0x0557, 0x0558 to 0x055B, 0x055C to 0x055F, 0x0560 to 0x0563, 0x0564 to 0x0567, 0x0568 to 0x056B, 0x056C to 0x056F, 0x0570 to 0x0573, 0x0574 to 0x0577, 0x0578 to 0x057B, 0x057C to 0x057F, 0x0580 to 0x0583, 0x0584 to 0x0587, 0x0588 to 0x058B, 0x058C to 0x058F, 0x0590 to 0x0593, 0x0594 to 0x0597, 0x0598 to 0x059B, 0x059C to 0x059F, 0x05A0 to 0x05A3, 0x05A4 to 0x05A7, 0x05A8 to 0x05AB, 0x05AC to 0x05AF, 0x05B0 to 0x05B3, 0x05B4 to 0x05B7, 0x05B8 to 0x05BB, 0x05BC to 0x05BF, 0x05C0 to 0x05C3, 0x05C4 to 0x05C7, 0x05C8 to 0x05CB, 0x05CC to 0x05CF, 0x05D0 to 0x05D3, 0x05D4 to 0x05D7, 0x05D8 to 0x05DB, 0x05DC to 0x05DF, 0x05E0 to 0x05E3, 0x05E4 to 0x05E7, 0x05E8 to 0x05EB, 0x05EC to 0x05EF, 0x05F0 to 0x05F3, 0x05F4 to 0x05F7, 0x05F8 to 0x05FB, 0x05FC to 0x05FF, 0x0600 to 0x0603, 0x0604 to 0x0607, 0x0608 to 0x060B, 0x060C to 0x060F, 0x0610 to 0x0613, 0x0614 to 0x0617, 0x0618 to 0x061B, 0x061C to 0x061F, 0x0620 to 0x0623, 0x0624 to 0x0627, 0x0628 to 0x062B, 0x062C to 0x062F, 0x0630 to 0x0633, 0x0634 to 0x0637, 0x0638 to 0x063B, 0x063C to 0x063F, 0x0640 to 0x0643, 0x0644 to 0x0647, 0x0648 to 0x064B, 0x064C to 0x064F, 0x0650 to 0x0653, 0x0654 to 0x0657, 0x0658 to 0x065B, 0x065C to 0x065F, 0x0660 to 0x0663, 0x0664 to 0x0667, 0x0668 to 0x066B, 0x066C to 0x066F, 0x0670 to 0x0673, 0x0674 to 0x0677, 0x0678 to 0x067B, 0x067C to 0x067F, 0x0680 to 0x0683, 0x0684 to 0x0687, 0x0688 to 0x068B, 0x068C to 0x068F, 0x0690 to 0x0693, 0x0694 to 0x0697, 0x0698 to 0x069B, 0x069C to 0x069F, 0x06A0 to 0x06A3, 0x06A4 to 0x06A7, 0x06A8 to 0x06AB, 0x06AC to 0x06AF, 0x06B0 to 0x06B3, 0x06B4 to 0x06B7, 0x06B8 to 0x06BB, 0x06BC to 0x06BF, 0x06C0 to 0x06C3, 0x06C4 to 0x06C7, 0x06C8 to 0x06CB, 0x06CC to 0x06CF, 0x06D0 to 0x06D3, 0x06D4 to 0x06D7, 0x06D8 to 0x06DB, 0x06DC to 0x06DF, 0x06E0 to 0x06E3, 0x06E4 to 0x06E7, 0x06E8 to 0x06EB, 0x06EC to 0x06EF, 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0x07CF, 0x07D0 to 0x07D3, 0x07D4 to 0x07D7, 0x07D8 to 0x07DB, 0x07DC to 0x07DF, 0x07E0 to 0x07E3, 0x07E4 to 0x07E7, 0x07E8 to 0x07EB, 0x07EC to 0x07EF, 0x07F0 to 0x07F3, 0x07F4 to 0x07F7, 0x07F8 to 0x07FB, 0x07FC to 0x07FF, 0x0800 to 0x0803, 0x0804 to 0x0807, 0x0808 to 0x080B, 0x080C to 0x080F, 0x0810 to 0x0813, 0x0814 to 0x0817, 0x0818 to 0x081B, 0x081C to 0x081F, 0x0820 to 0x0823, 0x0824 to 0x0827, 0x0828 to 0x082B, 0x082C to 0x082F, 0x0830 to 0x0833, 0x0834 to 0x0837, 0x0838 to 0x083B, 0x083C to 0x083F, 0x0840 to 0x0843, 0x0844 to 0x0847, 0x0848 to 0x084B, 0x084C to 0x084F, 0x0850 to 0x0853, 0x0854 to 0x0857, 0x0858 to 0x085B, 0x085C to 0x085F, 0x0860 to 0x0863, 0x0864 to 0x0867, 0x0868 to 0x086B, 0x086C to 0x086F, 0x0870 to 0x0873, 0x0874 to 0x0877, 0x0878 to 0x087B, 0x087C to 0x087F, 0x0880 to 0x0883, 0x0884 to 0x0887, 0x0888 to 0x088B, 0x088C to 0x088F, 0x0890 to 0x0893, 0x0894 to 0x0897, 0x0898 to 0x089B, 0x089C to 0x089F, 0x08A0 to 0x08A3, 0x08A4 to 0x08A7, 0x08A8 to 0x08AB, 0x08AC to 0x08AF, 0x08B0 to 0x08B3, 0x08B4 to 0x08B7, 0x08B8 to 0x08BB, 0x08BC to 0x08BF, 0x08C0 to 0x08C3, 0x08C4 to 0x08C7, 0x08C8 to 0x08CB, 0x08CC to 0x08CF, 0x08D0 to 0x08D3, 0x08D4 to 0x08D7, 0x08D8 to 0x08DB, 0x08DC to 0x08DF, 0x08E0 to 0x08E3, 0x08E4 to 0x08E7, 0x08E8 to 0x08EB, 0x08EC to 0x08EF, 0x08F0 to 0x08F3, 0x08F4 to 0x08F7, 0x08F8 to 0x08FB, 0x08FC to 0x08FF, 0x0900 to 0x0903, 0x0904 to 0x0907, 0x0908 to 0x090B, 0x090C to 0x090F, 0x0910 to 0x0913, 0x0914 to 0x0917, 0x0918 to 0x091B, 0x091C to 0x091F, 0x0920 to 0x0923, 0x0924 to 0x0927, 0x0928 to 0x092B, 0x092C to 0x092F, 0x0930 to 0x0933, 0x0934 to 0x0937, 0x0938 to 0x093B, 0x093C to 0x093F, 0x0940 to 0x0943, 0x0944 to 0x0947, 0x0948 to 0x094B, 0x094C to 0x094F, 0x0950 to 0x0953, 0x0954 to 0x0957, 0x0958 to 0x095B, 0x095C to 0x095F, 0x0960 to 0x0963, 0x0964 to 0x0967, 0x0968 to 0x096B, 0x096C to 0x096F, 0x0970 to 0x0973, 0x0974 to 0x0977, 0x0978 to 0x097B, 0x097C to 0x097F, 0x0980 to 0x0983, 0x0984 to 0x0987, 0x0988 to 0x098B, 0x098C to 0x098F, 0x0990 to 0x0993, 0x0994 to 0x0997, 0x0998 to 0x099B, 0x099C to 0x099F, 0x09A0 to 0x09A3, 0x09A4 to 0x09A7, 0x09A8 to 0x09AB, 0x09AC to 0x09AF, 0x09B0 to 0x09B3, 0x09B4 to 0x09B7, 0x09B8 to 0x09BB, 0x09BC to 0x09BF, 0x09C0 to 0x09C3, 0x09C4 to 0x09C7, 0x09C8 to 0x09CB, 0x09CC to 0x09CF, 0x09D0 to 0x09D3, 0x09D4 to 0x09D7, 0x09D8 to 0x09DB, 0x09DC to 0x09DF, 0x09E0 to 0x09E3, 0x09E4 to 0x09E7, 0x09E8 to 0x09EB, 0x09EC to 0x09EF, 0x09F0 to 0x09F3, 0x09F4 to 0x09F7, 0x09F8 to 0x09FB, 0x09FC to 0x09FF, 0x0A00 to 0x0A03, 0x0A04 to 0x0A07, 0x0A08 to 0x0A0B, 0x0A0C to 0x0A0F, 0x0A10 to 0x0A13, 0x0A14 to 0x0A1



3. Updated R0x3060 Register Description

Old Register Description:

R12384 R0x3060	15:0	0x0000	ANALOG_GAIN (R/W)	Y	N
	15	X	Reserved		
	14:12	0x0000	COARSE_GAIN_CB Coarse Analog gain in context B. Gain is 2 power of the register value.	Y	N
	11:8	0x0000	FINE_GAIN_CB Fine analog gain in context B	Y	N
	7	X	Reserved		
	6:4	0x0000	COARSE_GAIN Coarse Analog gain in context A. Gain is 2 power of the register value.	Y	N
	3:0	0x0000	FINE_GAIN Fine analog gain in context A.	Y	N
Defines analog gains for both contexts $\text{analog_gain} = 2^{\text{coarse_gain}} \cdot \left(\frac{32}{32 - \text{fine_gain}} \right)$					

New Register Description:

Register Hex	Bits	Default	Name	Attributes			
R0x3060	15:0	0x0000	ANALOG_GAIN (R/W)	S			
	15	X	Reserved				
	14:12	0x0000	COARSE_GAIN_CB Coarse Analog gain in context B. Gain is 2 power of the register value.	S			
	11:8	0x0000	FINE_GAIN_CB Fine analog gain in context B	S			
	7	X	Reserved				
	6:4	0x0000	COARSE_GAIN Coarse Analog gain in context A. Gain is 2 power of the register value.	S			
	3:0	0x0000	FINE_GAIN Fine analog gain in context A.	S			
Defines analog gains for both contexts $\text{analog_gain} = 2^{\text{coarse_gain}} \cdot \left(\frac{32}{32 - \text{fine_gain}} \right)$							

4. Added register R0x30FE

New Register Description:

R0x30FE	15:0	0x0080	NOISE_PEDESTAL (R/W)				
	Pedestal added prior to memory operations. Noise pedestal and AdaCD pedestals should be set to the same value.						



5. Updated R0x31E0 Register Description

Old Register Description:

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R11768 R0x31E0	15:0	0x0000	PIX_DEF_ID (R/W)	N	N
	15	0x0000	Reserved		
	14	0x0000	Reserved		
	13	X	Reserved		
	12	0x0000	Reserved		
	11	0x0000	Reserved		
	10	0x0000	Reserved		
	9	0x0000	Reserved		
	8	0x0000	Reserved		
	7:2	X	Reserved		
	1	0x0000	Reserved		
	0	0x0000	ENABLE Enable pixel defect correction.	N	N

New Register Description

Register Hex	Bits	Default	Name	Attributes			
R0x31E0	15:0	0x0000	PIX_DEF_ID (R/W)				
	15	0x0000	Reserved				
	14	0x0000	Reserved				
	13	X	Reserved				
	12	0x0000	Reserved				
	11	0x0000	Reserved				
	10	0x0000	Reserved				
	9	0x0000	Reserved				
	8	0x0000	Reserved				
	7:2	X	Reserved				
	1	0x0000	CORRECTION_MODE Mode of pixel defect correction. 0: Tags bad pixels with the reserved value 0. 1: Corrects bad pixels using the traditional 1D correction scheme.		Y		
	0	0x0000	ENABLE Enable pixel defect correction.		Y		

List of Affected Standard Parts:

Note: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the [PCN Customized Portal](#).

AR0237CSSC12SHRA0-DR	AR0237CSSC12SPRA0-DR	AR0237IRSH12SHRA0-DR
AR0237IRSH12SPRA0-DR		

Japanese translation of the notification starts here.
通知の日本語訳はここから始まります。

Note: *The Japanese version is for reference only. In case of any differences between the English and Japanese version, the English version shall control.*

注：日本語版は参照用です。英語版と日本語版の違いがある場合は、英語版が優先されます。



変更件名:	AR0237 レジスタリファレンスの変更	
発効日:	24 February 2020	
連絡先情報:	現地のオン・セミコンダクター営業所または <Sonya.Yip@onsemi.com> にお問い合わせください。	
通知種別:	本製品速報は通知目的のみのものです。オン・セミコンダクターは本製品速報の発行により本変更を実行します。	
変更カテゴリ:	資料変更	
変更サブカテゴリ:	データシート/製品資料の変更	
影響を受ける拠点:	オン・セミコンダクター拠点: なし	外部製造工場 / 下請業者拠点: なし
<p>説明および目的:</p> <p>AR0237CS レジスタリファレンスが新しい情報を元に更新されました。 この変更は製品の形状、適合性、または機能に影響を及ぼしません。</p> <p>AR0237CS レジスタリファレンスの変更</p> <p>1. 追加されたレジスタ属性情報を含み更新された導入セクション</p> <p>以前の導入セクション:</p> <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>Bad Frames</p> <p>A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame. Many changes to the sensor register settings can cause a bad frame. For example, when line_length_pck (R0x0342-3) is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.</p> <p>Register Map</p> <p>The tables in this section show which locations are used within the 16-bit address space. Locations that are not shown in the table are reserved for future use; to maintain compatibility with future designs they should not be read from or written to. Locations that are shown as "Reserved" should not be accessed. The default read values of registers are subject to change.</p> </div> <div style="width: 45%;"> <p>By default, bad frames are not masked. In the register tables, the "Bad Frame" column shows where changing a register or register field will cause a bad frame. This notation is used:</p> <ul style="list-style-type: none"> • <i>N</i>—No. Changing the register value will not produce a bad frame. • <i>Y</i>—Yes. Changing the register value might produce a bad frame. • <i>YM</i>—Yes; but the bad frame will be masked out when mask_corrupted_frames (R0x0105) is set to "1." <p>CAUTION: The effect of writing to reserved registers is undefined and may include the possibility of causing permanent electrical damage to the sensor.</p> <p>Table 1 below lists registers and their default values. Register addresses are shown as 16-bit values in both decimal and hexadecimal. Table 2 lists registers and their descriptions.</p> </div> </div>		



新しい導入セクション:

Buffering

In register tables, buffering shows the timing with which a newly-written register value takes effect. The notation used is:

Blank – Unbuffered. By default register update takes effect immediately.

S – Single frame sync'd. Register update in frame N takes effect in frame N+1.

D – Double frame sync'd. Register update in frame N takes effect in frame N+2.

Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame.

Many changes to the sensor register settings can cause a bad frame. For example, when `line_length_pck` is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

By default, bad frames are not masked. If the masked bad frame option is enabled, both LV and FV are inhibited for these frames so that the vertical blanking time between frames is extended by the frame time.

In the register tables, the "Bad Frame" column shows where changing a register or register field will cause a bad frame. This notation is used:

Blank – No. Changing the register value will not produce a bad frame.

Y – Yes. Changing the register value might produce a bad frame.

YM – Yes. But the bad frame will be masked out when `mask_corrupted_frames` (R0x301A[9]) is set to "1".

Embedded

In register tables, the embedded column notes whether or not the register is present in the per_frame embedded data.

The notation used is:

Blank – By default, a register is not present in the embedded data

E – The register is present in the embedded data.

Locked

In register tables, locked notes whether writes to the register are protected by R0x3010. The notation used is

Blank – By default, writes to a register are not protected by R0x3010

L – Writes to the register are protected by R0x3010

2. レジスタリファレンス内の全てのレジスタについて、Frame Syn'd 列および Bad Frame 列を新しい属性列と入れ替え

以前のレジスタ記述列の例

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12288 R0x3000	15:0	0x0356	CHIP_VERSION_REG (R/W)	N	N
		Model ID. Read-only. Can be made read/write by clearing R0x301A-B[3].			
R12290 R0x3002	15:0	0x0004	Y_ADDR_START (R/W)	Y	YM
		The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value.			

新しいレジスタ記述列の例:

Attributes Columns: Usage and Values, left to right

Column 1: Buffering <blank> = Unbuffered S = Single Frame Sync'd D = Double Frame Sync'd	Column 2: Bad Frame <blank> = No bad frame Y = Causes a bad frame YM = Maskable bad frame	Column 3: Embedded <blank> = Not embedded E = embedded	Column 4: Locked <blank> = Not locked L = locked
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Register Hex	Bits	Default	Name	Attributes			
R0x3000	15:0	0x0256	CHIP_VERSION_REG (R/W)				
	Model ID. Read-only. Can be made read/write by clearing R0x301A-B[3].						
R0x3002	15:0	0x0000	Y_ADDR_START (R/W)	S	YM		
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value.						

3. 更新した R0x3060 レジスタ記述

以前のレジスタ記述:

R12354 R0x3060	15:0	0x0000	ANALOG_GAIN (R/W)	Y	N
	15	X	Reserved		
	14:12	0x0000	COARSE_GAIN_CB Coarse Analog gain in context B. Gain is 2 power of the register value.	Y	N
	11:8	0x0000	FINE_GAIN_CB Fine analog gain in context B	Y	N
	7	X	Reserved		
	6:4	0x0000	COARSE_GAIN Coarse Analog gain in context A. Gain is 2 power of the register value.	Y	N
	3:0	0x0000	FINE_GAIN Fine analog gain in context A.	Y	N
Defines analog gains for both contexts $\text{analog_gain} = 2^{\text{coarse_gain}} \cdot \left(\frac{32}{2^{\text{coarse_gain}} + \text{fine_gain}} \right)$					

新しいレジスタ記述:

Register Hex	Bits	Default	Name	Attributes			
R0x3060	15:0	0x0000	ANALOG_GAIN (R/W)	S			
	15	X	Reserved				
	14:12	0x0000	COARSE_GAIN_CB Coarse Analog gain in context B. Gain is 2 power of the register value.	S			
	11:8	0x0000	FINE_GAIN_CB Fine analog gain in context B	S			
	7	X	Reserved				
	6:4	0x0000	COARSE_GAIN Coarse Analog gain in context A. Gain is 2 power of the register value.	S			
	3:0	0x0000	FINE_GAIN Fine analog gain in context A.	S			
Defines analog gains for both contexts							



4. 追加したレジスタ R0x30FE

新しいレジスタ記述:

R0x30FE	15:0	0x0080	NOISE_PEDESTAL (R/W)				
	Pedestal added prior to memory operations. Noise pedestal and AdaCD pedestals should be set to the same value.						

5. 更新した R0x31E0 レジスタ記述

以前のレジスタ記述:

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12768 R0x31E0	15:0	0x0000	PIX_DEF_ID (R/W)	N	N
	15	0x0000	Reserved		
	14	0x0000	Reserved		
	13	X	Reserved		
	12	0x0000	Reserved		
	11	0x0000	Reserved		
	10	0x0000	Reserved		
	9	0x0000	Reserved		
	8	0x0000	Reserved		
	7:2	X	Reserved		
	1	0x0000	Reserved		
	0	0x0000	ENABLE Enable pixel defect correction.	N	N

新しいレジスタ記述:

Register Hex	Bits	Default	Name	Attributes			
R0x31E0	15:0	0x0000	PIX_DEF_ID (R/W)				
	15	0x0000	Reserved				
	14	0x0000	Reserved				
	13	X	Reserved				
	12	0x0000	Reserved				
	11	0x0000	Reserved				
	10	0x0000	Reserved				
	9	0x0000	Reserved				
	8	0x0000	Reserved				
	7:2	X	Reserved				
	1	0x0000	CORRECTION_MODE Mode of pixel defect correction. 0: Tags bad pixels with the reserved value 0. 1: Corrects bad pixels using the traditional 1D correction scheme.		Y		
	0	0x0000	ENABLE Enable pixel defect correction.		Y		

**影響を受ける部品の一覧:**

注: 標準の部品番号(既製品)のみが部品一覧に記載されます。本 PCN に影響を受けるカスタム 部品は、PCN メールのお客様の特定の PCN の付属文書、または PCN カスタマイズポータルに記載されています。

AR0237CSSC12SHRA0-DR	AR0237CSSC12SPRA0-DR	AR0237IRSH12SHRA0-DR
AR0237IRSH12SPRA0-DR		