ON Semiconductor®

Product Bulletin

Document #:PB23131X
Issue Date:24 Feb 2020

Title of Change:	AR0237 Register Reference Changes
Effective date:	24 Feb 2020
Contact information:	Contact your local ON Semiconductor Sales Office or Sonya.Yip@onsemi.com
Type of notification:	This Product Bulletin is for notification purposes only. ON Semiconductor will proceed with implementation of this change upon publication of this Product Bulletin.
Change Category:	Documentation Change
Change Sub-Category(s):	Datasheet/Product Doc change

Sites Affected:

ON Semiconductor Sites	**External Foundry/Subcon Sites**
None	None

Description and Purpose:

The AR0237CS Register Reference has been updated with new information. These changes do not affect form, fit, or function of the product.

AR0237CS Register Reference Changes

1. Updated Introduction section with information about register attributes being added

Old Introduction Section:

Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame. Many changes to the sensor register settings can cause a bad frame. For example, when line_length_pck (R0x0342–3) is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

Register Map

The tables in this section show which locations are used within the 16–bit address space. Locations that are not shown in the table are reserved for future use; to maintain compatibility with future designs they should not be read from or written to. Locations that are shown as "Reserved" should not be accessed. The default read values of registers are subject to change.

By default, bad frames are not masked. In the register tables, the "Bad Frame" column shows where changing a register or register field will cause a bad frame. This notation is used:

- *N*—No. Changing the register value will not produce a bad frame.
- *Y*—Yes. Changing the register value might produce a bad frame.
- *YM*—Yes; but the bad frame will be masked out when mask_corrupted_frames (R0x0105) is set to "1."

CAUTION: The effect of writing to reserved registers is undefined and may include the possibility of causing permanent electrical damage to the sensor.

Table 1 below lists registers and their default values. Register addresses are shown as 16– bit values in both decimal and hexadecimal. Table 2 lists registers and their descriptions.

New Introduction Section:

Buffering

In register tables, buffering shows the timing with which a newly−written register value takes effect. The notation used is:

Blank – Unbuffered. By default register update takes effect immediately.

S – Single frame sync'd. Register update in frame N takes effect in frame N+1.

D –Double frame sync'd. Register update in frame N takes effect in frame N+2.

Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame.

Many changes to the sensor register settings can cause a bad frame. For example, when line_length_pck is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

By default, bad frames are not masked. If the masked bad frame option is enabled, both LV and FV are inhibited for these frames so that the vertical blanking time between frames is extended by the frame time.

In the register tables, the "Bad Frame" column shows where changing a register or register field will cause a bad frame. This notation is used:

Blank – No. Changing the register value will not produce a bad frame.

Y – Yes. Changing the register value might produce a bad frame.

YM – Yes. But the bad frame will be masked out when mask_corrupted_frames (R0x301A[9]) is set to "1".

Embedded

In register tables, the embedded column notes whether or not the register is present in the per_frame embedded data.

The notation used is:

Blank – By default, a register is not present in the embedded data

E – The register is present in the embedded data.

Locked

In register tables, locked notes whether writes to the register are protected by R0x3010. The notation used is

Blank – By default, writes to a register are not protected by R0x3010

L – Writes to the register are protected by R0x3010

2. Replaced Frame Syn'd and Bad Frame columns with new attribute columns for all registers in the Register Reference

Old Register Description Column Example:

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12288 R0x3000	15:0	0x0356	CHIP_VERSION_REG (R/W)	N	N
	Model ID. Read-only. Can be made read/write by clearing R0x301A−B[3].				
R12290 R0x3002	15:0	0x0004	Y_ADDR_START (R/W)	Y	YM
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value.				

New Register Description Column Example:

Attributes Columns; Usage and Values, left to right

Column 1: Buffering	Column 2: Bad Frame	Column 3: Embedded	Column 4: Locked
<blank> = Unbuffered S = Single Frame Synced D = Double Frame Synced	<blank> = No bad frame Y = Causes a bad frame YM = Maskable bad frame	<blank> = Not embedded E = embedded	<blank> = Not locked L = locked

Register Hex	Bits	Default	Name	Attributes			
R0x3000	15:0	0x0256	CHIP_VERSION_REG (R/W)				
	Model ID. Read−only. Can be made read/write by clearing R0x301A−B[3].						
R0x3002	15:0	0x0000	Y_ADDR_START (R/W)	S	YM		
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value.						

3. Updated R0x3060 Register Description

Old Register Description:

R12384 R0x3060	15:0	0x0000	ANALOG_GAIN (R/W)	Y	N
	15	X	Reserved		
	14:12	0x0000	COARSE_GAIN_CB Coarse Analog gain in context B. Gain is 2 power of the register value.	Y	N
	11:8	0x0000	FINE_GAIN_CB Fine analog gain in context B	Y	N
	7	X	Reserved		
	6:4	0x0000	COARSE_GAIN Coarse Analog gain in context A. Gain is 2 power of the register value.	Y	N
	3:0	0x0000	FINE_GAIN Fine analog gain in context A.	Y	N
	Defines analog gains for both contexts $analog\_gain = 2^{coarse\_gain} \cdot \left(\frac{32}{32 - fine\_gain}\right)$				

New Register Description:

Register Hex	Bits	Default	Name	Attributes			
R0x3060	15:0	0x0000	ANALOG_GAIN (R/W)	S			
	15	X	Reserved				
	14:12	0x0000	COARSE_GAIN_CB Coarse Analog gain in context B. Gain is 2 power of the register value.	S			
	11:8	0x0000	FINE_GAIN_CB Fine analog gain in context B	S			
	7	X	Reserved				
	6:4	0x0000	COARSE_GAIN Coarse Analog gain in context A. Gain is 2 power of the register value.	S			
	3:0	0x0000	FINE_GAIN Fine analog gain in context A.	S			
	Defines analog gains for both contexts						

4. Added register R0x30FE

New Register Description:

R0x30FE	15:0	0x0080	NOISE_PEDESTAL (R/W)				
	Pedestal added prior to memory operations. Noise pedestal and AdaCD pedestals should be set to the same value.						

5. Updated R0x31E0 Register Description

Old Register Description:

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12768 R0x31E0	15:0	0x0000	PIX_DEF_ID (R/W)	N	N
	15	0x0000	Reserved		
	14	0x0000	Reserved		
	13	X	Reserved		
	12	0x0000	Reserved		
	11	0x0000	Reserved		
	10	0x0000	Reserved		
	9	0x0000	Reserved		
	8	0x0000	Reserved		
	7:2	X	Reserved		
	1	0x0000	Reserved		
	0	0x0000	ENABLE Enable pixel defect correction.	N	N

New Register Description

Register Hex	Bits	Default	Name	Attributes			
R0x31E0	15:0	0x0000	PIX_DEF_ID (R/W)				
	15	0x0000	Reserved				
	14	0x0000	Reserved				
	13	X	Reserved				
	12	0x0000	Reserved				
	11	0x0000	Reserved				
	10	0x0000	Reserved				
	9	0x0000	Reserved				
	8	0x0000	Reserved				
	7:2	X	Reserved				
	1	0x0000	CORRECTION_MODE Mode of pixel defect correction. 0: Tags bad pixels with the reserved value 0. 1: Corrects bad pixels using the traditional 1D correction scheme.		Y		
	0	0x0000	ENABLE Enable pixel defect correction.		Y		

List of Affected Standard Parts:

***Note**: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal**.*

AR0237CSSC12SHRA0-DR	AR0237CSSC12SPRA0-DR	AR0237IRSH12SHRA0-DR
AR0237IRSH12SPRA0-DR		

Japanese translation of the notification starts here.

通知の日本語訳はここから始まります。

Note*: The Japanese version is for reference only. In case of any differences between the English and Japanese version, the English version shall control.*

注：日本語版は参照用です。英語版と日本語版の違いがある場合は、英語版が優先されます.

ON Semiconductor®

製品速報

文書番号: PB23131X
発行日: 24 Feb 2020

変更件名:	AR0237 レジスタ リファレンスの変更	
発効日:	24 February 2020	
連絡先情報:	現地のオン・セミコンダクター営業所または <Sonya.Yip@onsemi.com> にお問い合わせください。	
通知種別:	本製品速報は通知目的のみのものです。オン・セミコンダクターは本製品速報の発行により本変更を実行します。	
変更カテゴリ:	資料変更	
変更サブカテゴリ:	データシート/製品資料の変更	
影響を受ける拠点:	オン・セミコンダクター拠点: なし	外部製造工場 / 下請業者拠点: なし

説明および目的:

AR0237CS レジスタ リファレンスが新しい情報を元に更新されました。
この変更は製品の形状、適合性、または機能に影響を及ぼしません。

AR0237CS レジスタ リファレンスの変更

1. 追加されたレジスタ属性情報を含み更新された導入セクション

以前の導入セクション:

Bad Frames

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CAUTION: The effect of writing to reserved registers is undefined and may include the possibility of causing permanent electrical damage to the sensor.

Table 1 below lists registers and their default values. Register addresses are shown as 16– bit values in both decimal and hexadecimal. Table 2 lists registers and their descriptions.

新しい導入セクション:

Buffering

In register tables, buffering shows the timing with which a newly−written register value takes effect. The notation used is:

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A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame.

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YM – Yes. But the bad frame will be masked out when mask_corrupted_frames (R0x301A[9]) is set to "1".

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The notation used is:

Blank – By default, a register is not present in the embedded data

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Locked

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Blank – By default, writes to a register are not protected by R0x3010

L – Writes to the register are protected by R0x3010

2. レジスタ リファレンス内の全てのレジスタについて、Frame Syn'd 列および Bad Frame 列を新しい属性列と入れ替え

以前のレジスタ記述列の例

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12288 R0x3000	15:0	0x0356	CHIP_VERSION_REG (R/W)	N	N
	Model ID. Read-only. Can be made read/write by clearing R0x301A−B[3].				
R12290 R0x3002	15:0	0x0004	Y_ADDR_START (R/W)	Y	YM
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value.				

新しいレジスタ記述列の例:

Attributes Columns; Usage and Values, left to right

Column 1: Buffering	Column 2: Bad Frame	Column 3: Embedded	Column 4: Locked
<blank> = Unbuffered S = Single Frame Synced D = Double Frame Synced	<blank> = No bad frame Y = Causes a bad frame YM = Maskable bad frame	<blank> = Not embedded E = embedded	<blank> = Not locked L = locked

Register Hex	Bits	Default	Name	Attributes			
R0x3000	15:0	0x0256	CHIP_VERSION_REG (R/W)				
	Model ID. Read-only. Can be made read/write by clearing R0x301A-B[3].						
R0x3002	15:0	0x0000	Y_ADDR_START (R/W)	S	YM		
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value.						

3. 更新した R0x3060 レジスタ記述

以前のレジスタ記述:

R12384 R0x3060	15:0	0x0000	ANALOG_GAIN (R/W)	Y	N
	15	X	Reserved		
	14:12	0x0000	COARSE_GAIN_CB Coarse Analog gain in context B. Gain is 2 power of the register value.	Y	N
	11:8	0x0000	FINE_GAIN_CB Fine analog gain in context B	Y	N
	7	X	Reserved		
	6:4	0x0000	COARSE_GAIN Coarse Analog gain in context A. Gain is 2 power of the register value.	Y	N
	3:0	0x0000	FINE_GAIN Fine analog gain in context A.	Y	N
	Defines analog gains for both contexts $analog\_gain = 2^{coarse\_gain} \cdot \left(\frac{32}{32 - fine\_gain}\right)$				

新しいレジスタ記述:

Register Hex	Bits	Default	Name	Attributes			
R0x3060	15:0	0x0000	ANALOG_GAIN (R/W)	S			
	15	X	Reserved				
	14:12	0x0000	COARSE_GAIN_CB Coarse Analog gain in context B. Gain is 2 power of the register value.	S			
	11:8	0x0000	FINE_GAIN_CB Fine analog gain in context B	S			
	7	X	Reserved				
	6:4	0x0000	COARSE_GAIN Coarse Analog gain in context A. Gain is 2 power of the register value.	S			
	3:0	0x0000	FINE_GAIN Fine analog gain in context A.	S			
	Defines analog gains for both contexts						

4. 追加したレジスタ R0x30FE

新しいレジスタ記述:

R0x30FE	15:0	0x0080	NOISE_PEDESTAL (R/W)				
	Pedestal added prior to memory operations. Noise pedestal and AdaCD pedestals should be set to the same value.						

5. 更新した R0x31E0 レジスタ記述

以前のレジスタ記述:

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12768 R0x31E0	15:0	0x0000	PIX_DEF_ID (R/W)	N	N
	15	0x0000	Reserved		
	14	0x0000	Reserved		
	13	X	Reserved		
	12	0x0000	Reserved		
	11	0x0000	Reserved		
	10	0x0000	Reserved		
	9	0x0000	Reserved		
	8	0x0000	Reserved		
	7:2	X	Reserved		
	1	0x0000	Reserved		
	0	0x0000	ENABLE Enable pixel defect correction.	N	N

新しいレジスタ記述:

Register Hex	Bits	Default	Name	Attributes			
R0x31E0	15:0	0x0000	PIX_DEF_ID (R/W)				
	15	0x0000	Reserved				
	14	0x0000	Reserved				
	13	X	Reserved				
	12	0x0000	Reserved				
	11	0x0000	Reserved				
	10	0x0000	Reserved				
	9	0x0000	Reserved				
	8	0x0000	Reserved				
	7:2	X	Reserved				
	1	0x0000	CORRECTION_MODE Mode of pixel defect correction. 0: Tags bad pixels with the reserved value 0. 1: Corrects bad pixels using the traditional 1D correction scheme.		Y		
	0	0x0000	ENABLE Enable pixel defect correction.		Y		

影響を受ける部品の一覧:

注: 標準の部品番号(既製品)のみが部品一覧に記載されます。 本 PCN に影響を受けるカスタム 部品は、PCN メールの顧客の特定の PCN の付属文書、または PCN カスタマイズポータルに記載されています。

AR0237CSSC12SHRA0-DR	AR0237CSSC12SPRA0-DR	AR0237IRSH12SHRA0-DR
AR0237IRSH12SPRA0-DR		