Product Bulletin

Document #:PB24313X
Issue Date:13 May 2022

Title of Change:	RSL10 Recommended Retention Regulator and RC Oscillator Settings Pertaining to Sleep Mode
Effective date:	13 May 2022
Contact information:	Contact your local onsemi Sales Office or Ben.Widsten@onsemi.com
Type of notification:	This Product Bulletin is for notification purposes only. onsemi will proceed with implementation of this change upon publication of this Product Bulletin.
Change Category:	Improvemed firmware settings
Change Sub-Category(s):	Datasheet/Product Doc change

Sites Affected:

onsemi Sites	**External Foundry/Subcon Sites**
None	None

Description and Purpose:

For NCH-RSL10-101Q48-ABG, NCH-RSL10-101WC51-ABG and NCH-RSL10-101S51-ACG it is recommended to set the retention regulator trim setting for VDDMRET, VDDTRET and VDDCRET to 1 and to set the RC oscillator frequency to 3MHz prior to entering sleep mode for proper functionality across the operating temperature. The settings are to be applied by the customer in the customer's firmware. If the settings are not applied, RSL10 may not wake properly from sleep mode across the operating temperature. RSL10 SDK 3.6 reflects these changes. These changes will not impact form, fit, or function of product(s).

List of Affected Standard Parts:

***Note**: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal**.*

NCH-RSL10-101S51-ACG	NCH-RSL10-101WC51-ABG	NCH-RSL10-101Q48-ABG