# SiC JFET Division

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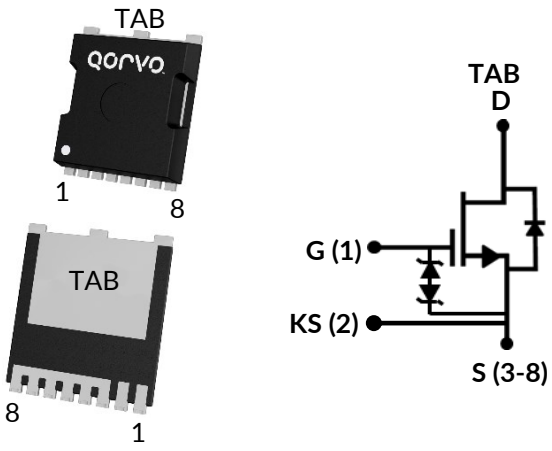
DATASHEET

# UJ4SC075010L8S




| Part Number | Package | Marking |
|---|---|---|
| UJ4SC075010L8S | MO-229 | UJ4SC075010L8S |

RoHS COMPLIANT | Pb LEAD FREE | HF HALOGEN FREE

# Silicon Carbide (SiC) Cascode JFET - EliteSiC, Power N-Channel, TOLL, 750V, 10.7 mohm

Rev. C, January 2025

## Description

The UJ4SC075010L8S is a 750V, 10.7mΩ G4 SiC FET. It is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows use of off-the-shelf gate drivers hence requiring minimal re-design when replacing Si IGBTs, Si superjunction devices or SiC MOSFETs. Available in the space-saving MO-229 package which enables automated assembly, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

## Features

- On-resistance $R_{DS(on)}$: 10.7mΩ (typ)
- Operating temperature: 175°C (max)
- Excellent reverse recovery: $Q_{rr}$ = 274nC
- Low body diode $V_{FSD}$: 1.1V
- Low gate charge: $Q_G$ =75nC
- Threshold voltage $V_{G(th)}$: 4.5V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected, HBM class 2
- MO-229 package for faster switching, clean gate waveforms

## Typical applications

- Solid state relays and circuit-breakers
- Line rectification and active-bridge rectification circuits in AC/DC front-ends
- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

## Maximum Ratings

| Parameter | Symbol | Test Conditions | Value | Units |
|---|---|---|---|---|
| Drain-source voltage | $V_{DS}$ | | 750 | V |
| Gate-source voltage | $V_{GS}$ | DC | -20 to +20 | V |
| | | AC (f > 1Hz) | -25 to +25 | V |
| Continuous drain current [1] | $I_D$ | $T_C$ < 75°C | 106 | A |
| | | $T_C$ = 100°C | 92 | A |
| Pulsed drain current [2] | $I_{DM}$ | $T_C$ = 25°C | 300 | A |
| Single pulsed avalanche energy [3] | $E_{AS}$ | L=15mH, $I_{AS}$ = 4.5A | 151 | mJ |
| SiC FET dv/dt ruggedness | dv/dt | $V_{DS}$ [ 500V | 100 | V/ns |
| Power dissipation | $P_{tot}$ | $T_C$ = 25°C | 556 | W |
| Maximum junction temperature | $T_{J,max}$ | | 175 | °C |
| Operating and storage temperature | $T_J$, $T_{STG}$ | | -55 to 175 | °C |
| Reflow soldering temperature | $T_{solder}$ | reflow MSL 1 | 260 | °C |

1. Limited by bondwires
2. Pulse width $t_p$ limited by $T_{J,max}$
3. Starting $T_J$ = 25°C

## Thermal Characteristics

| Parameter | Symbol | Test Conditions | Value | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Thermal resistance, junction-to-case | $R_{\theta JC}$ | | | 0.21 | 0.27 | °C/W |

## Electrical Characteristics ($T_J$ = +25°C unless otherwise specified)

### Typical Performance - Static

| Parameter | Symbol | Test Conditions | Value | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Drain-source breakdown voltage | $BV_{DS}$ | $V_{GS}$=0V, $I_D$=1mA | 750 | | | V |
| Total drain leakage current | $I_{DSS}$ | $V_{DS}$=750V, $V_{GS}$=0V, $T_J$=25°C | | 3.5 | 60 | µA |
| | | $V_{DS}$=750V, $V_{GS}$=0V, $T_J$=175°C | | 45 | | |
| Total gate leakage current | $I_{GSS}$ | $V_{DS}$=0V, $T_J$=25°C, $V_{GS}$=-20V / +20V | | 2 | 20 | µA |
| Drain-source on-resistance | $R_{DS(on)}$ | $V_{GS}$=12V, $I_D$=60A, $T_J$=25°C | | 10.7 | 14.2 | mΩ |
| | | $V_{GS}$=12V, $I_D$=60A, $T_J$=125°C | | 18.1 | | |
| | | $V_{GS}$=12V, $I_D$=60A, $T_J$=175°C | | 24 | | |
| Gate threshold voltage | $V_{G(th)}$ | $V_{DS}$=5V, $I_D$=10mA | 3.5 | 4.5 | 5.5 | V |
| Gate resistance | $R_G$ | f=1MHz, open drain | | 2.3 | | Ω |

### Typical Performance - Reverse Diode

| Parameter | Symbol | Test Conditions | Value | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Diode continuous forward current [1] | $I_S$ | $T_C$ < 75°C | | | 106 | A |
| Diode pulse current [2] | $I_{S,pulse}$ | $T_C$=25°C | | | 300 | A |
| Forward voltage | $V_{FSD}$ | $V_{GS}$=0V, Is=30A, $T_J$=25°C | | 1.1 | 1.24 | V |
| | | $V_{GS}$=0V, $I_S$=30A, $T_J$=175°C | | 1.2 | | |
| Reverse recovery charge | $Q_{rr}$ | $V_{DS}$=400V, $I_S$=60A, $V_{GS}$=0V, $R_G$=30Ω di/dt=2500A/µs, $T_J$=25°C | | 274 | | nC |
| Reverse recovery time | $t_{rr}$ | | | 18.5 | | ns |
| Reverse recovery charge | $Q_{rr}$ | $V_{DS}$=400V, $I_S$=60A, $V_{GS}$=0V, $R_G$=30Ω di/dt=2500A/µs, $T_J$=150°C | | 290 | | nC |
| Reverse recovery time | $t_{rr}$ | | | 20 | | ns |

## Typical Performance - Dynamic

| Parameter | Symbol | Test Conditions | Value | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Input capacitance | $C_{iss}$ | $V_{DS}$=400V, $V_{GS}$=0V f=100kHz | | 3245 | | pF |
| Output capacitance | $C_{oss}$ | | | 178 | | |
| Reverse transfer capacitance | $C_{rss}$ | | | 1.2 | | |
| Effective output capacitance, energy related | $C_{oss(er)}$ | $V_{DS}$=0V to 400V, $V_{GS}$=0V | | 225 | | pF |
| Effective output capacitance, time related | $C_{oss(tr)}$ | $V_{DS}$=0V to 400V, $V_{GS}$=0V | | 470 | | pF |
| $C_{OSS}$ stored energy | $E_{oss}$ | $V_{DS}$=400V, $V_{GS}$=0V | | 18 | | µJ |
| Total gate charge | $Q_G$ | $V_{DS}$=400V, $I_D$=60A, $V_{GS}$ = -0V to 15V | | 75 | | nC |
| Gate-drain charge | $Q_{GD}$ | | | 13 | | |
| Gate-source charge | $Q_{GS}$ | | | 22 | | |
| Turn-on delay time | $t_{d(on)}$ | Notes 4 and 5, $V_{DS}$=400V, $I_D$=60A, Gate Driver =0V to +15V, Turn-on $R_{G,EXT}$=1Ω, Turn-off $R_{G,EXT}$=5Ω, inductive Load, FWD: same device with $V_{GS}$ = 0V and $R_G$ = 5Ω, RC snubber: $R_S$=5Ω and $C_S$=440pF, $T_J$=25°C | | 17.6 | | ns |
| Rise time | $t_r$ | | | 22.4 | | |
| Turn-off delay time | $t_{d(off)}$ | | | 65 | | |
| Fall time | $t_f$ | | | 12.8 | | |
| Turn-on energy including $R_S$ energy | $E_{ON}$ | | | 173 | | µJ |
| Turn-off energy including $R_S$ energy | $E_{OFF}$ | | | 132 | | |
| Total switching energy | $E_{TOTAL}$ | | | 305 | | |
| Snubber $R_S$ energy during turn-on | $E_{RS\_ON}$ | | | 11 | | |
| Snubber $R_S$ energy during turn-off | $E_{RS\_OFF}$ | | | 37 | | |
| Turn-on delay time | $t_{d(on)}$ | Notes 4 and 5, $V_{DS}$=400V, $I_D$=60A, Gate Driver =0V to +15V, Turn-on $R_{G,EXT}$=1Ω, Turn-off $R_{G,EXT}$=5Ω, inductive Load, FWD: same device with $V_{GS}$ = 0V and $R_G$ = 5Ω, RC snubber: $R_S$=5Ω and $C_S$=440pF, $T_J$=150°C | | 18 | | ns |
| Rise time | $t_r$ | | | 25 | | |
| Turn-off delay time | $t_{d(off)}$ | | | 68 | | |
| Fall time | $t_f$ | | | 13.6 | | |
| Turn-on energy including $R_S$ energy | $E_{ON}$ | | | 203 | | µJ |
| Turn-off energy including $R_S$ energy | $E_{OFF}$ | | | 145 | | |
| Total switching energy | $E_{TOTAL}$ | | | 348 | | |
| Snubber $R_S$ energy during turn-on | $E_{RS\_ON}$ | | | 11 | | |
| Snubber $R_S$ energy during turn-off | $E_{RS\_OFF}$ | | | 37 | | |

4. Measured with the switching test circuit in Figure 26.

5. In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.

## Typical Performance Diagrams

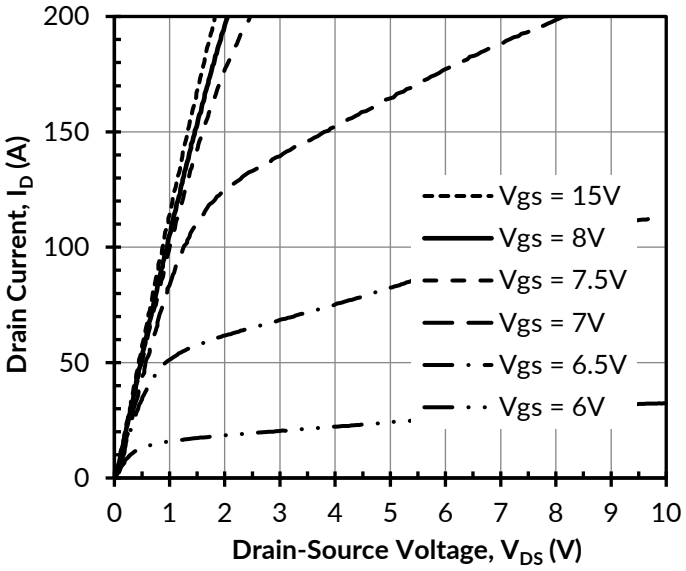



Figure 1. Typical output characteristics at $T_J$ = - 55°C, tp < 250µs

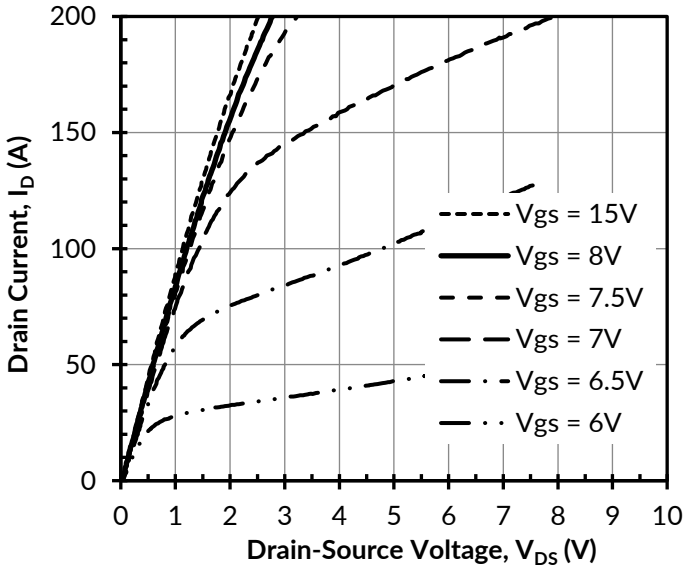



Figure 2. Typical output characteristics at $T_J$ = 25°C, tp < 250µs

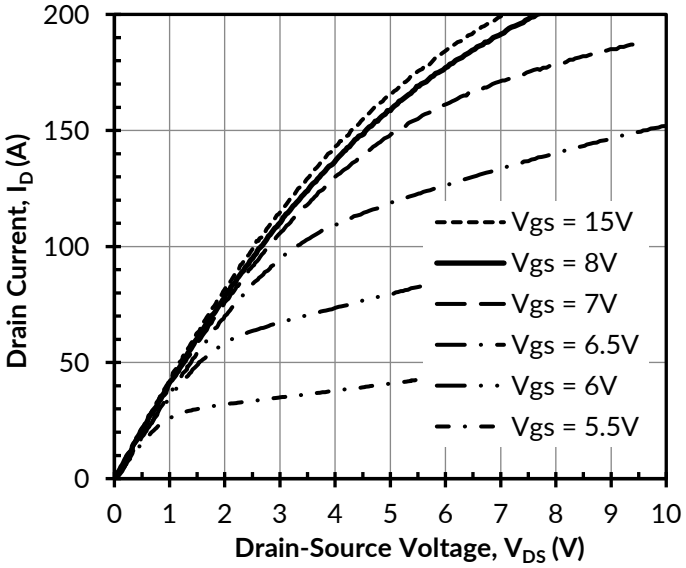



Figure 3. Typical output characteristics at $T_J$ = 175°C, tp < 250µs

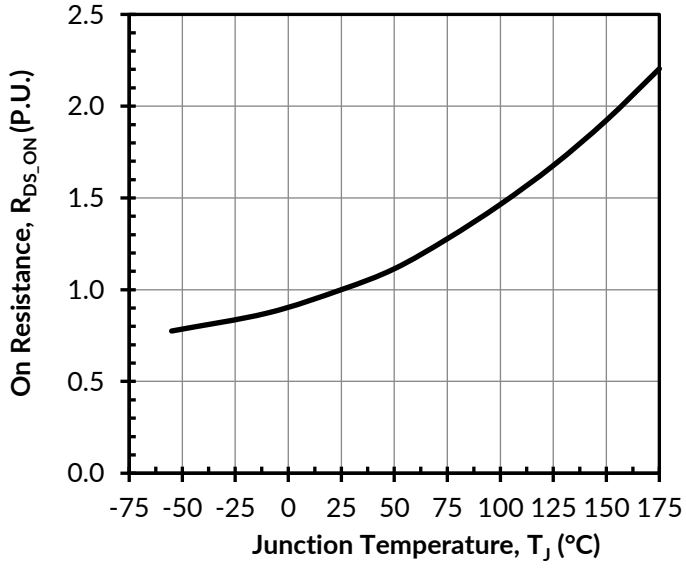



Figure 4. Normalized on-resistance vs. temperature at $V_{GS}$ = 12V and $I_D$ = 60A

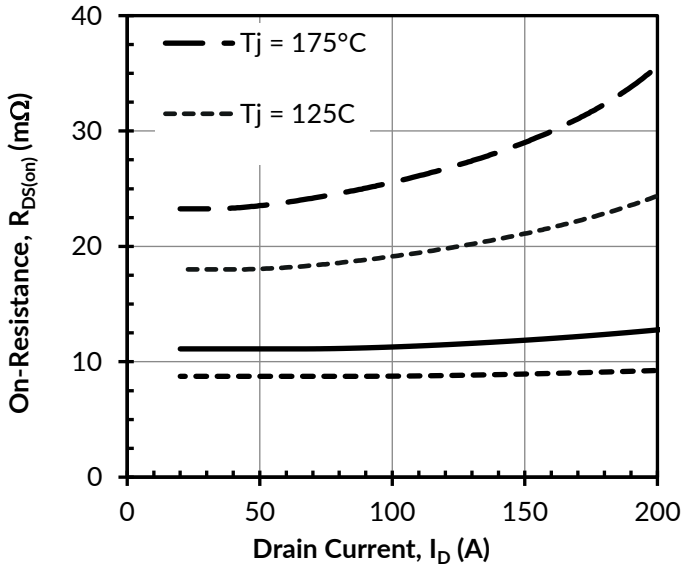



Figure 5. Typical drain-source on-resistances at $V_{GS}$ = 12V

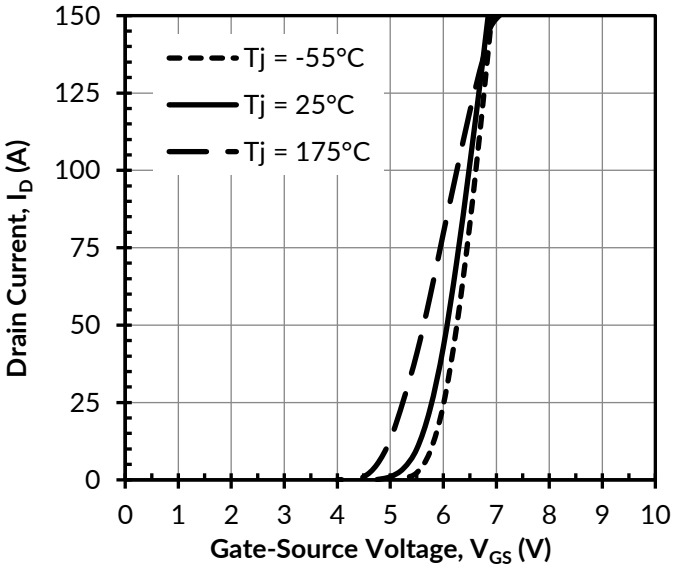



Figure 6. Typical transfer characteristics at $V_{DS}$ = 5V

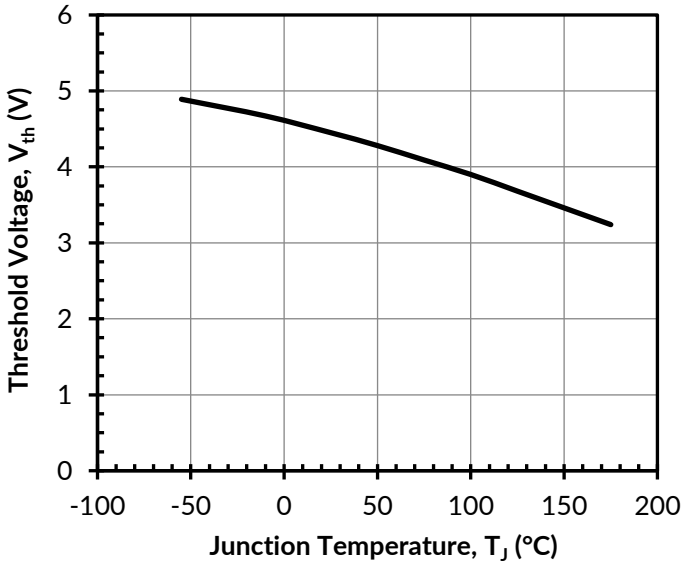



Figure 7. Threshold voltage vs. junction temperature at $V_{DS}$ = 5V and $I_D$ = 10mA

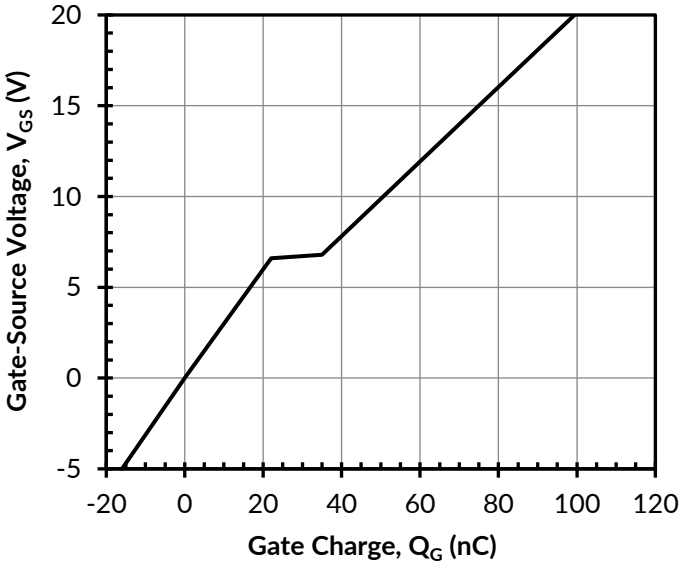



Figure 8. Typical gate charge at $I_D$ = 60A

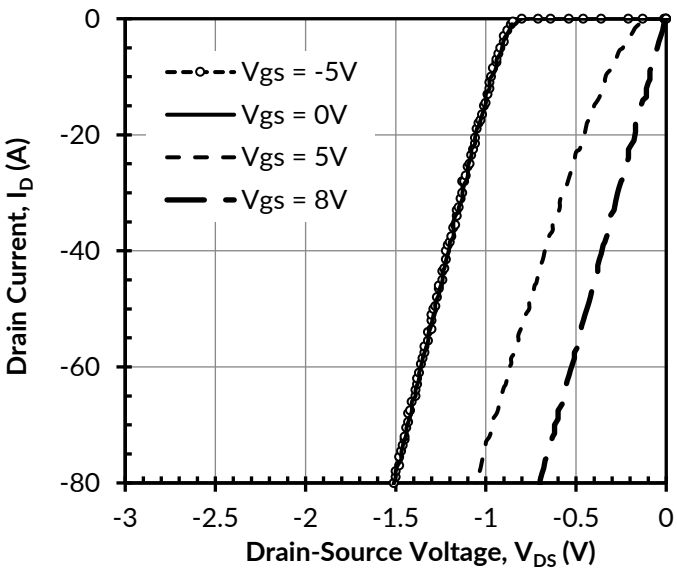



Figure 9. 3rd quadrant characteristics at $T_J$ = -55°C

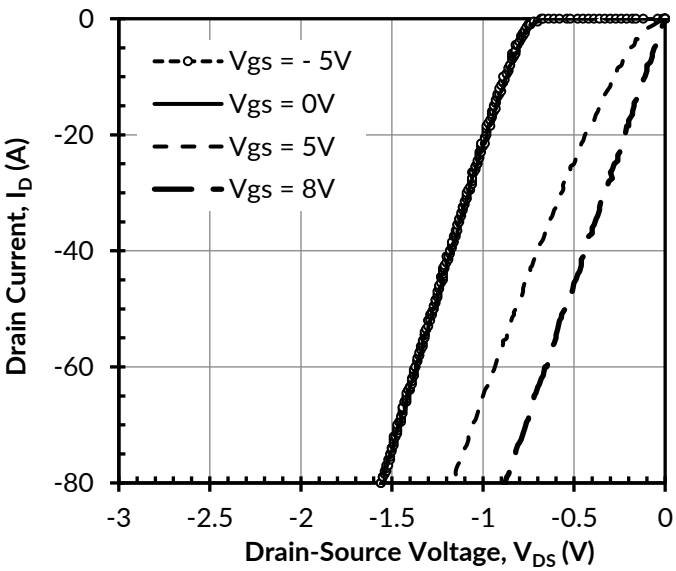



Figure 10. 3rd quadrant characteristics at $T_J$ = 25°C

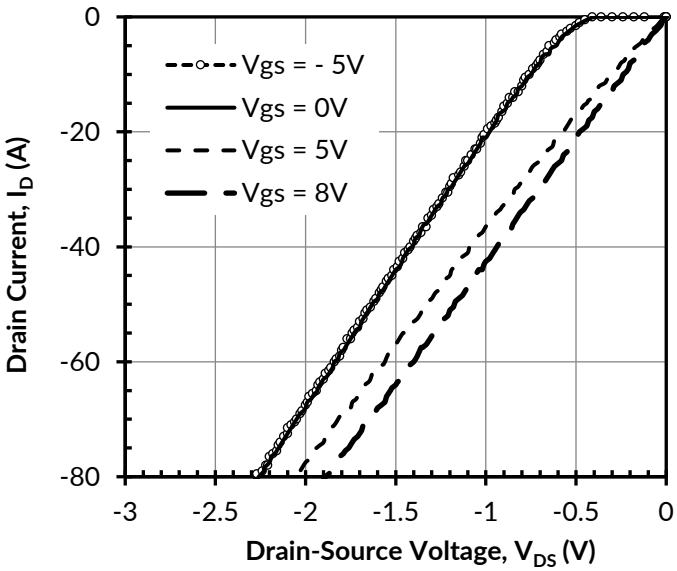



Figure 11. 3rd quadrant characteristics at $T_J$ = 175°C

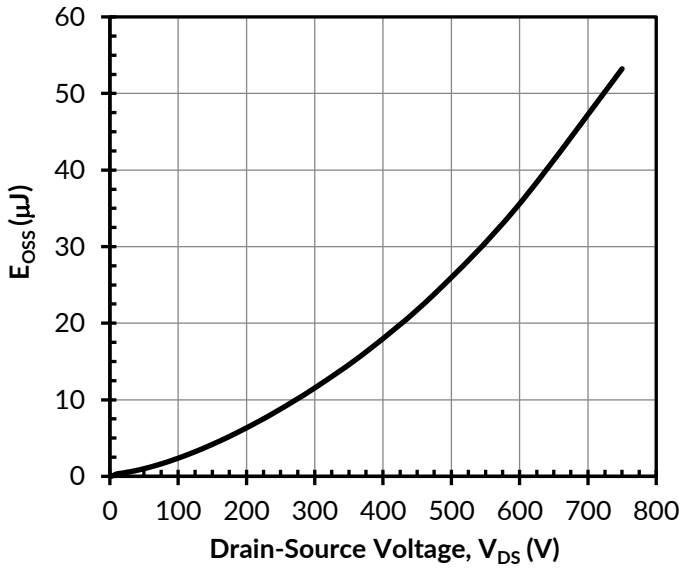



Figure 12. Typical stored energy in $C_{OSS}$ at $V_{GS}$ = 0V

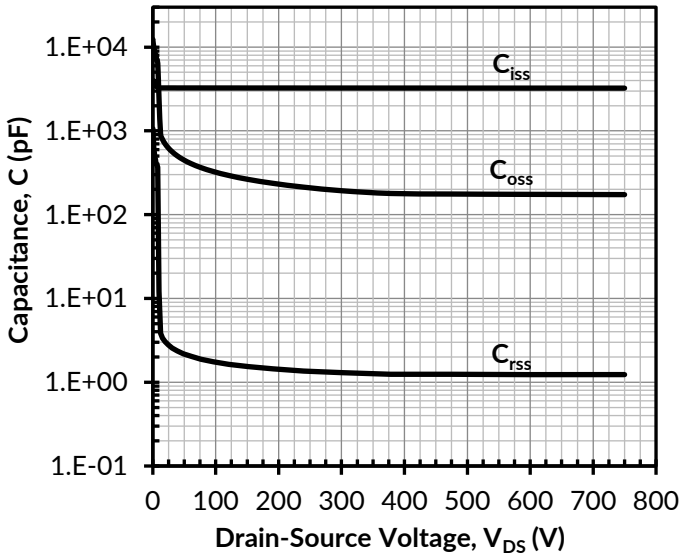



Figure 13. Typical capacitances at f = 100kHz and $V_{GS}$ = 0V

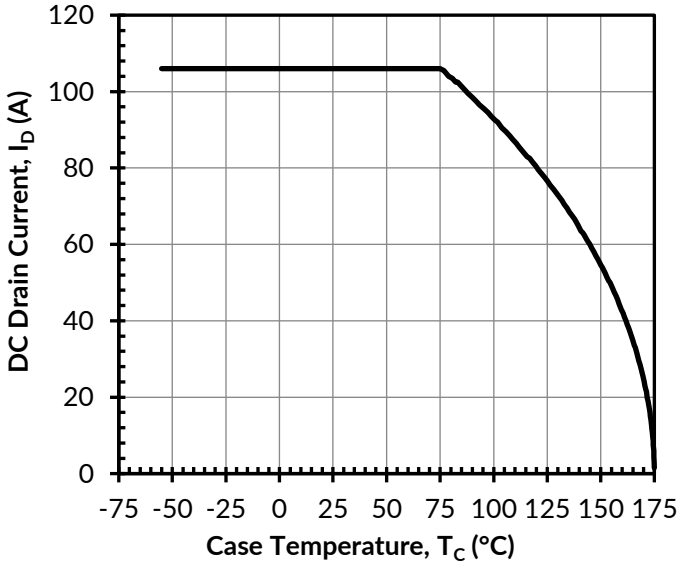



Figure 14. DC drain current derating

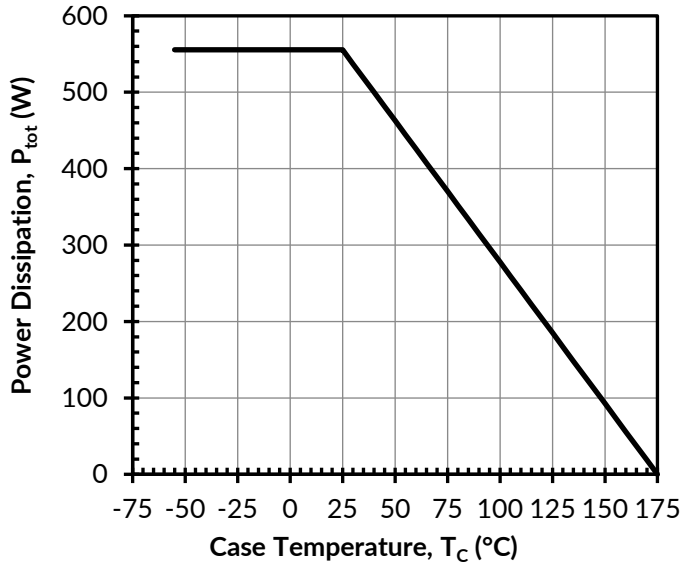



Figure 15. Total power dissipation

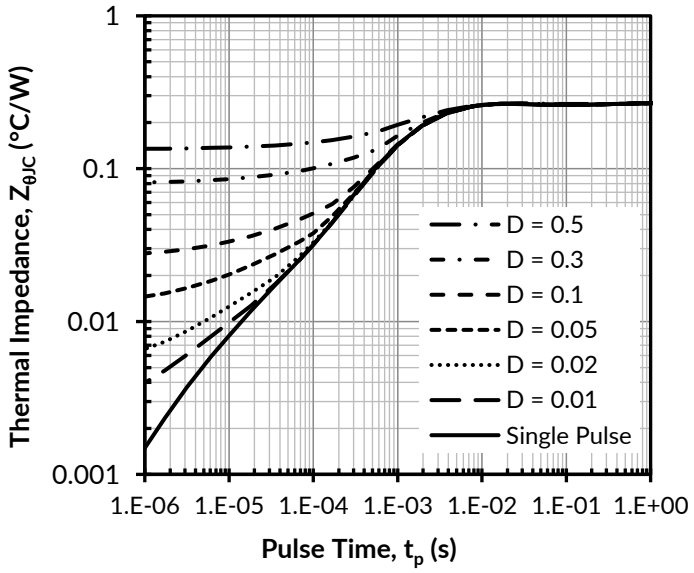



Figure 16. Maximum transient thermal impedance

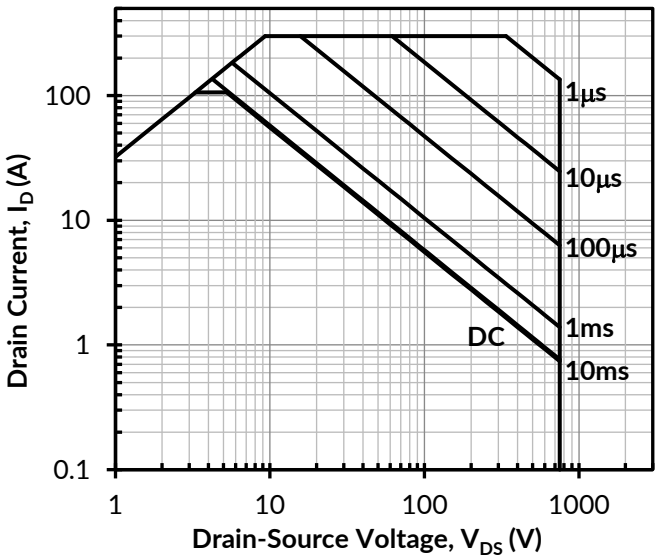



Figure 17. Safe operation area at $T_C$ = 25°C, D = 0, Parameter $t_p$

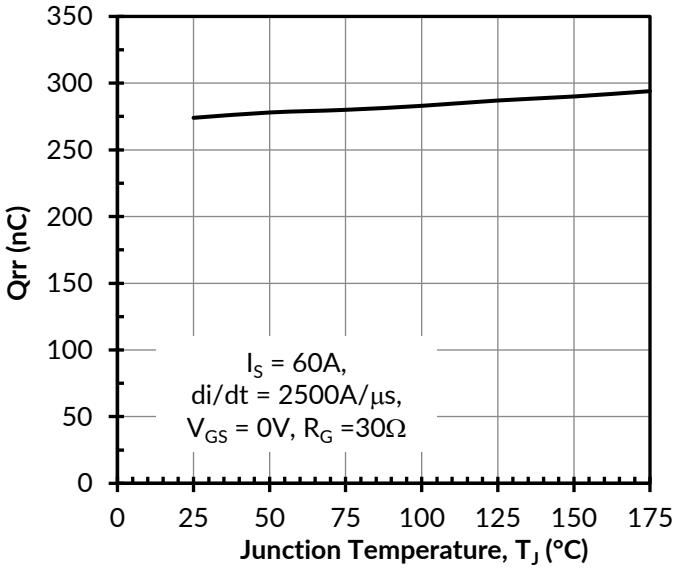



Figure 18. Reverse recovery charge Qrr vs. junction temperature at $V_{DS}$ = 400V

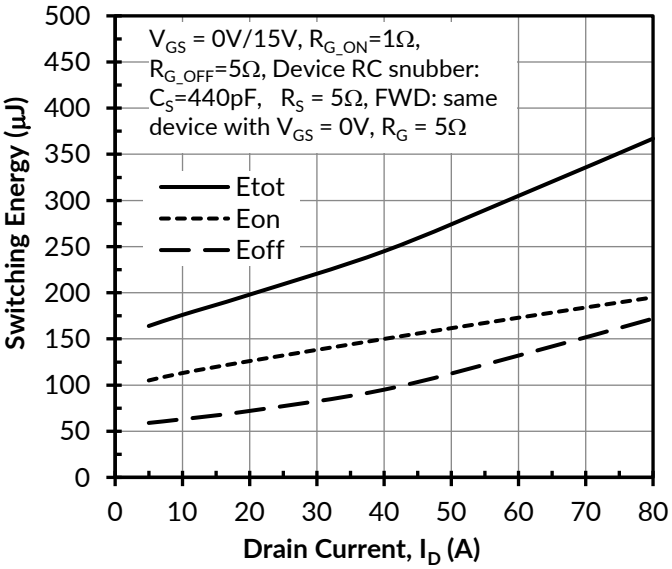



Figure 19. Clamped inductive switching energy vs. drain current at $V_{DS}$ = 400V and $T_J$ = 25°C

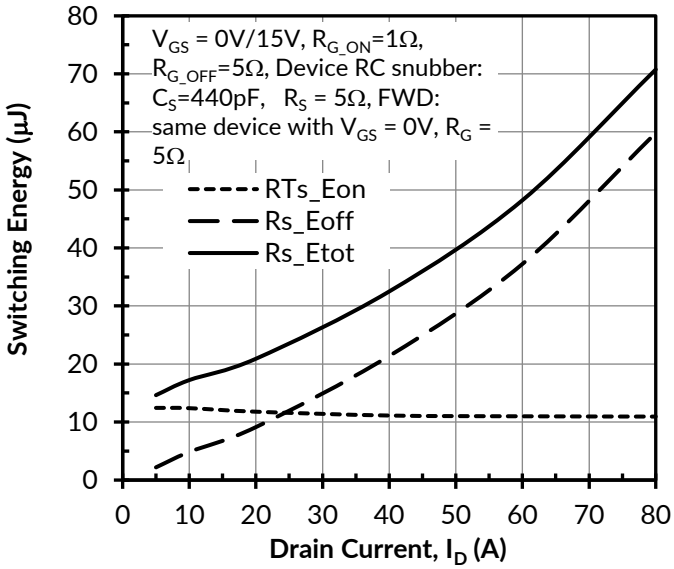



Figure 20. RC snubber energy loss vs. drain current at $V_{DS}$ = 400V and $T_J$ = 25°C

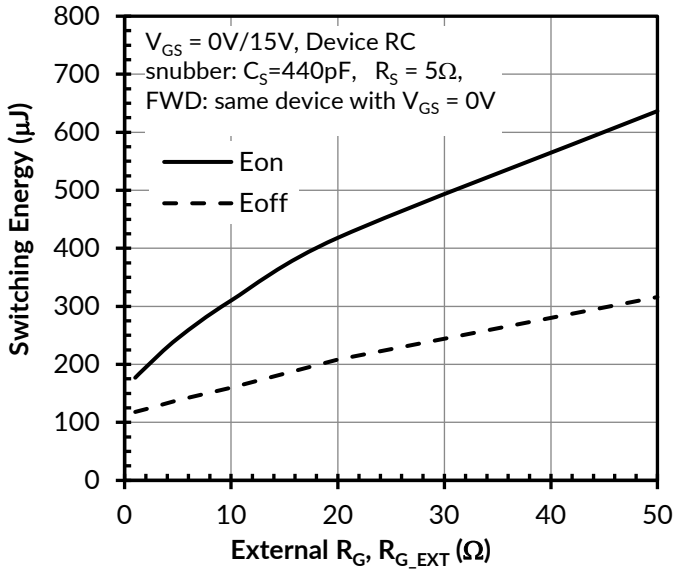



Figure 21. Clamped inductive switching energy vs. $R_{G,EXT}$ at $V_{DS}$ = 400V, $I_D$ = 60A, and $T_J$ = 25°C

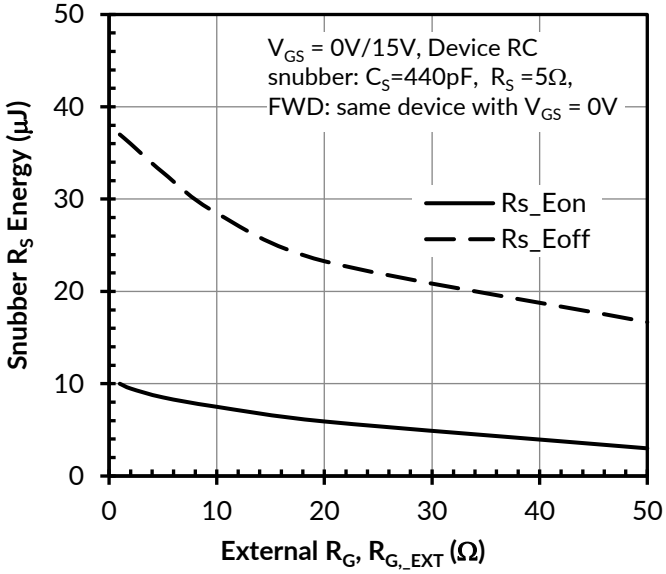



Figure 22. RC snubber energy losses vs. $R_{G,EXT}$ at $V_{DS}$ = 400V, $I_D$ = 60A, and $T_J$ = 25°C

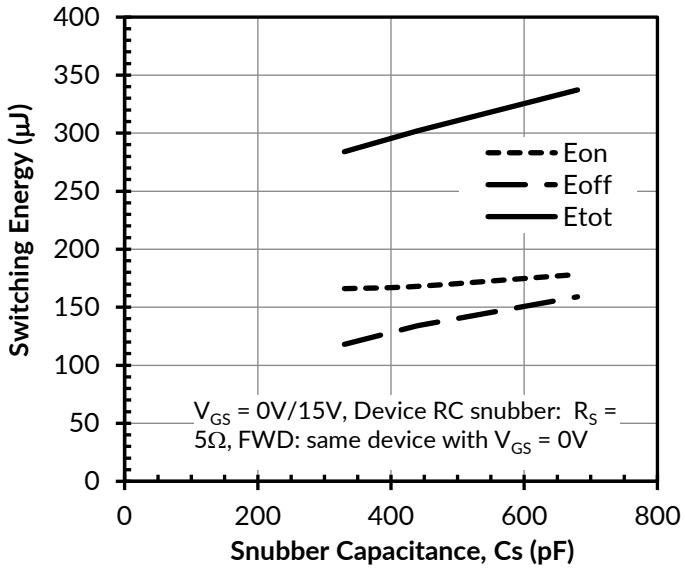



Figure 23. Clamped inductive switching energy vs. Snubber Capacitance Cs at $V_{DS}$ = 400V, $I_D$ = 60A, and $T_J$ = 25°C

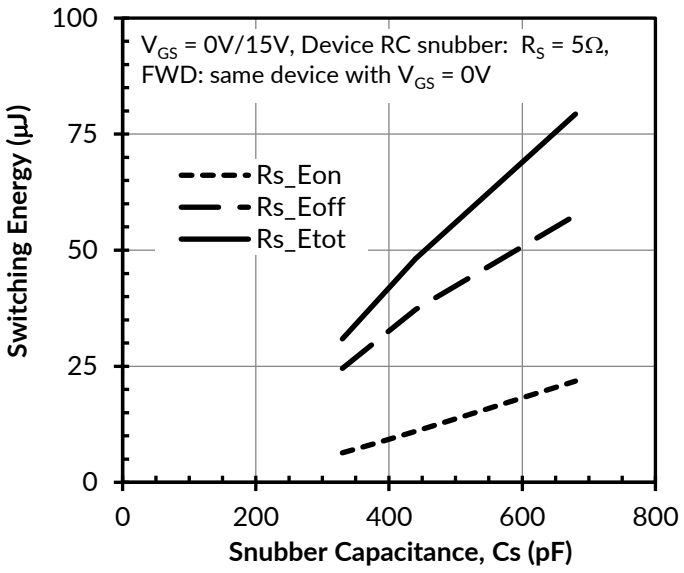



Figure 24. RC snubber energy loss vs. Snubber Capacitance Cs at $V_{DS}$ = 400V, $I_D$ = 60A, and $T_J$ = 25°C

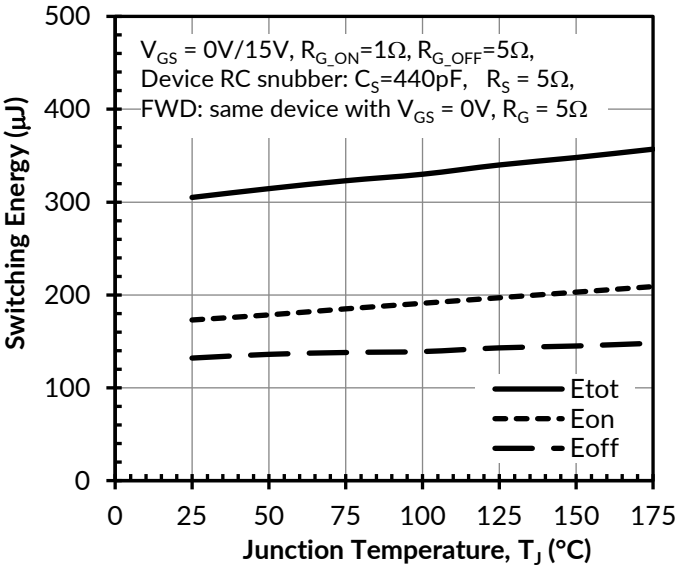



Figure 25. Clamped inductive switching energies vs. junction temperature $T_J$ at $V_{DS}$ = 400V, and $I_D$ = 60A

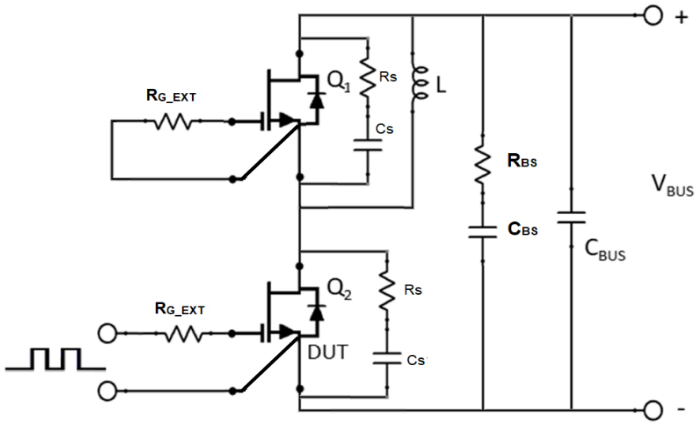
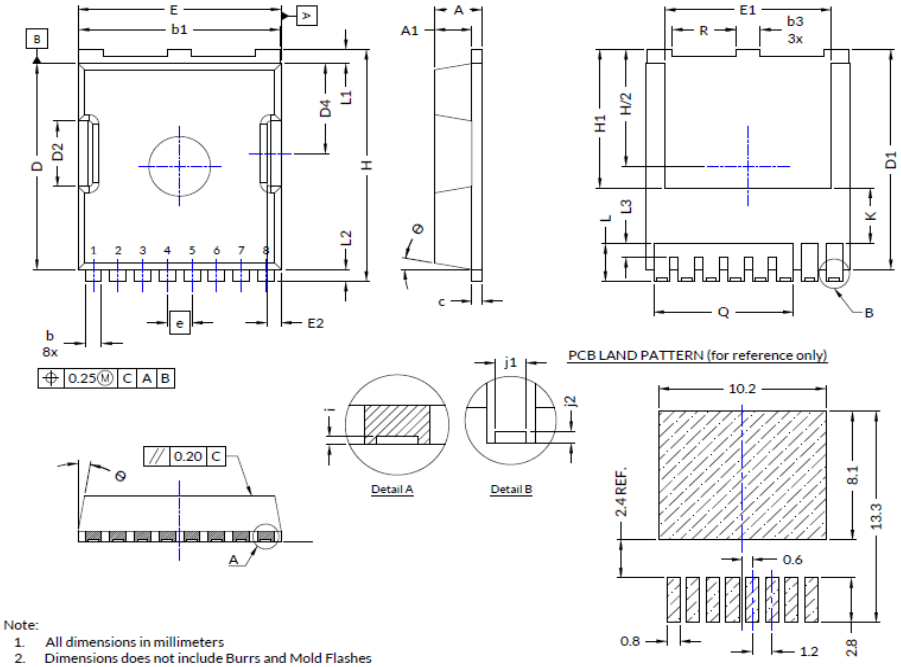



Figure 26. Schematic of the half-bridge mode switching test circuit. Note, device snubber (Rs =5Ω, Cs = 440pF) and bus RC snubber ($R_{BS}$ = 1Ω, $C_{BS}$=100nF) is used to reduce the power loop high frequency oscillations.

## Package Outlines




| TO-LL | | | |
|---|---|---|---|
| SYMBOL | Value | | |
| | Min | Nom | Max |
| A | 2.15 | 2.30 | 2.45 |
| A1 | | 1.80 REF | |
| b | 0.70 | 0.80 | 0.90 |
| b1 | 9.65 | 9.80 | 9.95 |
| b3 | 1.10 | 1.20 | 1.30 |
| c | 0.40 | 0.50 | 0.60 |
| D | 10.18 | 10.38 | 10.58 |
| D1 | 10.98 | 11.08 | 11.18 |
| D2 | 3.15 | 3.30 | 3.45 |
| D4 | 4.40 | 4.55 | 4.70 |
| E | 9.70 | 9.90 | 10.10 |
| E1 | 7.95 | 8.10 | 8.25 |
| E2 | 0.60 | 0.70 | 0.80 |
| e | | 1.20 BSC | |
| H | 11.48 | 11.68 | 11.88 |
| H1 | 6.80 | 6.95 | 7.10 |
| i | | 0.10 REF | |
| j1 | | 0.46 REF | |
| j2 | | 0.20 REF | |
| K | | 2.80 REF | |
| L | 1.40 | 1.90 | 2.10 |
| L1 | 0.50 | 0.70 | 0.90 |
| L2 | 0.48 | 0.60 | 0.72 |
| L3 | 0.30 | 0.70 | 0.80 |
| Q | | 6.80 REF | |
| R | 3.00 | 3.10 | 3.20 |
| θ | | 10° | |

Note:
1. All dimensions in millimeters
2. Dimensions does not include Burrs and Mold Flashes
3. Dimensions in compliance with JEDEC MO-299B except for backside heatsink exposed pad dimension, E1 and H1

Pin Designations:
1 : Gate
2 : Source Kelvin
3-8 : Source

## Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance ($C_{oss}$), gate charge ($Q_G$), and reverse recovery charge ($Q_{rr}$) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, seehttps://www.qorvo.com/design-hub.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at https://www.qorvo.com/design-hub.

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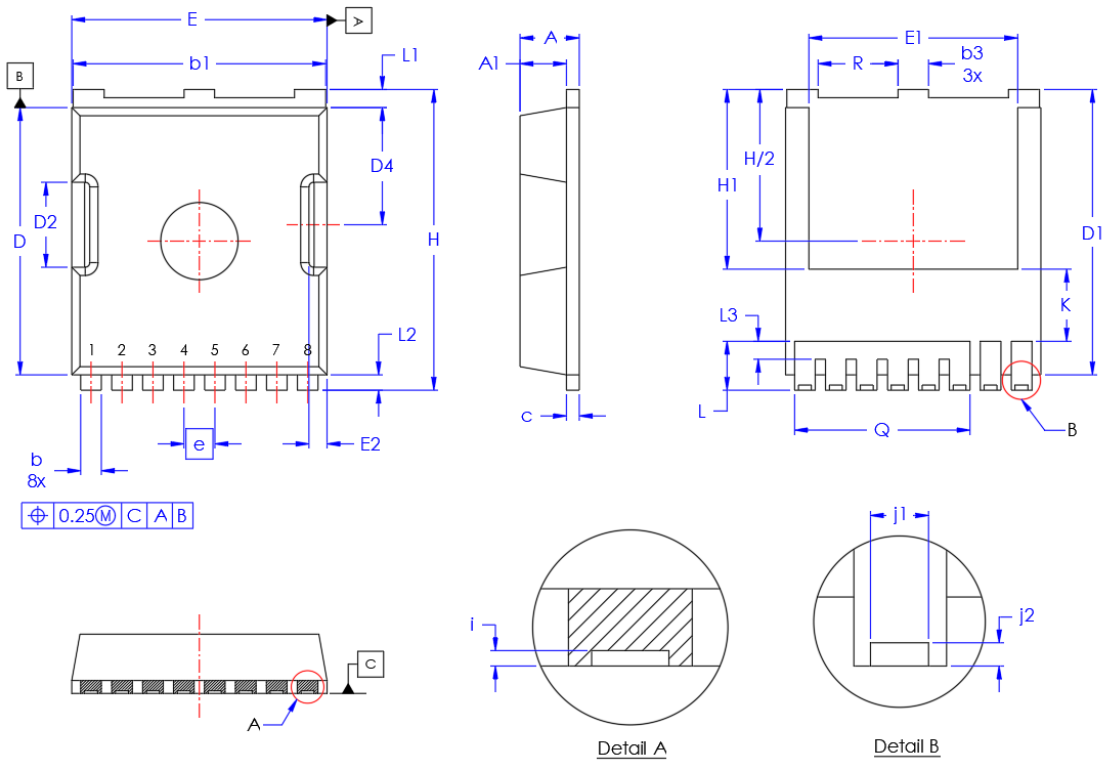
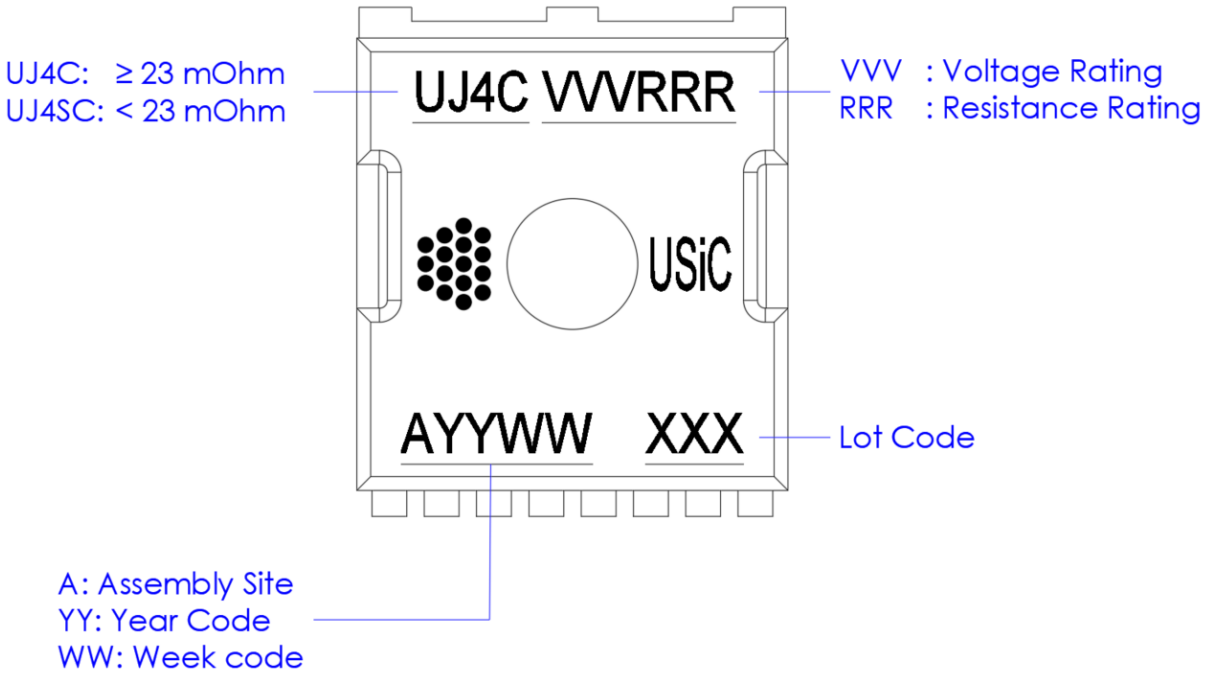
## PACKAGE OUTLINE




| SYMBOL | TO-LL Value | |
|---|---|---|
| | Min | Max |
| A | 2.15 | 2.45 |
| A1 | 1.80 REF | |
| b | 0.65 | 0.90 |
| b1 | 9.65 | 9.95 |
| b3 | 1.10 | 1.30 |
| c | 0.40 | 0.60 |
| D | 10.18 | 10.58 |
| D1 | 10.88 | 11.28 |
| D2 | 3.15 | 3.45 |
| D4 | 4.40 | 4.70 |
| E | 9.70 | 10.10 |
| E1 | 7.95 | 8.25 |
| E2 | 0.60 | 0.80 |
| e | 1.20 BSC | |
| H | 11.48 | 11.88 |
| H1 | 6.80 | 7.10 |
| i | 0.10 REF | |
| j1 | 0.46 REF | |
| j2 | 0.20 REF | |
| K | 2.80 REF | |
| L | 1.40 | 2.10 |
| L1 | 0.50 | 0.90 |
| L2 | 0.48 | 0.72 |
| L3 | 0.30 | 0.80 |
| Q | 6.80 REF | |
| R | 3.00 | 3.20 |

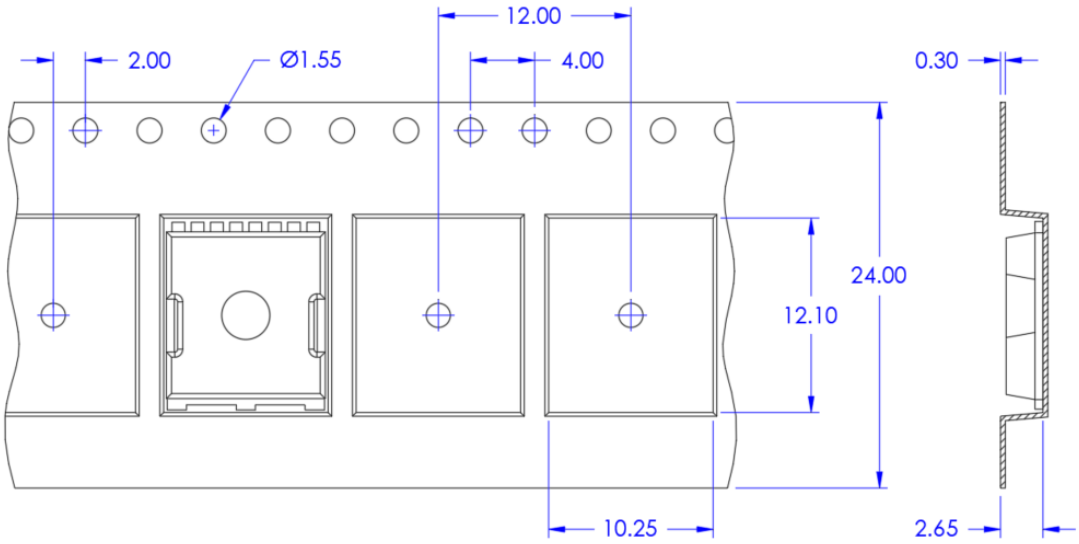
Note:
1. All dimensions in millimeters
2. Dimensions does not include Burrs and Mold Flashes

**PART MARKING**

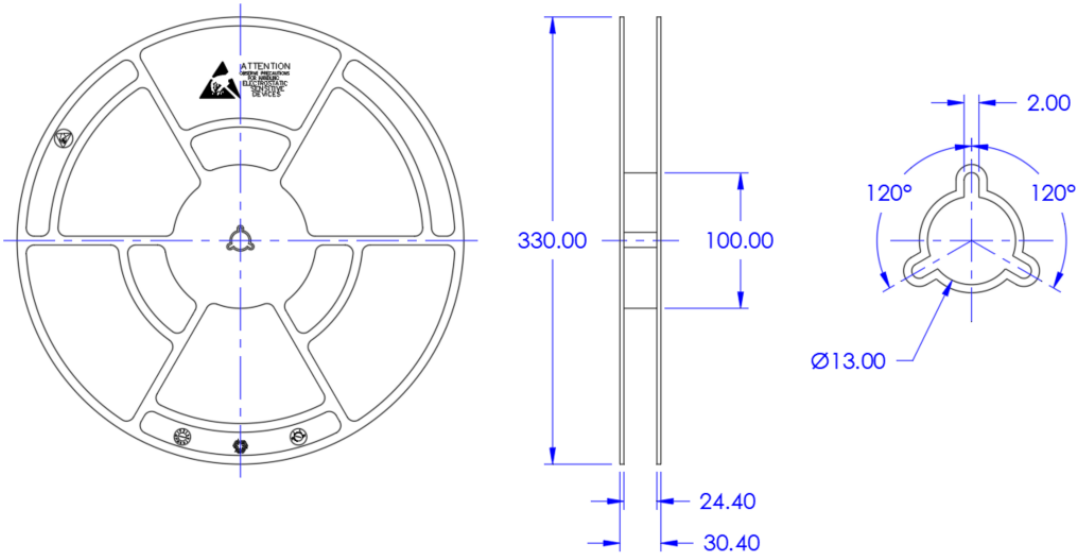


**PACKING TYPE**

*Carrier Tape*




*Reel*




All dimensions in millimeters
Quantity per Reel: 2000 units

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**REVISION HISTORY**

| Revision | Create Date (mm/dd/yyyy) | Description of Change | Initiator of Change |
|---|---|---|---|
| A | 10/13/2023 | Initial Production Release | Glenn Galang |
| B | 01/31/2024 | Corrected device orientation inside carrier tape pocket (Page 3) | Glenn Galang |
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## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
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