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## SiC JFET Division

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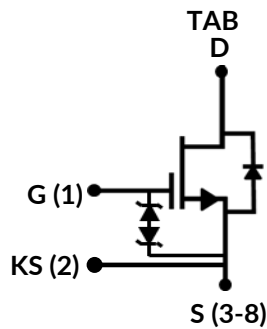
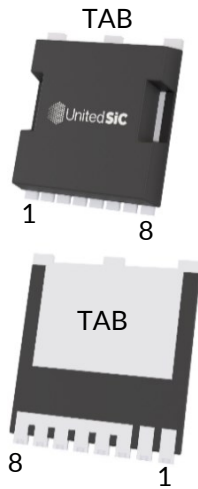
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DATASHEET

# UJ4C075023L8S



## Silicon Carbide (SiC) Cascode JFET - EliteSiC, Power N-Channel, TOLL, 750 V, 23 mohm

Rev. D, January 2025

### Description

The UJ4C075023L8S is a 750V, 23mΩ G4 SiC FET. It is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows use of off-the-shelf gate drivers hence requiring minimal re-design when replacing to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TOLL (MO-229) package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

### Features

- On-resistance  $R_{DS(on)}$ : 23mΩ (typ)
- Operating temperature: 175°C (max)
- Excellent reverse recovery:  $Q_{rr} = 122\text{nC}$
- Low body diode  $V_{FSD}$ : 1.23V
- Low gate charge:  $Q_G = 37.8\text{nC}$
- Threshold voltage  $V_{G(th)}$ : 4.8V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected: HBM class 2 and CDM class C3
- TOLL package for faster switching, clean gate waveforms

### Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Part Number	Package	Marking
UJ4C075023L8S	MO-229	UJ4C075023



## Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	$V_{DS}$		750	V
Gate-source voltage	$V_{GS}$	DC	-20 to +20	V
		AC ( $f > 1\text{Hz}$ )	-25 to +25	V
Continuous drain current <sup>1</sup>	$I_D$	$T_C = 25^\circ\text{C}$	64	A
		$T_C = 100^\circ\text{C}$	46	A
Pulsed drain current <sup>2</sup>	$I_{DM}$	$T_C = 25^\circ\text{C}$	196	A
Single pulsed avalanche energy <sup>3</sup>	$E_{AS}$	$L=15\text{mH}, I_{AS}=3\text{A}$	67	mJ
SiC FET dv/dt ruggedness	dv/dt	$V_{DS} [ 500\text{V}$	150	V/ns
Power dissipation	$P_{tot}$	$T_C = 25^\circ\text{C}$	278	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	$T_J, T_{STG}$		-55 to 175	$^\circ\text{C}$
Reflow soldering temperature	$T_{solder}$	reflow MSL 1	260	$^\circ\text{C}$

1. Limited by  $T_{J,max}$

2. Pulse width  $t_p$  limited by  $T_{J,max}$

3. Starting  $T_J = 25^\circ\text{C}$

## Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.42	0.54	$^\circ\text{C}/\text{W}$

## Electrical Characteristics ( $T_J = +25^\circ\text{C}$ unless otherwise specified)

### Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	$BV_{DS}$	$V_{GS}=0V, I_D=1mA$	750			V
Total drain leakage current	$I_{DSS}$	$V_{DS}=750V, V_{GS}=0V, T_J=25^\circ\text{C}$		2	30	$\mu\text{A}$
		$V_{DS}=750V, V_{GS}=0V, T_J=175^\circ\text{C}$		15		
Total gate leakage current	$I_{GSS}$	$V_{DS}=0V, T_J=25^\circ\text{C}, V_{GS}=-20V / +20V$		6	$\pm 20$	$\mu\text{A}$
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=12V, I_D=40A, T_J=25^\circ\text{C}$		23	29	$\text{m}\Omega$
		$V_{GS}=12V, I_D=40A, T_J=125^\circ\text{C}$		39		
		$V_{GS}=12V, I_D=40A, T_J=175^\circ\text{C}$		50		
Gate threshold voltage	$V_{G(th)}$	$V_{DS}=5V, I_D=10mA$	4	4.8	6	V
Gate resistance	$R_G$	$f=1\text{MHz}, \text{open drain}$		4.5		$\Omega$

### Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current <sup>1</sup>	$I_S$	$T_C = 25^\circ\text{C}$			64	A
Diode pulse current <sup>2</sup>	$I_{S,pulse}$	$T_C = 25^\circ\text{C}$			196	A
Forward voltage	$V_{FSD}$	$V_{GS}=0V, I_S=20A, T_J=25^\circ\text{C}$		1.23	1.39	V
		$V_{GS}=0V, I_S=20A, T_J=175^\circ\text{C}$		1.45		
Reverse recovery charge	$Q_{rr}$	$V_{DS}=400V, I_S=40A, V_{GS}=0V, R_G=50\Omega$		122		nC
Reverse recovery time	$t_{rr}$	$di/dt=1200A/\mu\text{s}, T_J=25^\circ\text{C}$		26.4		ns
Reverse recovery charge	$Q_{rr}$	$V_{DS}=400V, I_S=40A, V_{GS}=0V, R_G=50\Omega$		132		nC
Reverse recovery time	$t_{rr}$	$dt=1200A/\mu\text{s}, T_J=150^\circ\text{C}$		27.2		ns

## Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	$C_{iss}$	$V_{DS}=400V, V_{GS}=0V$ $f=100kHz$		1400		pF
Output capacitance	$C_{oss}$			93		
Reverse transfer capacitance	$C_{rss}$			2.5		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		116		pF
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		232		pF
$C_{OSS}$ stored energy	$E_{oss}$	$V_{DS}=400V, V_{GS}=0V$		9.3		$\mu J$
Total gate charge	$Q_G$	$V_{DS}=400V, I_D=40A,$ $V_{GS} = 0V$ to 15V		37.8		nC
Gate-drain charge	$Q_{GD}$			8		
Gate-source charge	$Q_{GS}$			11.8		
Turn-on delay time	$t_{d(on)}$	Notes 4, $V_{DS}=400V, I_D=40A,$ Gate Driver =0V to +15V,		11		ns
Rise time	$t_r$	Turn-on $R_{G,EXT}=1\Omega,$		25		
Turn-off delay time	$t_{d(off)}$	Turn-off $R_{G,EXT}=50\Omega,$		136		
Fall time	$t_f$	inductive Load, FWD:		13		
Turn-on energy	$E_{ON}$	same device with $V_{GS} = 0V$ and $R_G = 50\Omega,$ $T_J=25^\circ C$		244		$\mu J$
Turn-off energy	$E_{OFF}$			122		
Total switching energy	$E_{TOTAL}$			366		
Turn-on delay time	$t_{d(on)}$	Notes 4, $V_{DS}=400V, I_D=40A,$ Gate Driver =0V to +15V,		11		ns
Rise time	$t_r$	Turn-on $R_{G,EXT}=1\Omega,$		26		
Turn-off delay time	$t_{d(off)}$	Turn-off $R_{G,EXT}=50\Omega,$		131		
Fall time	$t_f$	inductive Load, FWD:		14		
Turn-on energy	$E_{ON}$	same device with $V_{GS} = 0V$ and $R_G = 50\Omega,$ $T_J=150^\circ C$		262		$\mu J$
Turn-off energy	$E_{OFF}$			135		
Total switching energy	$E_{TOTAL}$			397		

4. Measured with the switching test circuit in Figure 23.

## Typical Performance - Dynamic (continued)

Parameter	Symbol	Test Conditions	Value			Units	
			Min	Typ	Max		
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6, $V_{DS}=400V$ , $I_D=40A$ , Gate Driver =0V to +15V, Turn-on $R_{G,EXT}=1\Omega$ , Turn-off $R_{G,EXT}=5\Omega$ , inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_G = 5\Omega$ , RC snubber: $R_S=10\Omega$ and $C_S=200pF$ , $T_J=25^\circ C$		12		ns	
Rise time	$t_r$			30			
Turn-off delay time	$t_{d(off)}$			36			
Fall time	$t_f$			10			
Turn-on energy including $R_S$ energy	$E_{ON}$				268		$\mu J$
Turn-off energy including $R_S$ energy	$E_{OFF}$				68		
Total switching energy	$E_{TOTAL}$				336		
Snubber $R_S$ energy during turn-on	$E_{RS\_ON}$				3		
Snubber $R_S$ energy during turn-off	$E_{RS\_OFF}$				5.9		
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6, $V_{DS}=400V$ , $I_D=40A$ , Gate Driver =0V to +15V, Turn-on $R_{G,EXT}=1\Omega$ , Turn-off $R_{G,EXT}=5\Omega$ , inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_G = 5\Omega$ , RC snubber: $R_S=10\Omega$ and $C_S=200pF$ , $T_J=150^\circ C$		12		ns	
Rise time	$t_r$			30			
Turn-off delay time	$t_{d(off)}$			36			
Fall time	$t_f$			10			
Turn-on energy including $R_S$ energy	$E_{ON}$				269		$\mu J$
Turn-off energy including $R_S$ energy	$E_{OFF}$				66		
Total switching energy	$E_{TOTAL}$				335		
Snubber $R_S$ energy during turn-on	$E_{RS\_ON}$				2.9		
Snubber $R_S$ energy during turn-off	$E_{RS\_OFF}$				5.7		

5. Measured with the switching test circuit in Figure 24.

6. In this table, the switching energies (turn-on energy, turn-off energy and total energy) presented include the device RC snubber energy losses.

## Typical Performance Diagrams

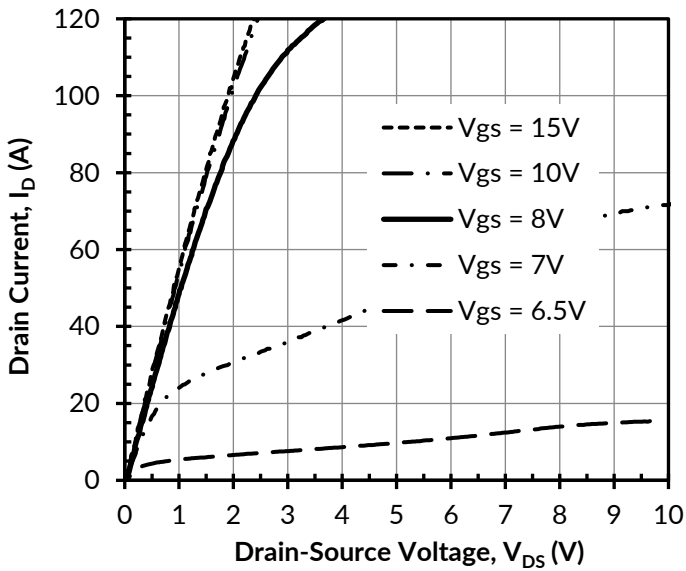


Figure 1. Typical output characteristics at  $T_j = -55^\circ\text{C}$ ,  $t_p < 250\mu\text{s}$

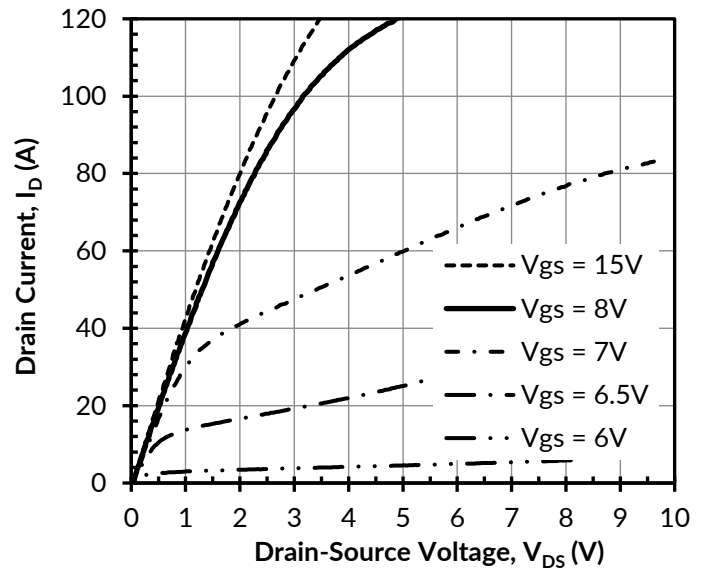


Figure 2. Typical output characteristics at  $T_j = 25^\circ\text{C}$ ,  $t_p < 250\mu\text{s}$

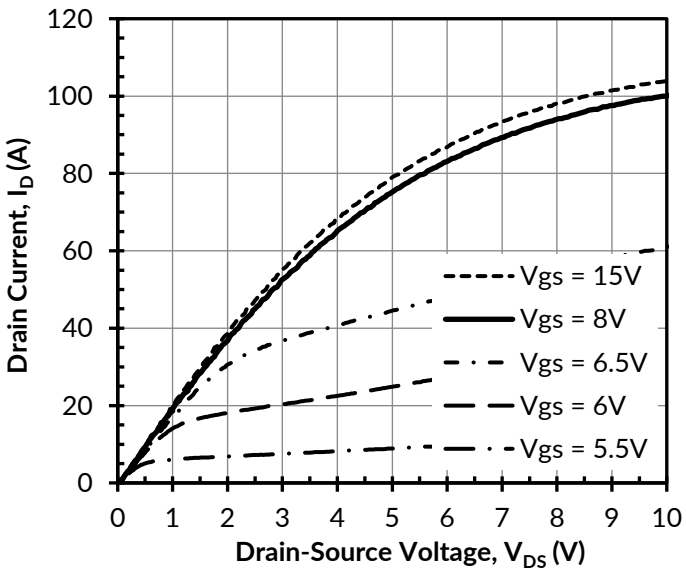


Figure 3. Typical output characteristics at  $T_j = 175^\circ\text{C}$ ,  $t_p < 250\mu\text{s}$

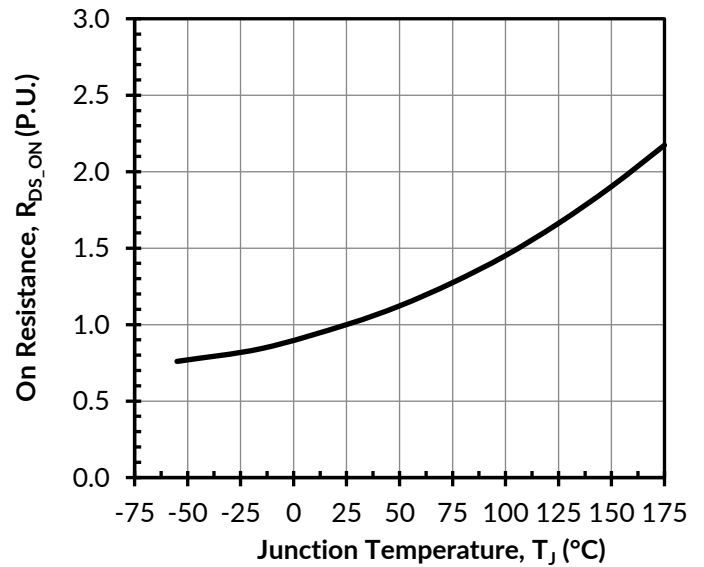


Figure 4. Normalized on-resistance vs. temperature at  $V_{GS} = 12\text{V}$

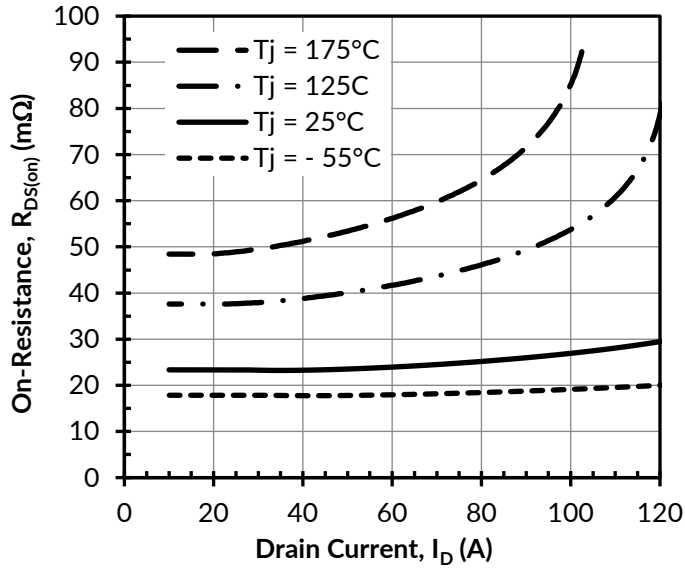


Figure 5. Typical drain-source on-resistances at  $V_{GS} = 12V$

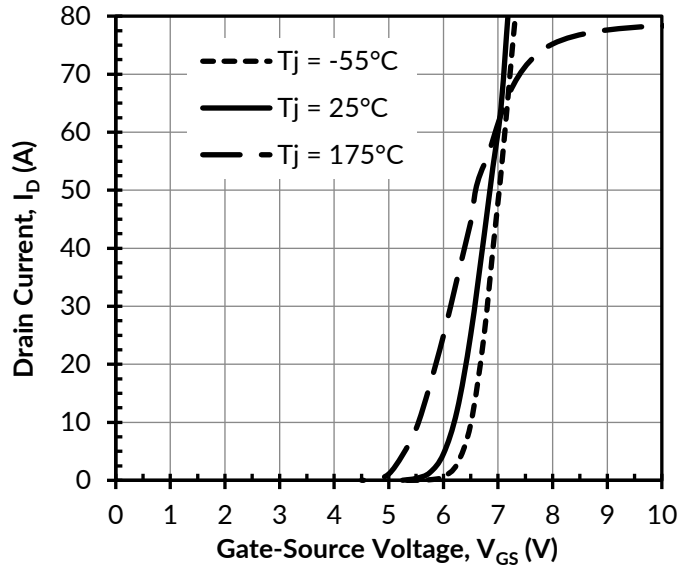


Figure 6. Typical transfer characteristics at  $V_{DS} = 5V$

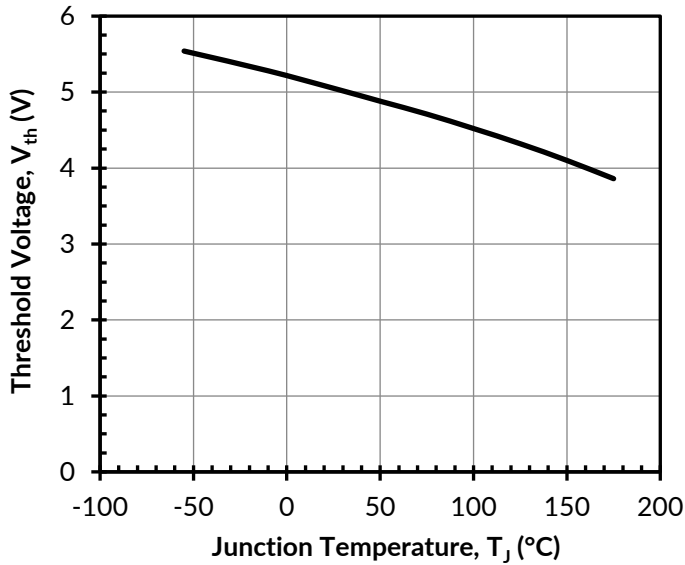


Figure 7. Threshold voltage vs. junction temperature at  $V_{DS} = 5V$  and  $I_D = 10mA$

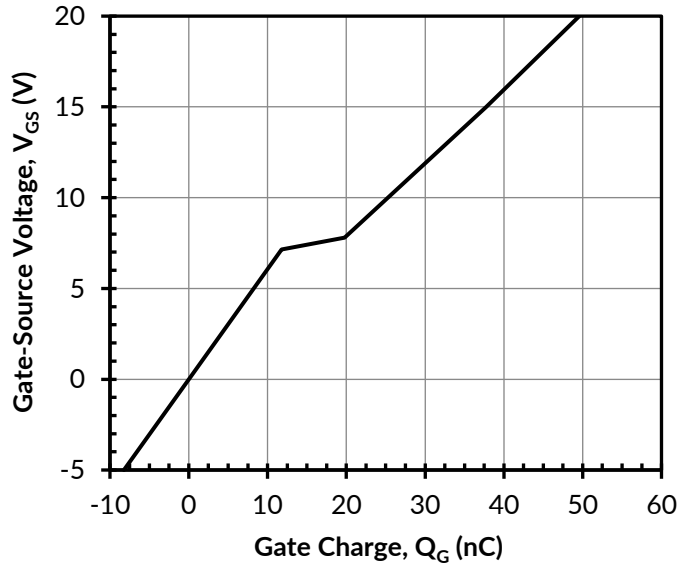


Figure 8. Typical gate charge at  $I_D = 40A$



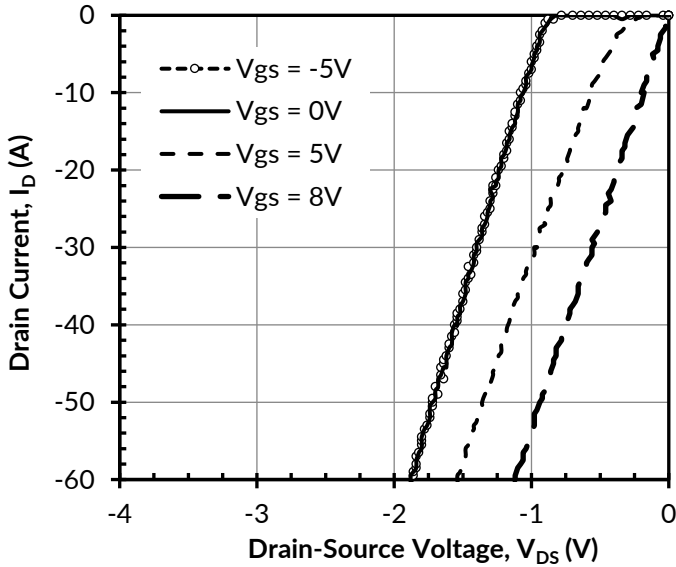


Figure 9. 3rd quadrant characteristics at  $T_j = -55^\circ\text{C}$

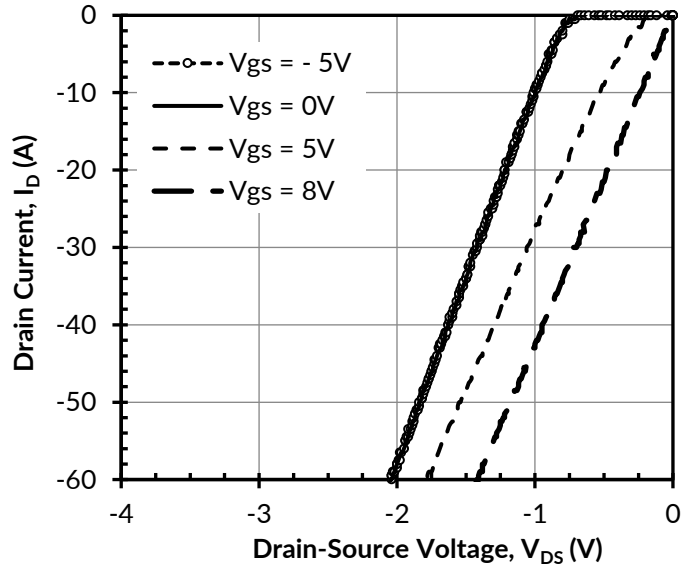


Figure 10. 3rd quadrant characteristics at  $T_j = 25^\circ\text{C}$

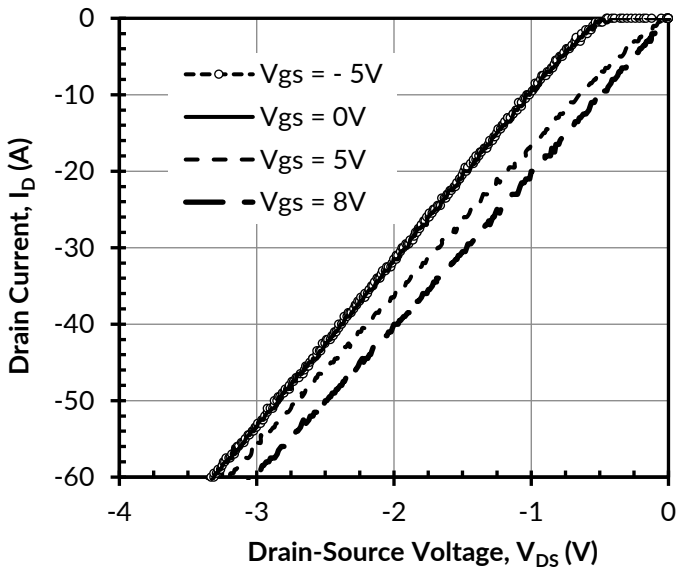


Figure 11. 3rd quadrant characteristics at  $T_j = 175^\circ\text{C}$

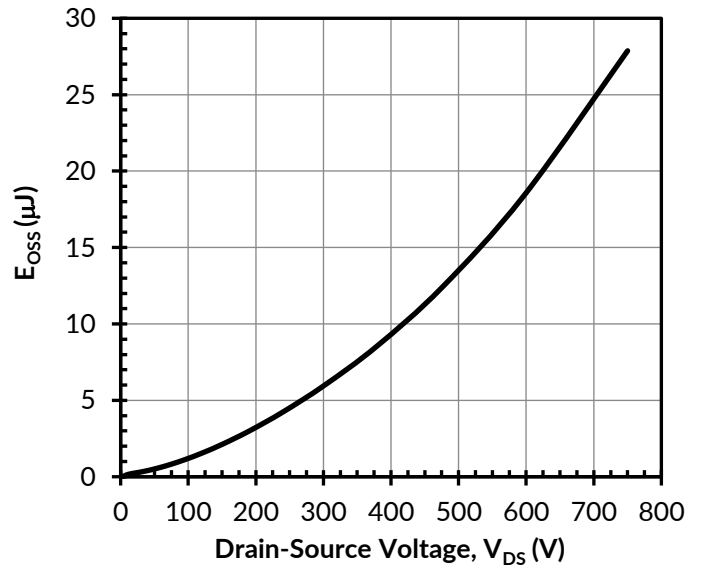


Figure 12. Typical stored energy in  $C_{OSS}$  at  $V_{GS} = 0\text{V}$

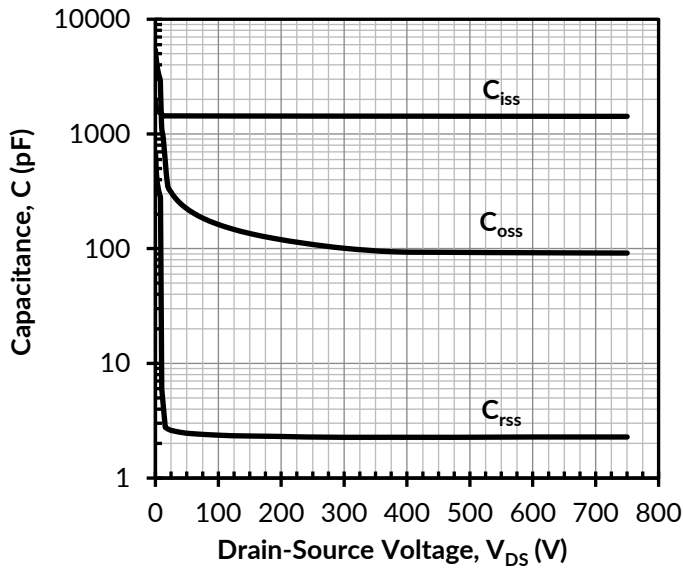


Figure 13. Typical capacitances at  $f = 100\text{kHz}$  and  $V_{GS} = 0\text{V}$

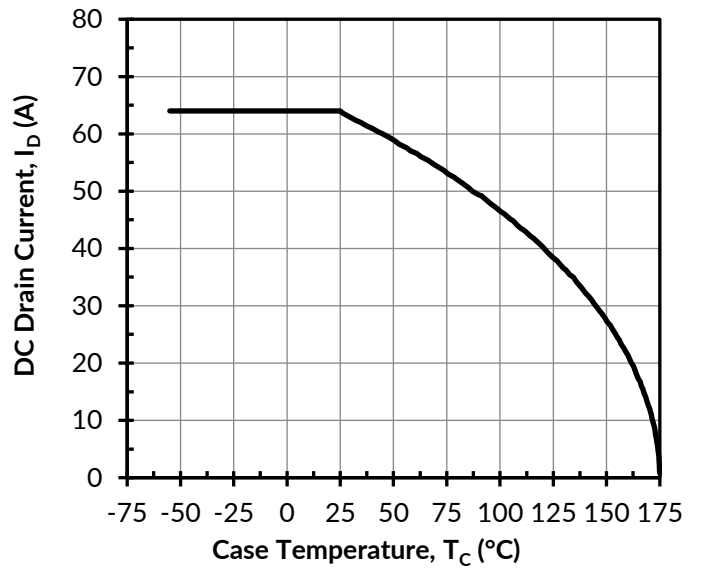


Figure 14. DC drain current derating

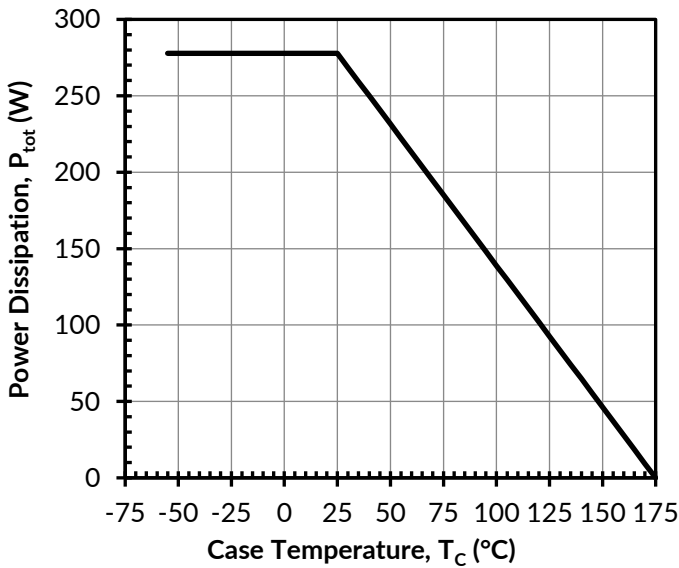


Figure 15. Total power dissipation

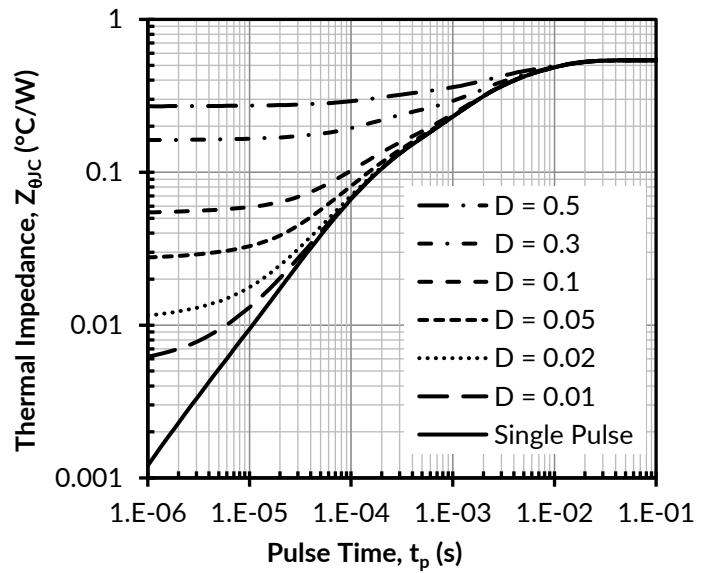


Figure 16. Maximum transient thermal impedance

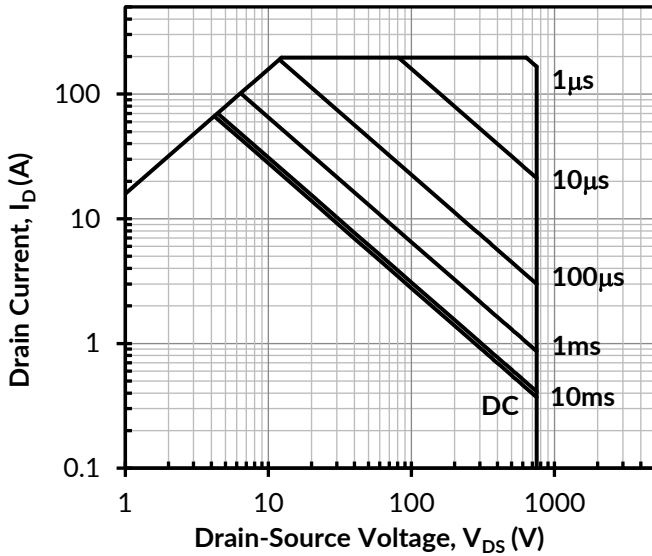


Figure 17. Safe operation area at  $T_C = 25^\circ\text{C}$ ,  $D = 0$ , Parameter  $t_p$

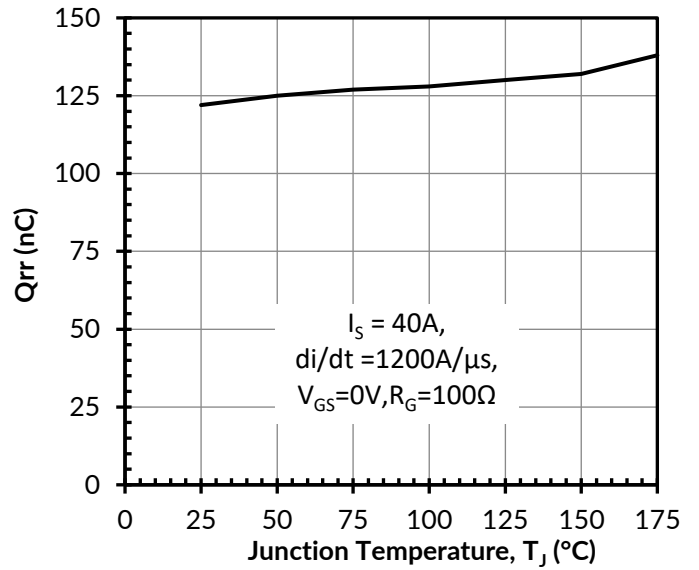


Figure 18. Reverse recovery charge  $Q_{rr}$  vs. junction temperature

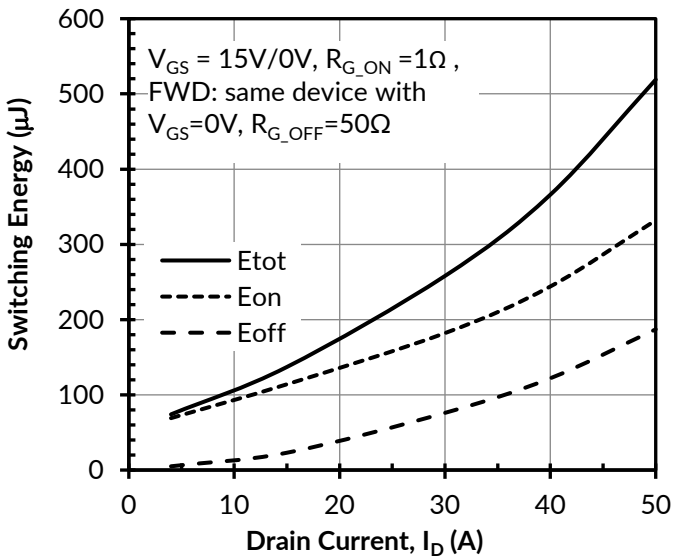


Figure 19. Clamped inductive switching energy vs. drain current at  $V_{DS} = 400\text{V}$  and  $T_J = 25^\circ\text{C}$

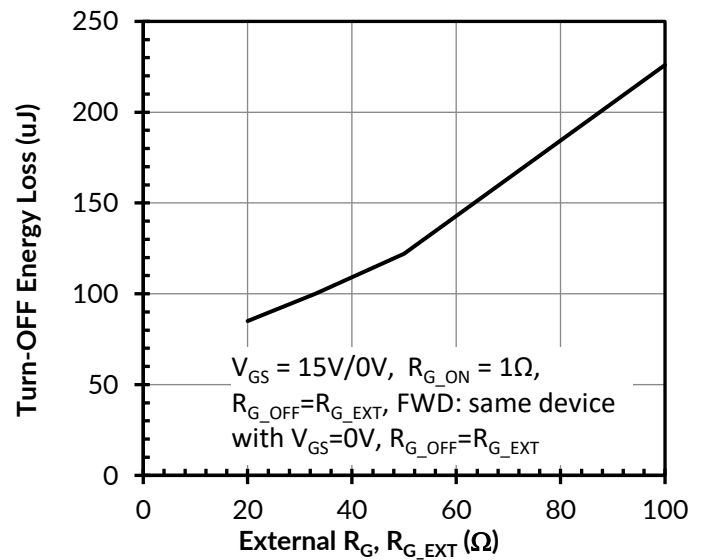


Figure 20. Clamped inductive switching energies vs.  $R_{G\_EXT}$  at  $V_{DS} = 400\text{V}$ ,  $I_D = 40\text{A}$ , and  $T_J = 25^\circ\text{C}$

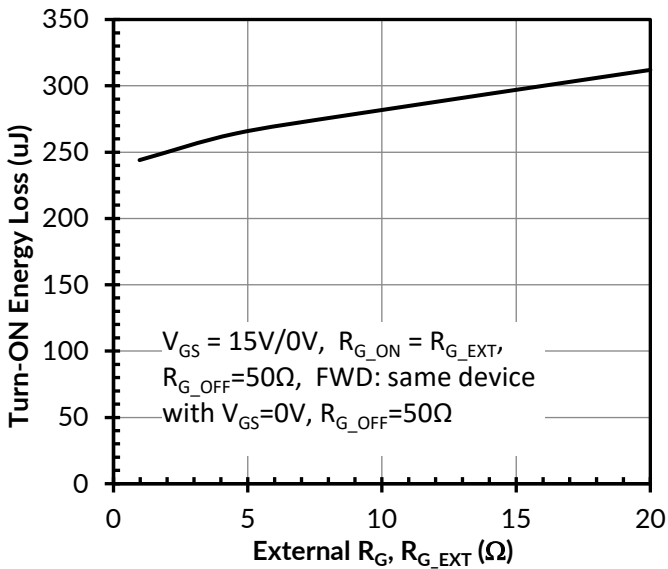


Figure 21. Clamped inductive switching energy vs. drain current at  $V_{DS} = 400V$ ,  $I_D = 40A$  and  $T_J = 25^\circ C$

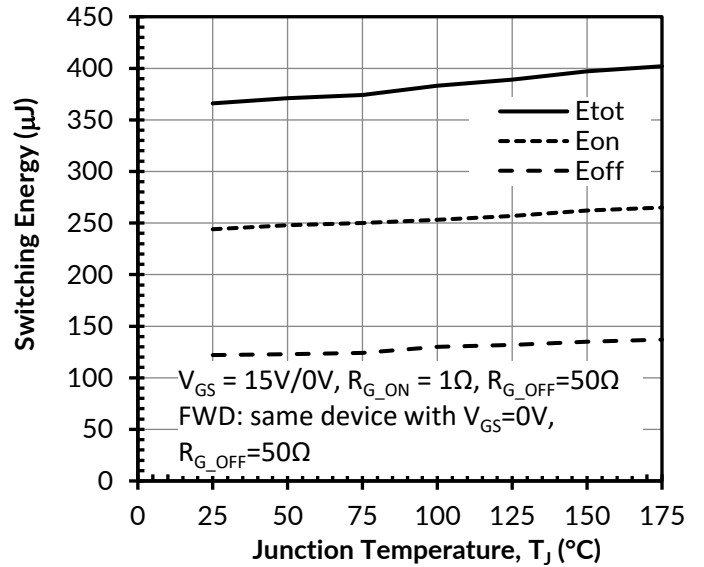


Figure 22. Clamped inductive switching energy vs. junction temperature at  $V_{DS} = 400V$  and  $I_D = 40A$

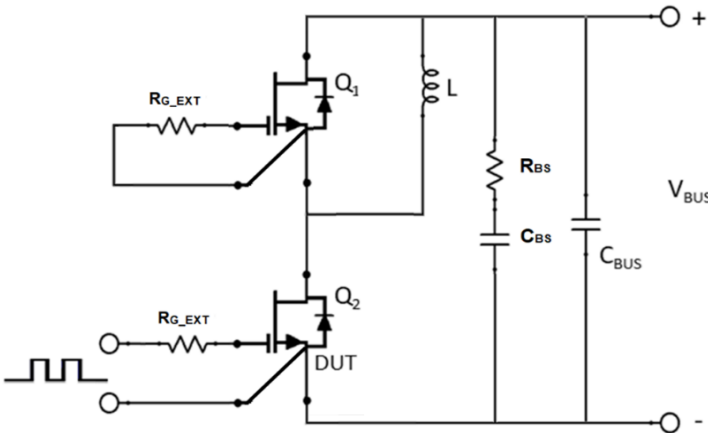


Figure 23. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber ( $R_{BS} = 2.5\Omega$ ,  $C_{BS}=100nF$ ) is used to reduce the power loop high frequency oscillations.

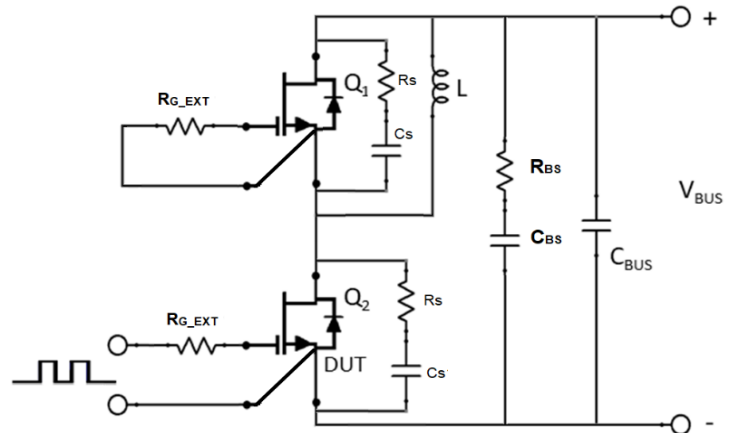
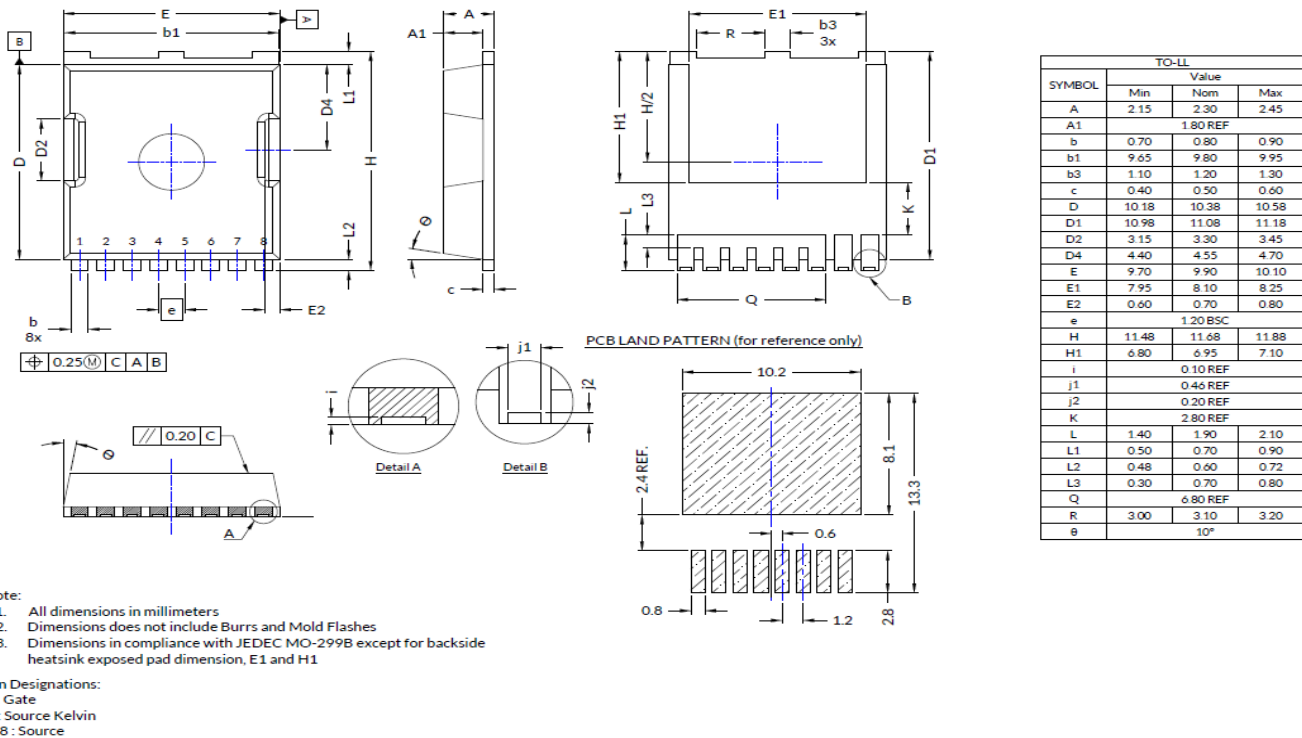


Figure 24. Schematic of the half-bridge mode switching test circuit with device RC snubbers ( $R_s = 10\Omega$ ,  $C_s = 200pF$ ) and a bus RC snubber ( $R_{BS} = 2.5\Omega$ ,  $C_{BS}=100nF$ ).

## Package Outlines



## Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ( $R_{DS(on)}$ ), output capacitance ( $C_{oss}$ ), gate charge ( $Q_G$ ), and reverse recovery charge ( $Q_{rr}$ ) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

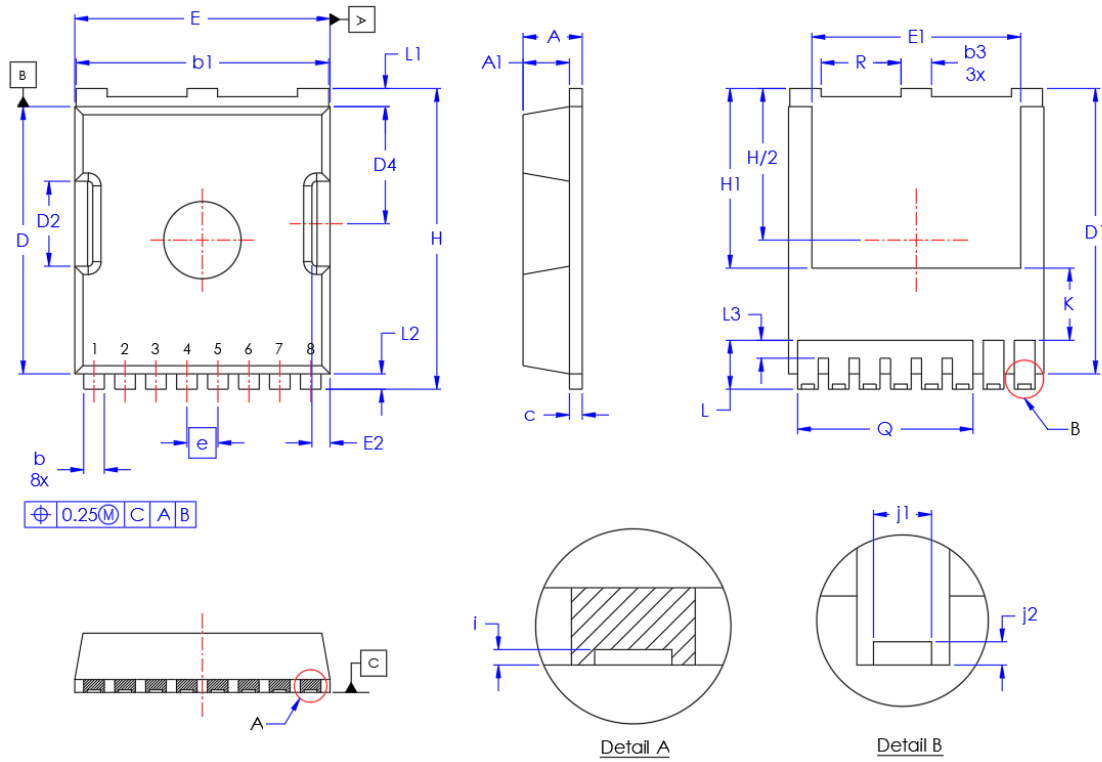
Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high  $dv/dt$  and  $di/dt$  rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see <https://www.qorvo.com/design-hub>.

A snubber circuit with a small  $R_{(G)}$ , or gate resistor, provides better EMI suppression with higher efficiency compared to using a high  $R_{(G)}$  value. There is no extra gate delay time when using the snubber circuitry, and a small  $R_{(G)}$  will better control both the turn-off  $V_{(DS)}$  peak spike and ringing duration, while a high  $R_{(G)}$  will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high  $R_{(G)}$ , while greatly reducing  $E_{(OFF)}$  from mid-to-full load range with only a small increase in  $E_{(ON)}$ . Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at <https://www.qorvo.com/design-hub>.

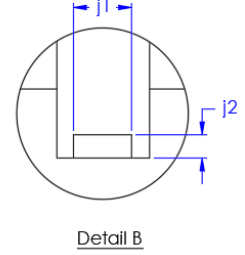
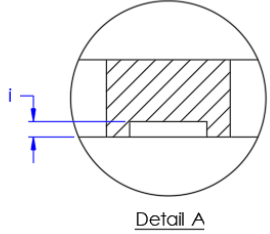
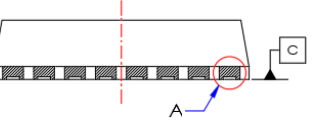
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**PACKAGE OUTLINE**



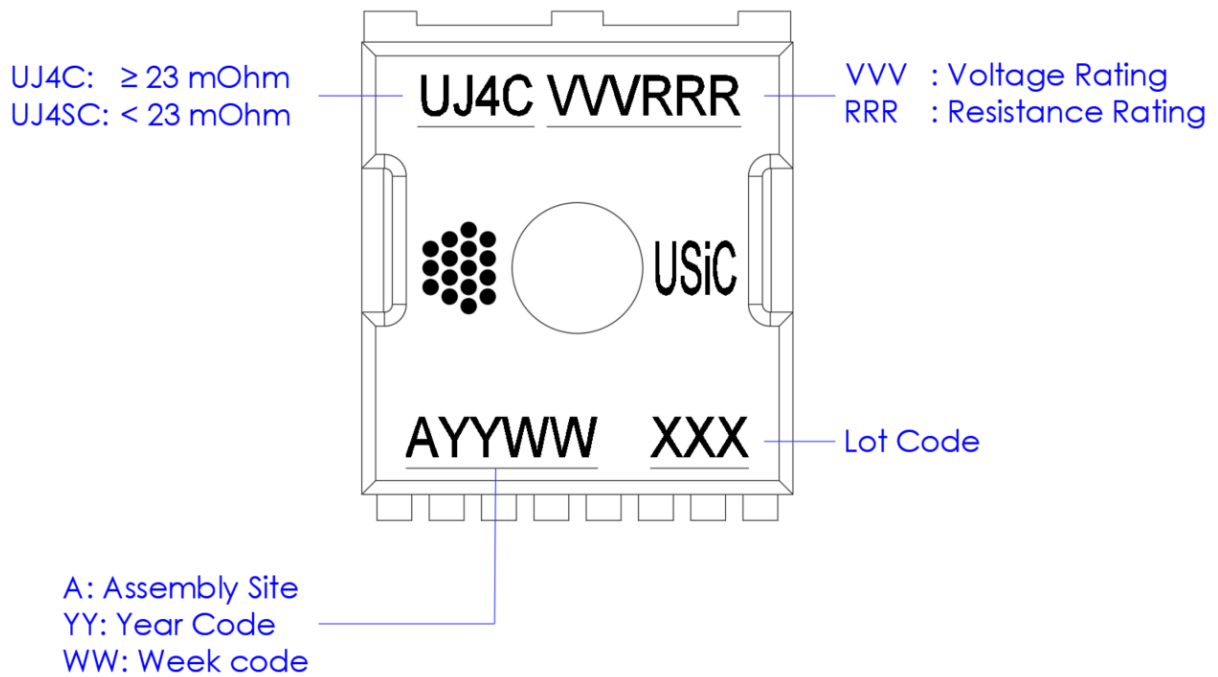
⊕ 0.25(M) C A B



SYMBOL	TO-LL Value	
	Min	Max
A	2.15	2.45
A1	1.80 REF	
b	0.65	0.90
b1	9.65	9.95
b3	1.10	1.30
c	0.40	0.60
D	10.18	10.58
D1	10.88	11.28
D2	3.15	3.45
D4	4.40	4.70
E	9.70	10.10
E1	7.95	8.25
E2	0.60	0.80
e	1.20 BSC	
H	11.48	11.88
H1	6.80	7.10
i	0.10 REF	
j1	0.46 REF	
j2	0.20 REF	
K	2.80 REF	
L	1.40	2.10
L1	0.50	0.90
L2	0.48	0.72
L3	0.30	0.80
Q	6.80 REF	
R	3.00	3.20

**Note:**

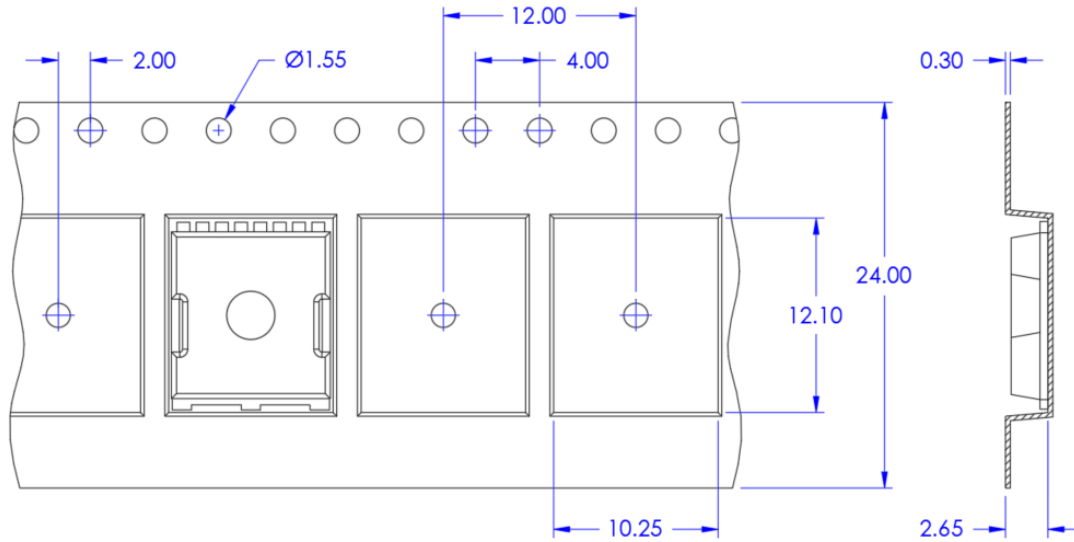
1. All dimensions in millimeters
2. Dimensions does not include Burrs and Mold Flashes

**PART MARKING**

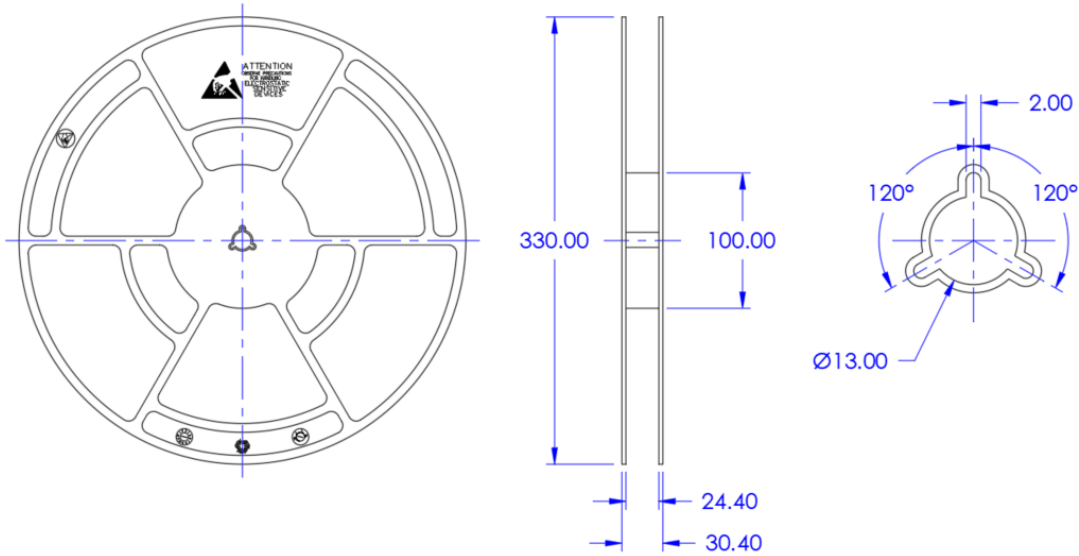


**PACKING TYPE**


*Carrier Tape*



*Reel*



All dimensions in millimeters  
Quantity per Reel: 2000 units

	TOLL PACKAGE OUTLINE, PART MARKING, TAPE AND REEL SPECIFICATION	Page 4 of 4
	DS_TOLL	Rev B

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**REVISION HISTORY**

Revision	Create Date (mm/dd/yyyy)	Description of Change	Initiator of Change
A	10/13/2023	Initial Production Release	Glenn Galang
B	01/31/2024	Corrected device orientation inside carrier tape pocket (Page 3)	Glenn Galang

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