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SiC JFET Division

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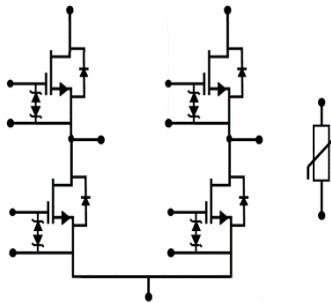
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DATASHEET

UFB15C12E1BC3N



Part Number	Package	Marking
UFB15C12E1BC3N	E1B	UFB15C12E1BC3N



Silicon Carbide (SiC) Cascode JFET Module - EliteSiC, Full-Bridge Module, 1200 V, 70 mohm

Rev. D, January 2025

Description

This SiC FET device is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s silicon-like gate-drive characteristics allows the use of unipolar gate drives, compatible with Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the E1B module package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads, and any application requiring standard gate drive. Advanced Ag sintering die attach technology gives the module superior thermal performance.

Features

- ◆ On-resistance: $R_{DS(on)} = 70m\Omega$ (typ)
- ◆ Operating temperature: 150°C (max)
- ◆ Excellent reverse recovery: $Q_{rr} = 140nC$
- ◆ Low body diode voltage: $V_{FSD} = 1.4V$
- ◆ Low gate charge: $Q_G = 46nC$
- ◆ Threshold voltage $V_{G(th)}$: 5V (typ) allowing 0 to 15V drive
- ◆ Low intrinsic capacitance
- ◆ ESD protected: HBM class 2 and CDM class C3
- ◆ AECQ Qualified

Typical applications

- ◆ EV charging
- ◆ PV inverters
- ◆ Switch mode power supplies
- ◆ Power factor correction modules
- ◆ Motor drives
- ◆ Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1200	V
Gate-source voltage	V_{GS}	DC	-20 to +20	V
		AC (f > 1Hz)	-25 to +25	V
Continuous drain current ¹	I_D	$T_C = 25^\circ\text{C}$	24	A
		$T_C = 105^\circ\text{C}$	15	A
Pulsed drain current ²	I_{DM}	$T_C = 25^\circ\text{C}$	80	A
Power dissipation per switch	P_{tot}	$T_C = 25^\circ\text{C}$	96	W
Maximum junction temperature	$T_{J,max}$		150	$^\circ\text{C}$
Operating and storage temperature	T_J, T_{STG}		-55 to 150	$^\circ\text{C}$

1. Limited by $T_{J,max}$

2. Pulse width t_p limited by $T_{J,max}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case per switch	$R_{\theta JC}$			1.0	1.3	$^\circ\text{C/W}$

NTC Thermistor Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Rated resistance	R_{25}	$T_{NTC} = 25^\circ\text{C}$		5		k Ω
Resistance value tolerance	$\Delta R/R$	$T_{NTC} = 25^\circ\text{C}$	-5		5	%
Power dissipation	P_{25}	$T_{NTC} = 25^\circ\text{C}$			20	mW
B constant	$B_{25/50}$	$R_2 = R_{25} \exp [B_{25/50} (1/T_2 - 1/(298.15 \text{ K}))]$		3375		K

Module

Parameter	Symbol	Test Conditions	Value	Units
Isolation voltage	V_{ISOL}	RMS, f = 50 Hz, t = 1 min	3	kV
Internal isolation			Al_2O_3	
Creepage distance		Terminal to heatsink	12.7	mm
		Terminal to terminal	6.3	
Clearance distance		Terminal to heatsink	10	mm
		Terminal to terminal	5	
Stray inductance module	L_{SCE}		11	nH

SiC FET Electrical Characteristics ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS}=0V, I_D=1mA$	1200			V
Total drain leakage current	I_{DSS}	$V_{DS}=1200V,$ $V_{GS}=0V, T_J=25^\circ\text{C}$		0.5	75	μA
		$V_{DS}=1200V,$ $V_{GS}=0V, T_J=150^\circ\text{C}$		2.5		
Total gate leakage current	I_{GSS}	$V_{DS}=0V, T_J=25^\circ\text{C},$ $V_{GS}=-20V / +20V$		6	20	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=12V, I_D=15A,$ $T_J=25^\circ\text{C}$		70	90	m Ω
		$V_{GS}=12V, I_D=15A,$ $T_J=125^\circ\text{C}$		111		
		$V_{GS}=12V, I_D=15A,$ $T_J=150^\circ\text{C}$		129		
Gate threshold voltage	$V_{G(th)}$	$V_{DS}=5V, I_D=10mA$	4	5	6	V
Gate resistance	R_G	$f=1\text{MHz}, \text{open drain}$		4.5		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current ¹	I_S	$T_C=25^\circ\text{C}$			24	A
Diode pulse current ²	$I_{S,pulse}$	$T_C=25^\circ\text{C}$			80	A
Forward voltage	V_{FSD}	$V_{GS}=0V, I_S=10A,$ $T_J=25^\circ\text{C}$		1.4	2	V
		$V_{GS}=0V, I_S=10A,$ $T_J=150^\circ\text{C}$		1.63		
Reverse recovery charge	Q_{rr}	$V_{DS}=800V, I_S=15A,$ $V_{GS}=0V, R_G=5\Omega,$ $di/dt=1200A/\mu\text{s},$ $T_J=25^\circ\text{C}$		140		nC
Reverse recovery time	t_{rr}	$V_{DS}=800V, I_S=15A,$ $V_{GS}=0V, R_G=5\Omega,$ $di/dt=1200A/\mu\text{s},$ $T_J=25^\circ\text{C}$		35		ns
Reverse recovery charge	Q_{rr}	$V_{DS}=800V, I_S=15A,$ $V_{GS}=0V, R_G=5\Omega,$ $di/dt=1200A/\mu\text{s},$ $T_J=150^\circ\text{C}$		141		nC
Reverse recovery time	t_{rr}	$V_{DS}=800V, I_S=15A,$ $V_{GS}=0V, R_G=5\Omega,$ $di/dt=1200A/\mu\text{s},$ $T_J=150^\circ\text{C}$		35		ns

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	$V_{DS}=800V, V_{GS}=0V$ $f=100kHz$		1445		pF
Output capacitance	C_{oss}			55		
Reverse transfer capacitance	C_{rss}			2		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to 800V, $V_{GS}=0V$		63		pF
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}=0V$ to 800V, $V_{GS}=0V$		128		pF
C_{oss} stored energy	E_{oss}	$V_{DS}=800V, V_{GS}=0V$		20		μJ
Total gate charge	Q_G	$V_{DS}=800V, I_D=15A,$ $V_{GS} = -5V$ to 15V		46		nC
Gate-drain charge	Q_{GD}			7		
Gate-source charge	Q_{GS}			19		
Turn-on delay time	$t_{d(on)}$	Notes 3 and 4		22.4		ns
Rise time	t_r	$V_{DS}=800V, I_D=15A,$ Gate Driver = -5V to +15V, $R_{G,ON}=1\Omega, R_{G,OFF}=20\Omega,$ inductive Load,		18.4		
Turn-off delay time	$t_{d(off)}$			65		
Fall time	t_f			10.4		
Turn-on energy	E_{ON}		FWD: same device with		396	
Turn-off energy	E_{OFF}	$V_{GS} = 0V$ and $R_G = 20\Omega,$		42		
Total switching energy	E_{TOTAL}	$T_J=25^\circ C$		438		
Turn-on delay time	$t_{d(on)}$	Notes 3 and 4		22		ns
Rise time	t_r	$V_{DS}=800V, I_D=15A,$ Gate Driver = -5V to +15V, $R_{G,ON}=1\Omega, R_{G,OFF}=20\Omega,$ inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_G = 20\Omega,$		16		
Turn-off delay time	$t_{d(off)}$			67		
Fall time	t_f			12		
Turn-on energy	E_{ON}		$T_J=150^\circ C$		381	
Turn-off energy	E_{OFF}			41		
Total switching energy	E_{TOTAL}			422		

3. Measured with the half-bridge mode switching test circuit in Figure 23.

4. A bus RC snubber ($R_{BS} = 2.5\Omega, C_{BS}=200nF$) must be applied to reduce the power loop high frequency oscillations.

Typical Performance - Dynamic (continued)

Parameter	Symbol	Test Conditions	Value			Units	
			Min	Typ	Max		
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6, $V_{DS}=800V$, $I_D=15A$, Gate Driver = -5V to +15V, $R_{G_ON} = 1\Omega$, $R_{G_OFF}=1\Omega$, inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_G = 1\Omega$, RC snubber: $R_S=5\Omega$ and $C_S=68pF$, $T_J=25^\circ C$		44		ns	
Rise time	t_r			20			
Turn-off delay time	$t_{d(off)}$			32			
Fall time	t_f			17.6			
Turn-on energy including R_S energy	E_{ON}				474		μJ
Turn-off energy including R_S energy	E_{OFF}				62		
Total switching energy	E_{TOTAL}				536		
Snubber R_S energy during turn-on	E_{RS_ON}				1		
Snubber R_S energy during turn-off	E_{RS_OFF}				0.7		
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6, $V_{DS}=800V$, $I_D=15A$, Gate Driver = -5V to +15V, $R_{G_ON} = 1\Omega$, $R_{G_OFF}=1\Omega$, inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_G = 1\Omega$, RC snubber: $R_S=5\Omega$ and $C_S=68pF$, $T_J=150^\circ C$		42.4		ns	
Rise time	t_r			19.2			
Turn-off delay time	$t_{d(off)}$			32.8			
Fall time	t_f			18.4			
Turn-on energy including R_S energy	E_{ON}				450		μJ
Turn-off energy including R_S energy	E_{OFF}				64		
Total switching energy	E_{TOTAL}				514		
Snubber R_S energy during turn-on	E_{RS_ON}				0.9		
Snubber R_S energy during turn-off	E_{RS_OFF}				0.9		

5. Measured with the half-bridge mode switching test circuit in Figure 24.

6. In this table, the switching energies (turn-on energy, turn-off energy and total energy) presented include the device RC snubber energy losses.

SiC FET Typical Performance Diagrams

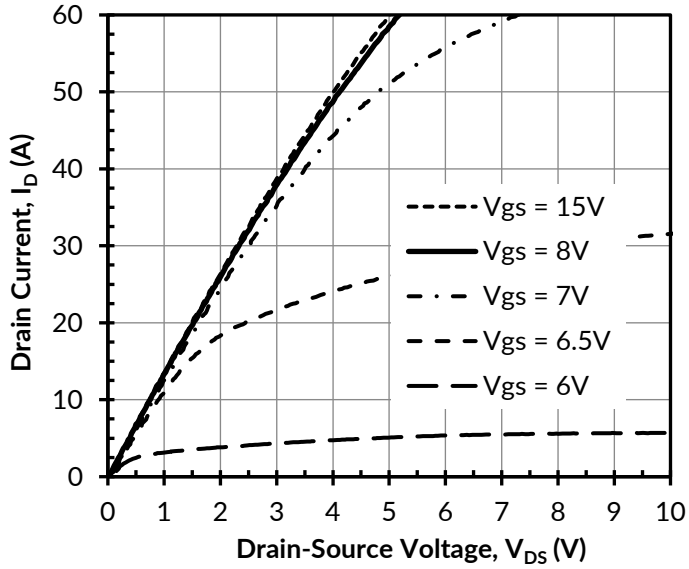


Figure 1. Typical output characteristics at $T_j = -55^\circ\text{C}$, $t_p < 250\mu\text{s}$

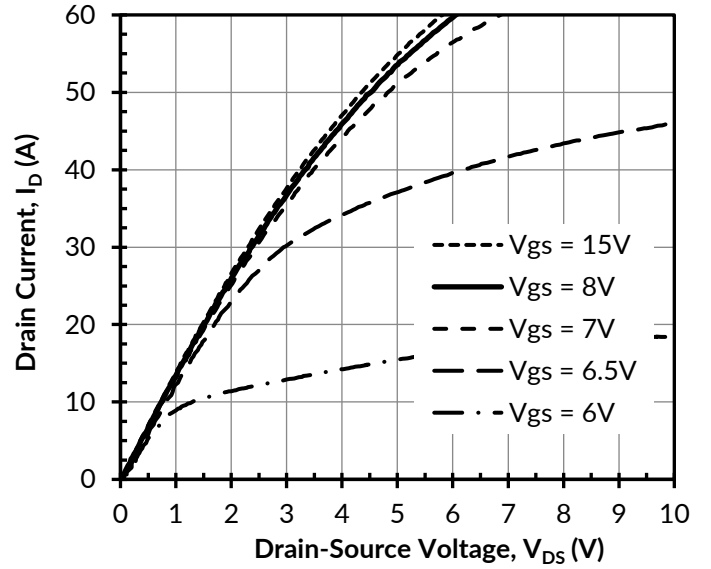


Figure 2. Typical output characteristics at $T_j = 25^\circ\text{C}$, $t_p < 250\mu\text{s}$

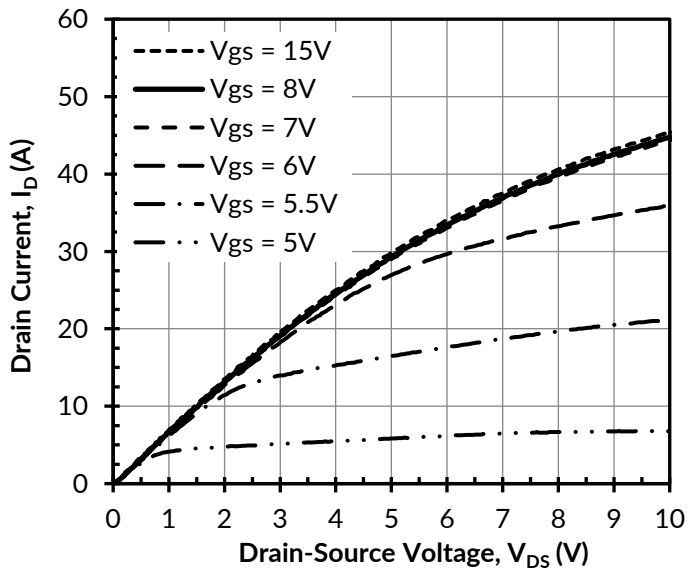


Figure 3. Typical output characteristics at $T_j = 150^\circ\text{C}$, $t_p < 250\mu\text{s}$

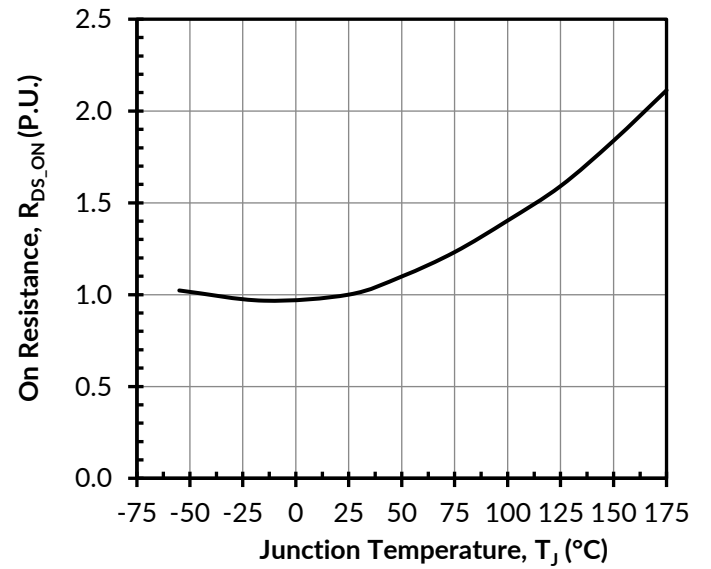


Figure 4. Normalized on-resistance vs. temperature at $V_{GS} = 12\text{V}$ and $I_D = 20\text{A}$

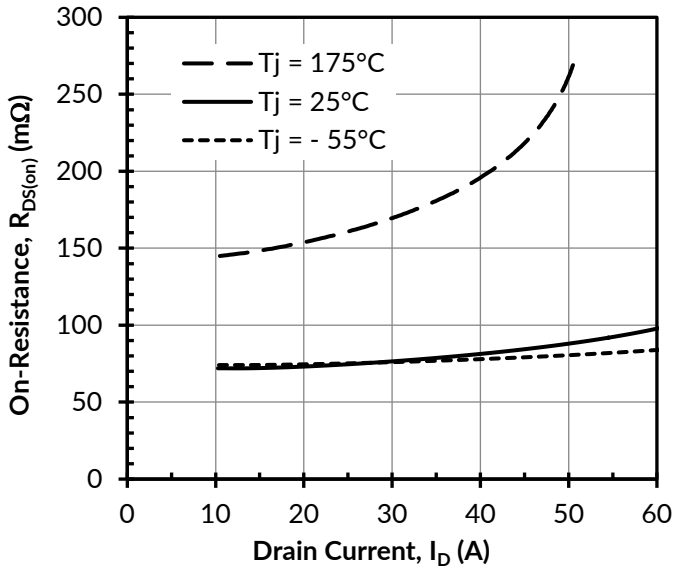


Figure 5. Typical drain-source on-resistances at $V_{GS} = 12V$

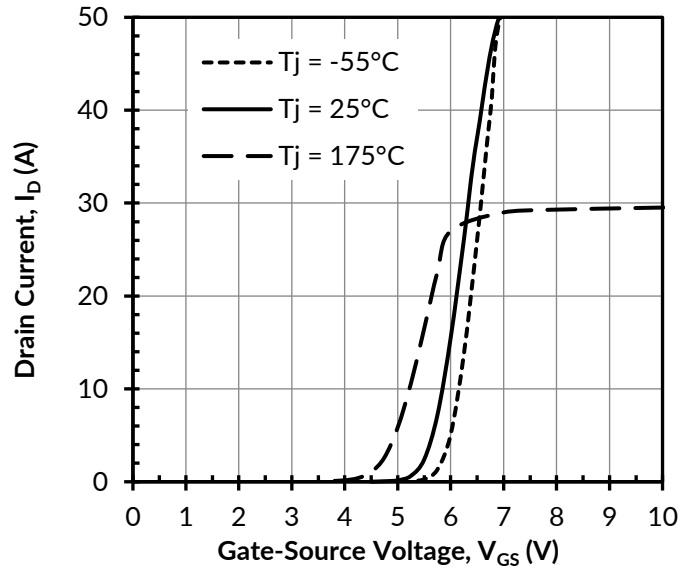


Figure 6. Typical transfer characteristics at $V_{DS} = 5V$

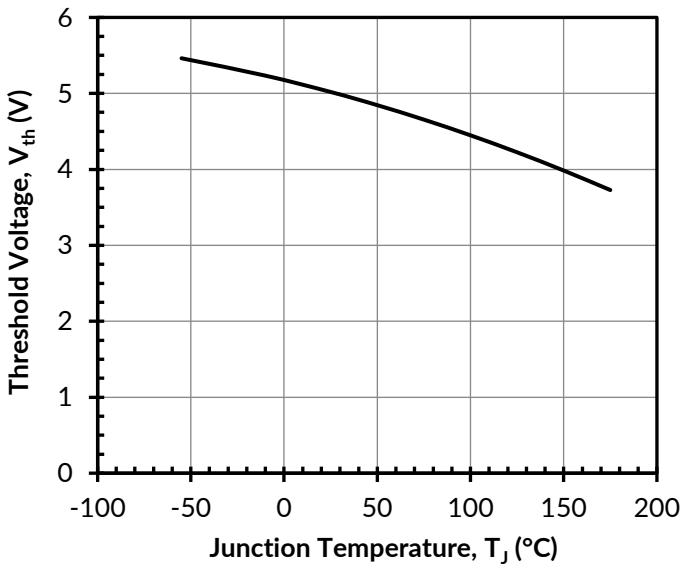


Figure 7. Threshold voltage vs. junction temperature at $V_{DS} = 5V$ and $I_D = 10mA$

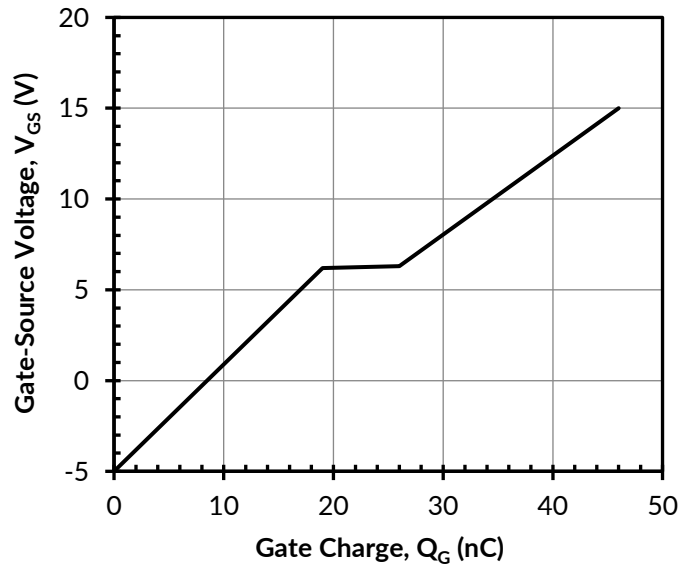


Figure 8. Typical gate charge at $V_{DS} = 800V$ and $I_D = 15A$

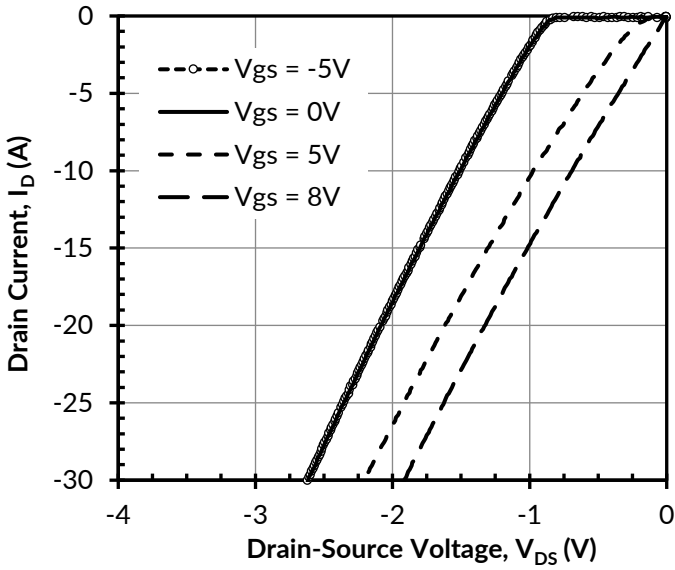


Figure 9. 3rd quadrant characteristics at $T_J = -55^\circ\text{C}$

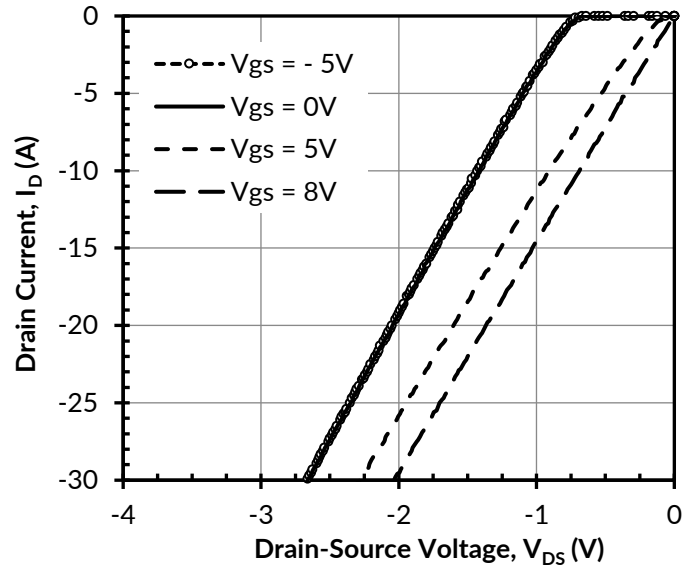


Figure 10. 3rd quadrant characteristics at $T_J = 25^\circ\text{C}$

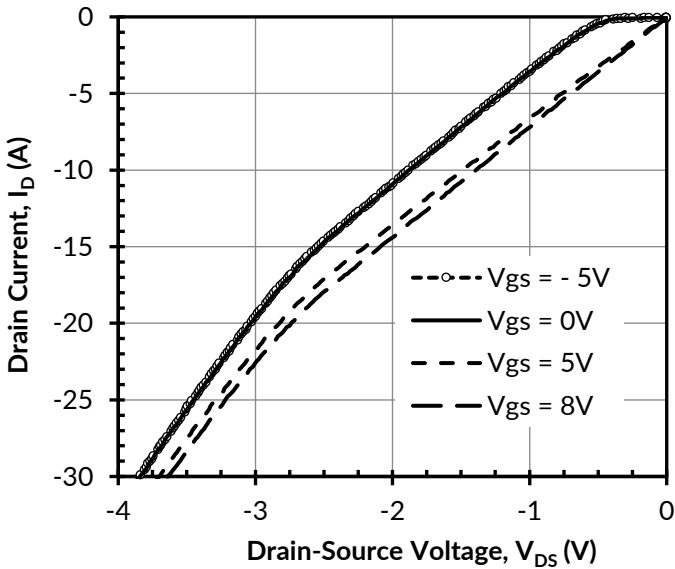


Figure 11. 3rd quadrant characteristics at $T_J = 150^\circ\text{C}$

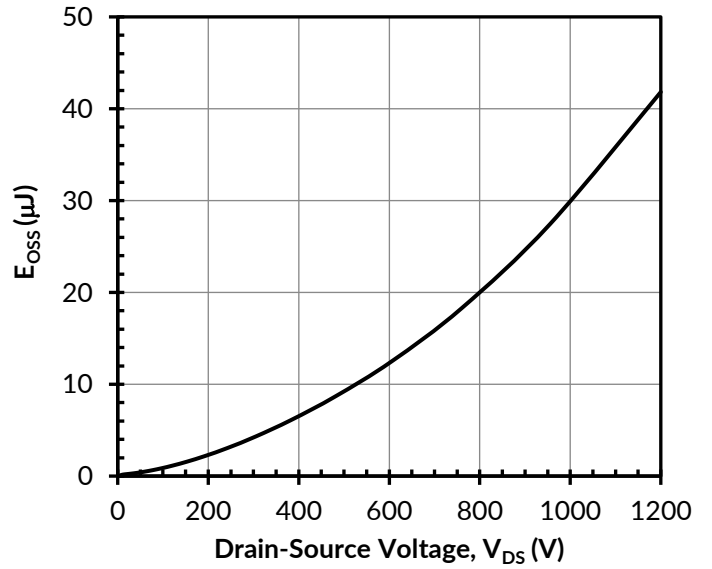


Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0\text{V}$

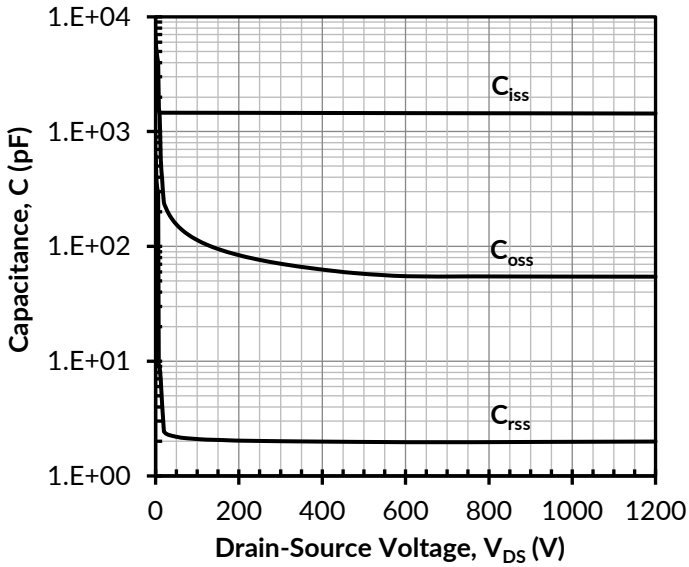


Figure 13. Typical capacitances at $f = 100\text{kHz}$ and $V_{GS} = 0\text{V}$

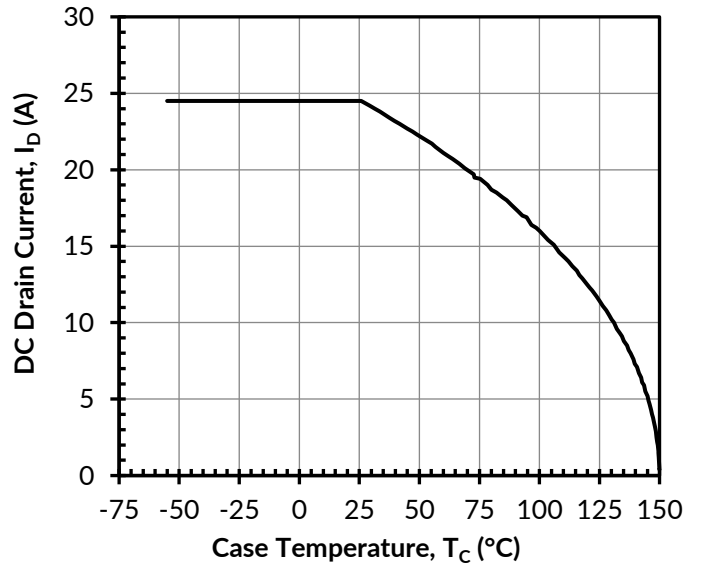


Figure 14. DC drain current derating

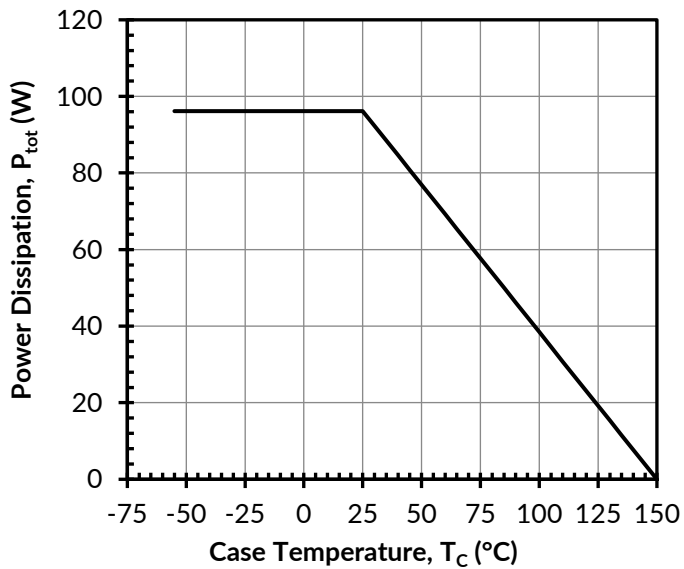


Figure 15. Total power dissipation

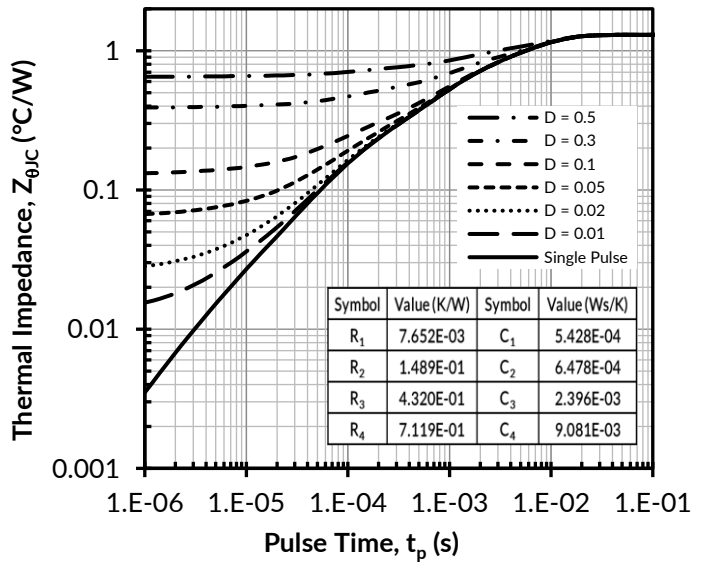


Figure 16. Maximum transient thermal impedance and parameters for thermal equivalent circuit (Foster) model

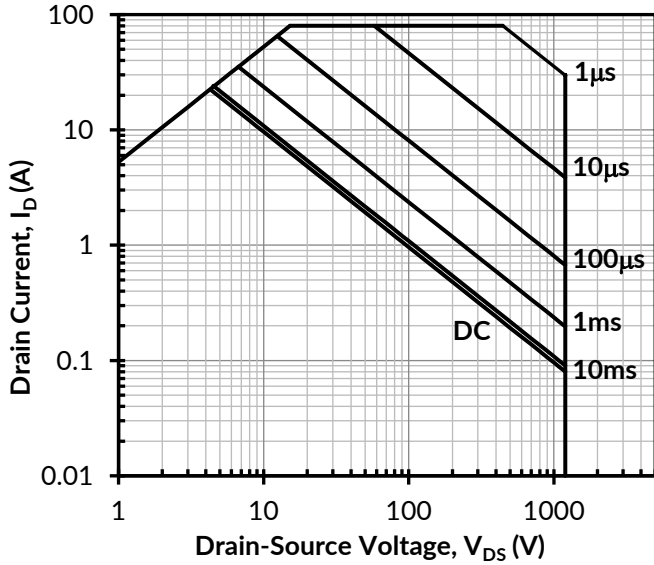


Figure 17. Safe operation area at $T_C = 25^\circ\text{C}$, $D = 0$, Parameter t_p

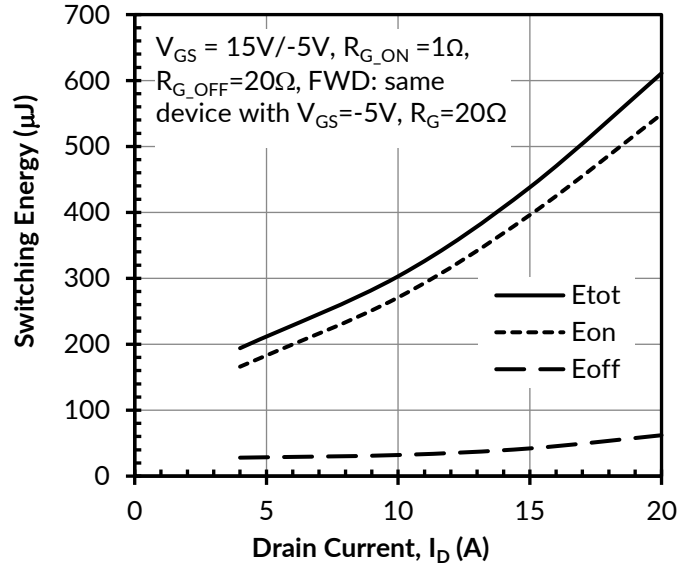


Figure 18. Clamped inductive switching energy vs. drain current at $V_{DS} = 800\text{V}$ and $T_J = 25^\circ\text{C}$

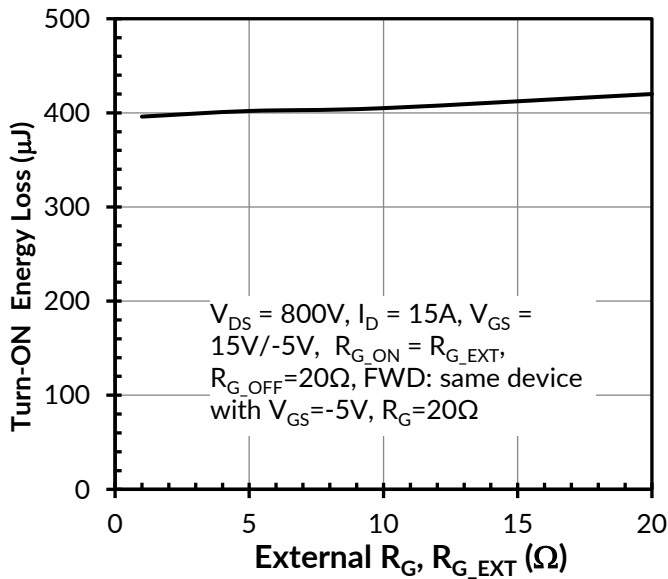


Figure 19. Clamped inductive switching turn-on energy vs. turn-on gate resistance R_G

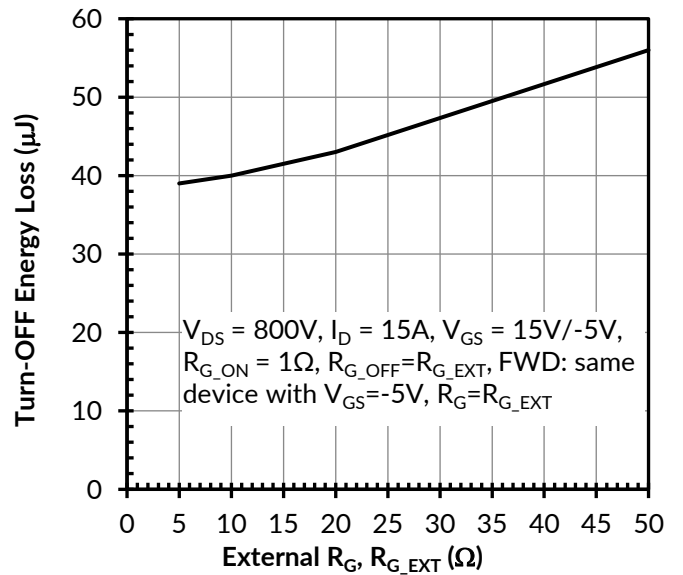


Figure 20. Clamped inductive switching turn-off energy vs. turn-off gate resistance R_G

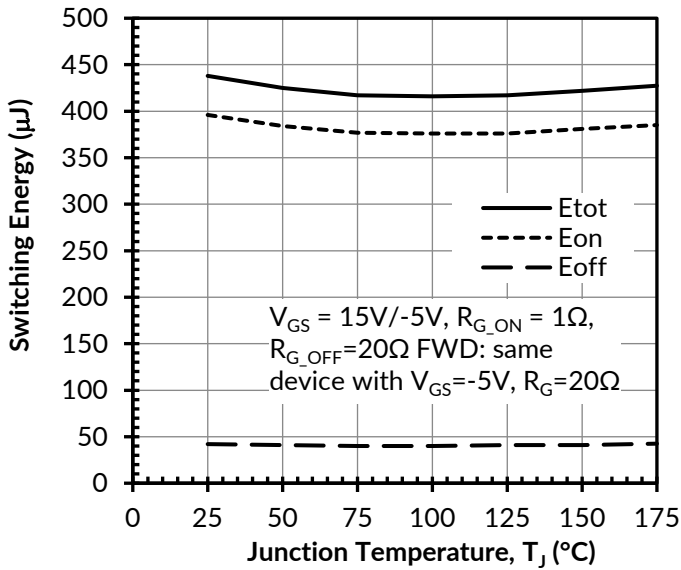


Figure 21. Clamped inductive switching energy vs. junction temperature at $V_{DS} = 800V$ and $I_D = 15A$

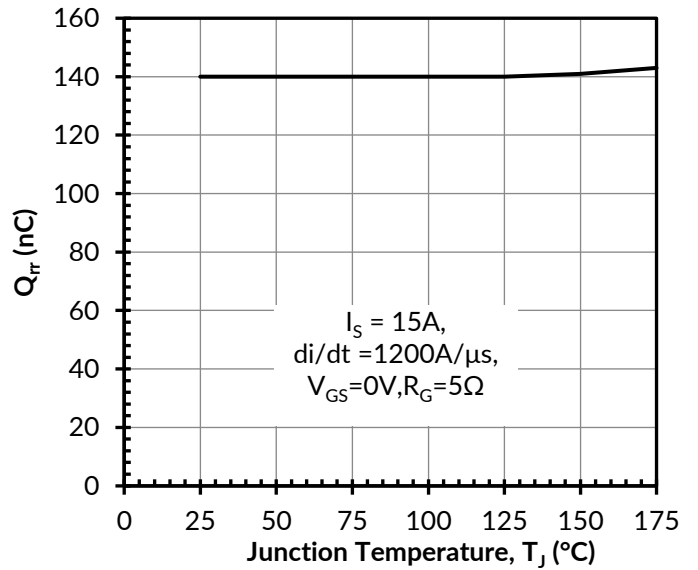


Figure 22. Reverse recovery charge Q_{rr} vs. junction temperature at $V_{DS} = 800V$

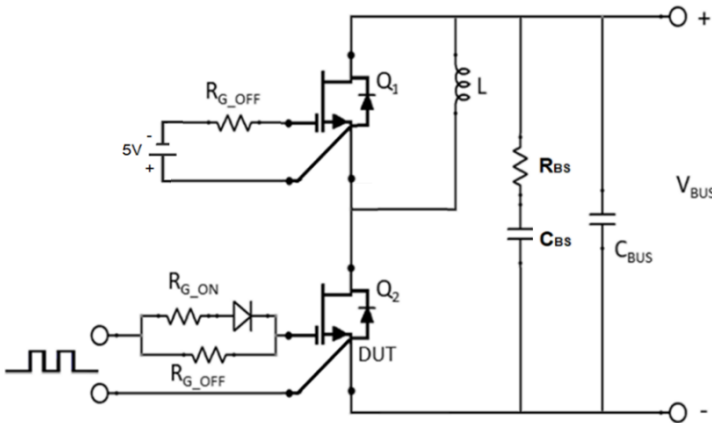


Figure 23. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber ($R_{BS} = 2.5\Omega$, $C_{BS} = 200nF$) must be applied to reduce the power loop high frequency oscillations.

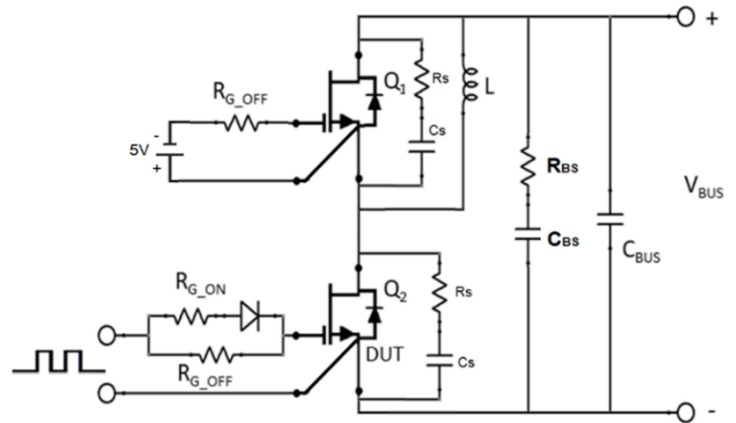
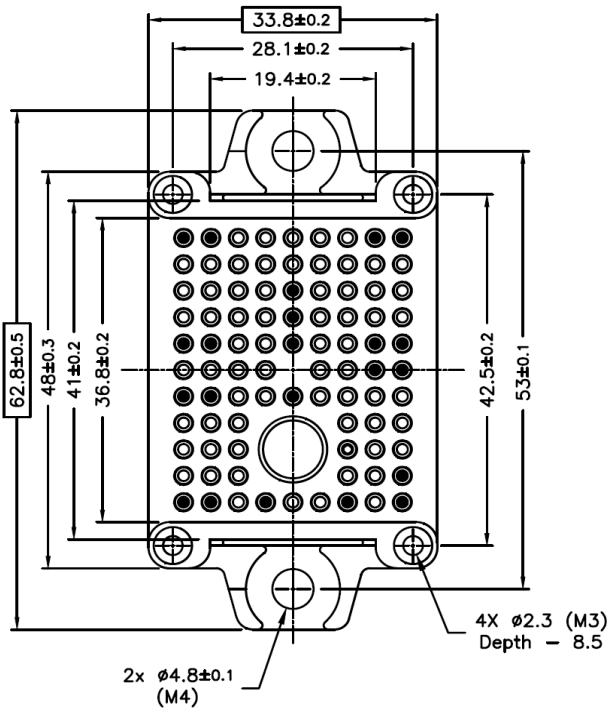
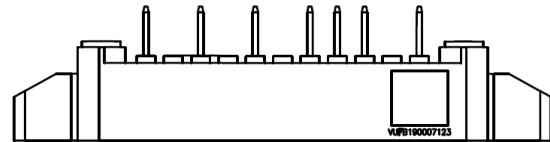
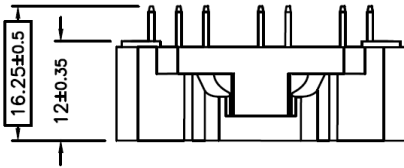
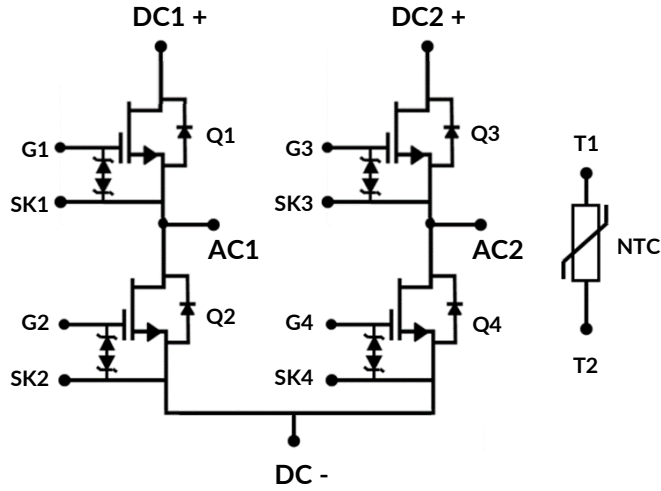
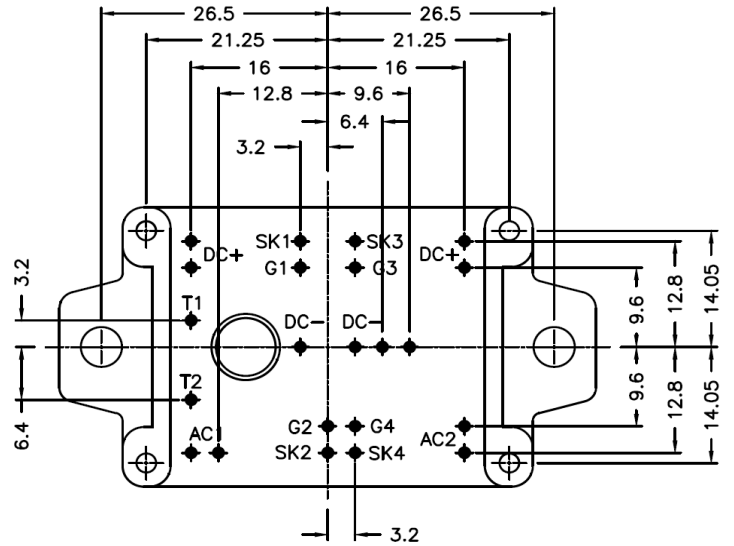


Figure 24. Schematic of the half-bridge mode switching test circuit with device RC snubbers ($R_s = 5\Omega$, $C_s = 68pF$) and a bus RC snubber ($R_{BS} = 2.5\Omega$, $C_{BS} = 200nF$).

Circuit Diagram and Pin Definitions



PCB HOLE PATTERN



NOTES:

1. All dimensions in millimeters (mm)
2. General tolerance: ± 0.1 mm, unless otherwise specified

Important Mounting Information

This product is recommended for use with solder pin attach and phase change thermal interface materials, and not recommended for implementations using press fit and application of thermal grease. Please refer to mounting guidelines and user guide documents associated with this product for detailed information.

Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see <https://www.qorvo.com/innovation/power-solutions/sic-power/sic-fet-design-tips>.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the Qorvo website at <https://www.qorvo.com/innovation/power-solutions/sic-power/sic-fet-design-tips>.

Important notice

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E1B PACKAGE OUTLINE, PART MARKING and TRAY SPECIFICATION

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Introduction

This Manufacturing Note is intended for manufacturing engineers who are currently using the module for prototype or production manufacturing. The information provided in this document is meant to assist customers with the set-up and characterization of their products.

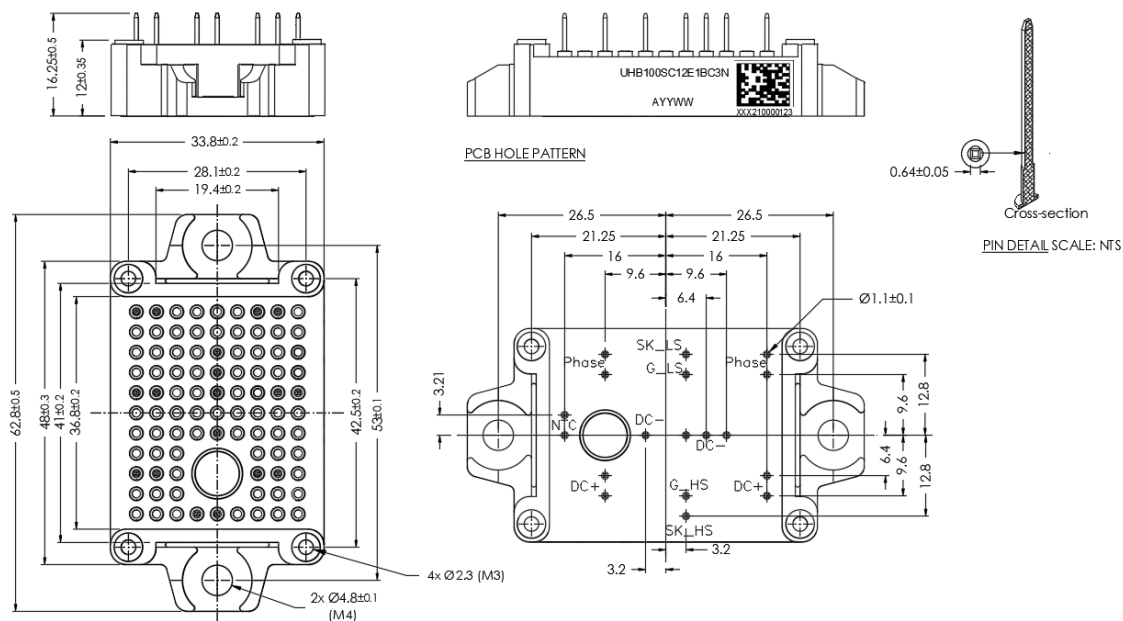
Module Package Description

This module is a SiC FET device based on a unique cascode circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's silicon-like gate-drive characteristics allows the use of unipolar gate drives, compatible with Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the E1B module package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads, and any application requiring standard gate drive Package Outline Drawing.

Package Outline Drawing

This product is recommended for use with solder pin attach and phase change thermal interface materials, and not recommended for implementations using press fit and application of thermal grease. Please refer to mounting guidelines and user guide documents associated with this product for detailed information.

Package outline for Half Bridge modules: UHB100SC12E1BC3N & UHB50SC12E1BC3N

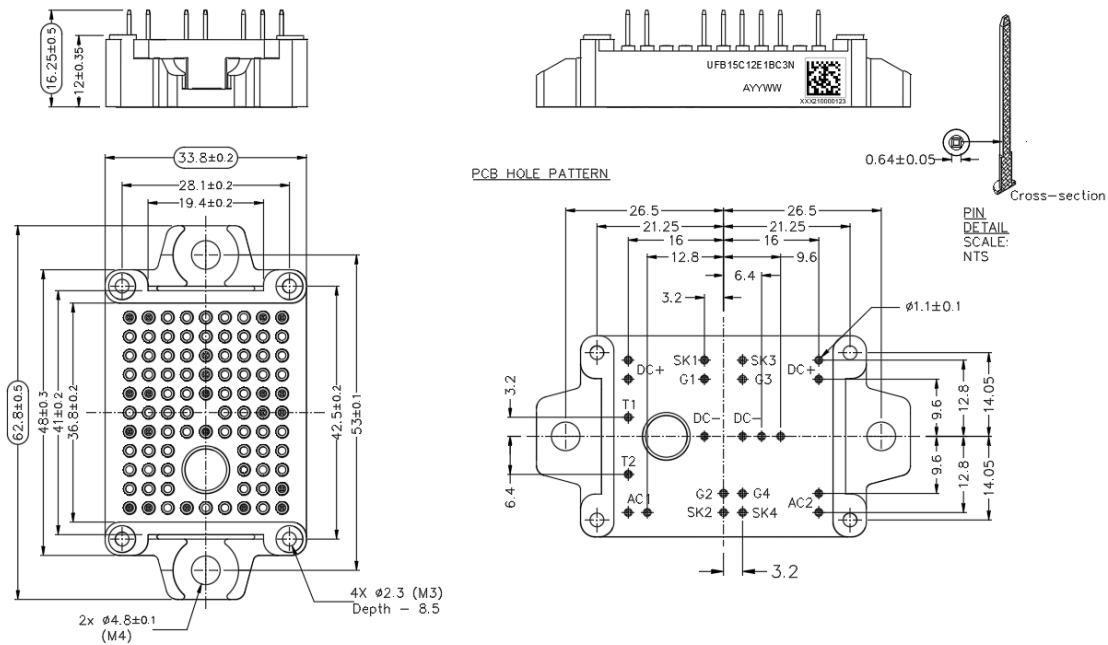


NOTES:

1. All dimensions in millimeters (mm)
2. General tolerance: ± 0.1 mm, unless otherwise specified

MANUFACTURING NOTE: E1B PACKAGE OUTLINE, PART MARKING and TRAY SPECIFICATION

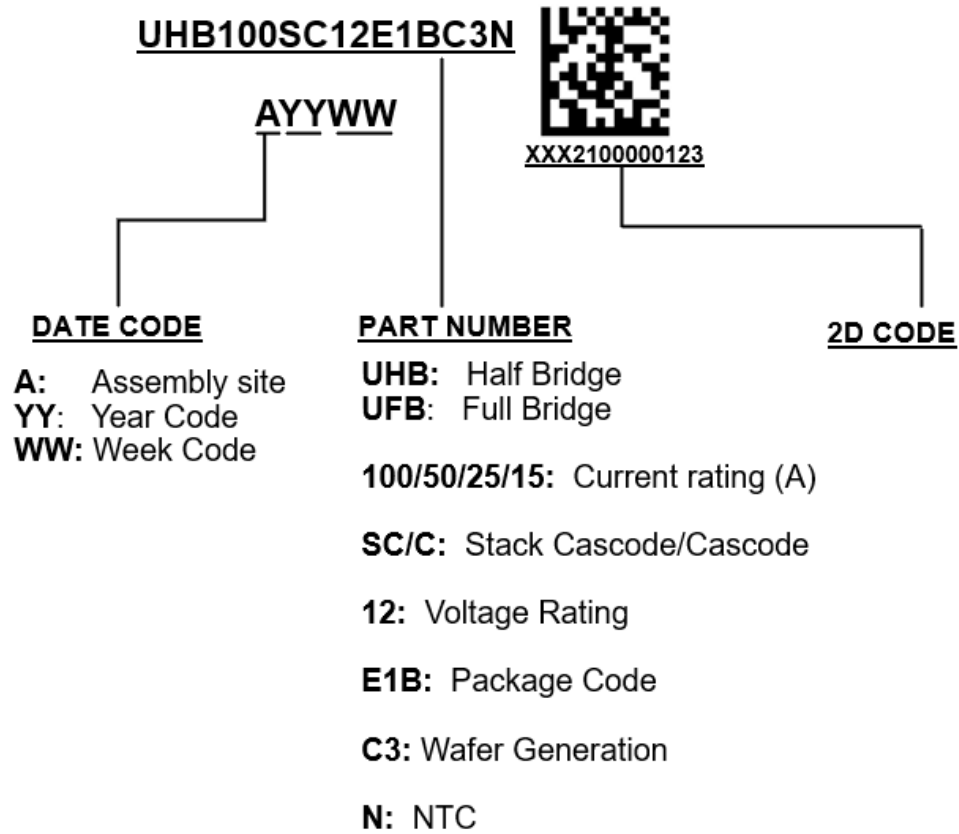
Package outline for Full Bridge modules: UFB15C12E1BC3N & UFB25SC12E1BC3N



NOTES:

1. All dimensions in millimeters (mm)
2. General tolerance: ± 0.1 mm, unless otherwise specified

Branding Diagram (Marking)



Carriers

Tray and Shipping Instructions

The module is placed in an ESD tray with a pocket carrier that holds the module in dead bug orientation. The pocket is designed to hold the module for shipping and for loading onto manufacturing equipment, while protecting the body and the solder pins from damaging stresses with a lid to seal the units firmly. Then trays are placed in a shipping box with desiccant, proper label, and protective packaging so secure the tray firmly prior packing with tape.

The individual tray pocket design and count can vary from vendor to vendor.

Tray

1. Tray size and specification for large quantity

Tray size: 356x276x30 mm
Material: PS
Unit Quantity per tray: 24 pcs



Figure 1

2. Tray size and specification for small quantity

Tray size: 199x192x31 mm
Material: PS
Unit Quantity per tray: 6 pcs

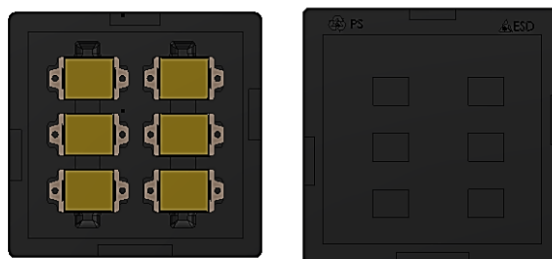


Figure 2

Storage and Handling

Storage and Handling Conditions

Excessive forces from shock or vibration as well as environmental factors must be avoided when transporting and handling the modules. Although it is not advised, it is feasible to store the modules at the temperature ranges listed in the datasheet. Furthermore, the modules can be subjected to environmental conditions, see reference below.

IEC 60721-3-1: Classification of environmental conditions.

IEC 60721- 3-2: Classification of groups of environmental parameters and their severities - Transportation and handling/

IEC 60721-3-3 Classification of groups of environmental parameters and their severities – Stationary use at weather protected locations.

ESD

Electrostatic discharge occurs naturally in the environment. With the increase in voltage potential, the outlets of neutralization or discharge will be sought. If the acquired discharge route is through a semiconductor device, destructive damage will result.

ESD countermeasure methods should be developed and used to Control potential ESD damage during handling in a factory environment at each manufacturing site.

This part is considered ESD sensitive and needs to be handled accordingly.

Qorvo recommends using standard ESD precautions (see Reference Documents) when handling these devices.

Reference Documents:

1. JEDEC Standard JESD625-A, "Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices."
2. ANSI/ESD S20.20, "Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)."

NOTE: The ESD level for this part is documented in the product qualification report that is available from Qorvo.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: +1 833-641-3811

Email: customer.support@qorvo.com

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