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DATA SHEET
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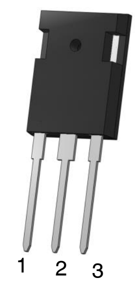
Silicon Carbide (SiC) Cascode JFET - EliteSiC, Power N-Channel, TO247-3, 1200 V, 80 mohm

UF3C120080K3S



TO247-3
CASE 340AK

Description

This SiC FET device is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si super-junction devices. Available in the TO247-3 package, this device exhibits ultralow gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads when used with recommended RC-snubbers, and any application requiring standard gate drive.

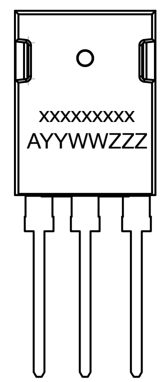
Features

- Typical On-resistance $R_{DS(on),typ}$ of 80 mΩ
- Maximum Operating Temperature of 175 °C
- Excellent Reverse Recovery
- Low Gate Charge
- Low Intrinsic Capacitance
- ESD Protected, HBM Class 2
- Very Low Switching Losses (required RC-snubber loss negligible under typical operating conditions)
- AEC-Q101 Qualified and PPAP Capable
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

Typical Applications

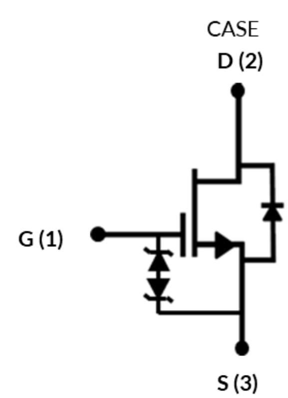
- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating

MARKING DIAGRAM



xxxxxxxxx = Specific Device Number
A = Assembly Location
YY = Year
WW = Work Week
ZZZ = Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	V_{DS}		1200	V
Gate-source Voltage	V_{GS}	DC	−25 to +25	V
Continuous Drain Current (Note 1)	I_D	T_C = 25 °C	33	A
		T_C = 100 °C	24	A
Pulsed Drain Current (Note 2)	I_{DM}	T_C = 25 °C	77	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	L = 15 mH, I_{AS} = 2.8 A	58.5	mJ
Power Dissipation	P_{tot}	T_C = 25 °C	254.2	W
Maximum Junction Temperature	$T_{J,max}$		175	°C
Operating and Storage Temperature	T_J, T_{STG}		−55 to 175	°C
Max. Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	T_L		250	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by $T_{J,max}$
2. Pulse width t_p limited by $T_{J,max}$
3. Starting T_J = 25 °C

THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		–	0.45	0.59	°C/W

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
TYPICAL PERFORMANCE – STATIC							
Drain-source Breakdown Voltage	BV_{DS}	V_{GS} = 0 V, I_D = 1 mA		1200	–	–	V
Total Drain Leakage Current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V, T_J = 25 °C		–	10	75	µA
		V_{DS} = 1200 V, V_{GS} = 0 V, T_J = 175°C		–	50	–	
Total Gate Leakage Current	I_{GSS}	V_{DS} = 0 V, T_J = 25 °C, V_{GS} = −20 V/ +20 V		–	6	±20	µA
Drain-source On-resistance	$R_{DS(on)}$	V_{GS} = 12 V, I_D = 20 A	T_J = 25 °C	–	80	100	mΩ
			T_J = 125 °C	–	130	–	
			T_J = 175 °C	–	172	–	
Gate Threshold Voltage	$V_{G(th)}$	V_{DS} = 5 V, I_D = 10 mA		4	5	6	V
Gate Resistance	R_G	f = 1 MHz, open drain		–	4.5	–	Ω
TYPICAL PERFORMANCE – REVERSE DIODE							
Diode Continuous Forward Current (Note 4)	I_S	T_C = 25 °C		–	–	33	A
Diode Pulse Current (Note 5)	$I_{S,pulse}$	T_C = 25 °C		–	–	77	A
Forward Voltage	V_{FSD}	V_{GS} = 0 V, I_S = 10 A, T_J = 25 °C		–	1.5	2	V
		V_{GS} = 0 V, I_S = 10 A, T_J = 175 °C		–	2	–	
Reverse Recovery Charge	Q_{rr}	V_{DS} = 800 V, I_S = 20 A, V_{GS} = −5 V, R_{G_EXT} = 10 Ω, di/dt = 2300 A/µs, T_J = 25 °C		–	212	–	nC
Reverse Recovery Time	t_{rr}			–	23	–	ns
Reverse Recovery Charge	Q_{rr}	V_{DS} = 800 V, I_S = 20 A, V_{GS} = −5 V, R_{G_EXT} = 10 Ω, di/dt = 2300 A/µs, T_J = 150 °C		–	124	–	nC
Reverse Recovery Time	t_{rr}			–	13	–	ns

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 100 V, V_{GS} = 0 V, f = 100 kHz	–	1500	–	pF
Output Capacitance	C_{oss}		–	100	–	
Reverse Transfer Capacitance	C_{rss}		–	2.1	–	
Effective Output Capacitance, Energy Related	$C_{oss(er)}$	V_{DS} = 0 V to 800 V, V_{GS} = 0 V	–	59	–	pF
Effective Output Capacitance, Time Related	$C_{oss(tr)}$		–	136	–	pF
C_{oss} Stored Energy	E_{oss}	V_{DS} = 800 V, V_{GS} = 0 V	–	19	–	μJ
Total Gate Charge	Q_G	V_{DS} = 800 V, I_D = 20 A, V_{GS} = −5 V to 15 V	–	51	–	nC
Gate-drain Charge	Q_{GD}		–	11	–	
Gate-source Charge	Q_{GS}		–	19	–	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 800 V, I_D = 20 A, Gate Driver = −5 V to +15 V, Turn-on $R_{G,EXT}$ = 1 Ω, Turn-off $R_{G,EXT}$ = 22 Ω, Inductive Load, FWD: Same Device With V_{GS} = −5 V, R_G = 22 Ω, RC Snubber: R_S = 5 Ω, C_S = 150 pF, T_J = 25 °C	–	26	–	ns
Rise Time	t_r		–	17	–	
Turn-off Delay Time	$t_{d(off)}$		–	57	–	
Fall Time	t_f		–	19	–	
Turn-on Energy Including R_S Energy (Note 6)	E_{ON}		–	500	–	μJ
Turn-off Energy Including R_S Energy (Note 6)	E_{OFF}		–	85	–	
Total Switching Energy Including R_S Energy (Note 6)	E_{TOTAL}		–	585	–	
Snubber R_S Energy During Turn-on	E_{RS_ON}		–	4.3	–	
Snubber R_S Energy During Turn-off	E_{RS_OFF}		–	3.8	–	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 800 V, I_D = 20 A, Gate Driver = −5 V to +15 V, Turn-on $R_{G,EXT}$ = 1 Ω, Turn-off $R_{G,EXT}$ = 22 Ω, Inductive Load, FWD: Same Device With V_{GS} = −5 V, R_G = 22 Ω, RC Snubber: R_S = 5 Ω, C_S = 150 pF, T_J = 150 °C	–	26	–	ns
Rise Time	t_r		–	16	–	
Turn-off Delay Time	$t_{d(off)}$		–	58	–	
Fall Time	t_f		–	19	–	
Turn-on Energy Including R_S Energy (Note 6)	E_{ON}		–	482	–	μJ
Turn-off Energy Including R_S Energy (Note 6)	E_{OFF}		–	87	–	
Total Switching Energy Including R_S Energy (Note 6)	E_{TOTAL}		–	569	–	
Snubber R_S Energy During Turn-on	E_{RS_ON}		–	4.1	–	
Snubber R_S Energy During Turn-off	E_{RS_OFF}		–	3.8	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Limited by $T_{J,max}$
5. Pulse width t_p limited by $T_{J,max}$
6. The switching performance are evaluated with a RC snubber circuit as shown in Figure 29.

TYPICAL PERFORMANCE DIAGRAMS

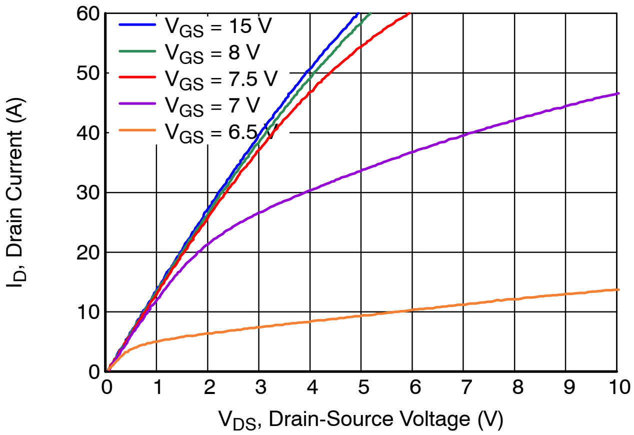


Figure 1. Typical Output Characteristics at T_J = −55 °C, t_p < 250 μs

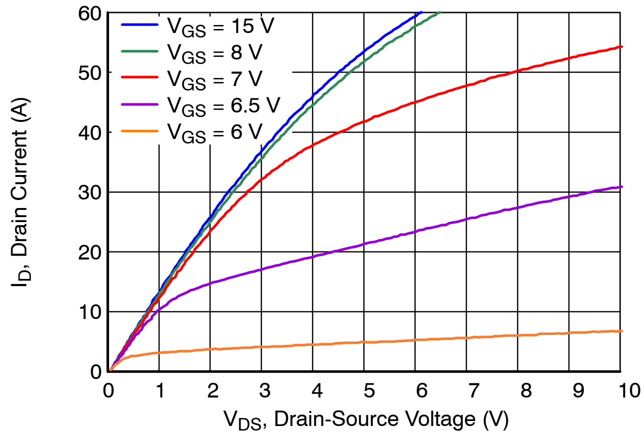


Figure 2. Typical Output Characteristics at T_J = 25 °C, t_p < 250 μs

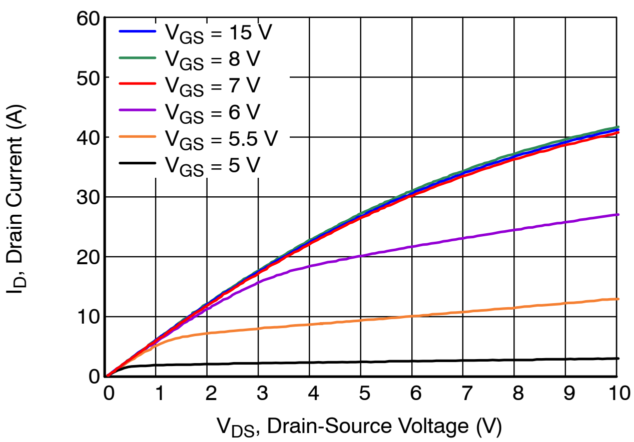


Figure 3. Typical Output Characteristics at T_J = 175 °C, t_p < 250 μs

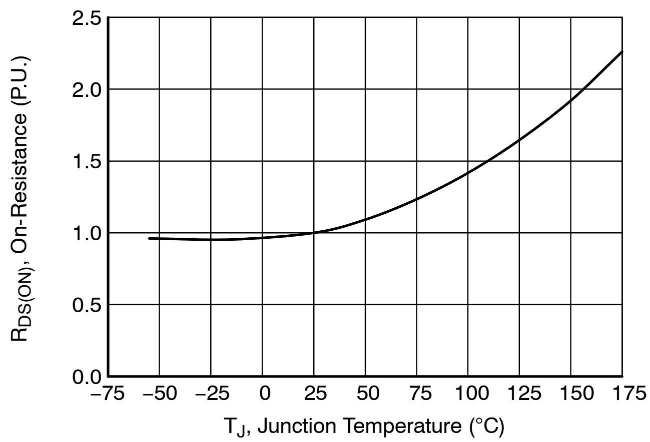


Figure 4. Normalized On-Resistance vs. Temperature at V_{GS} = 12 V and I_D = 20 A

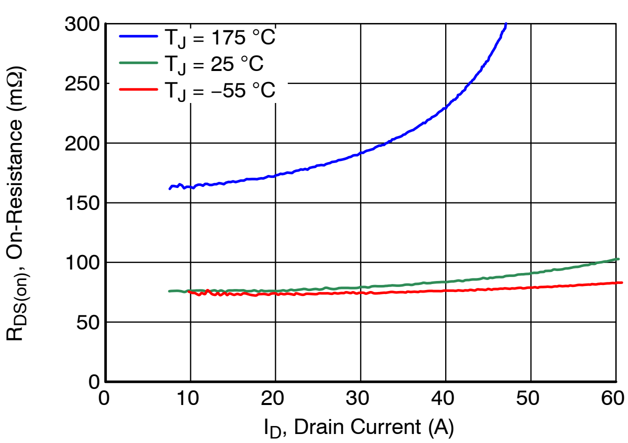


Figure 5. Typical Drain-Source On-Resistances at V_{GS} = 12 V

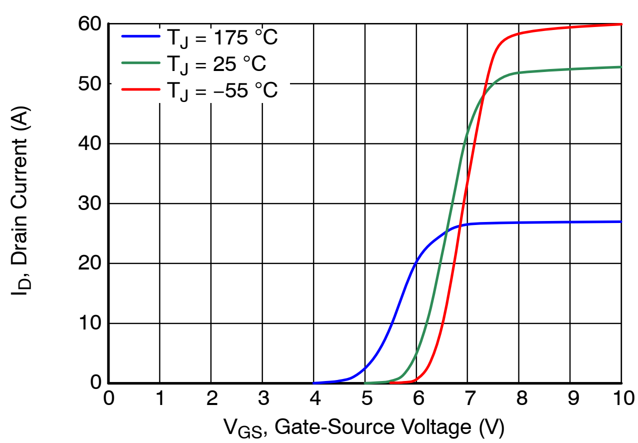


Figure 6. Typical Transfer Characteristics at V_{DS} = 5 V

TYPICAL PERFORMANCE DIAGRAMS (continued)

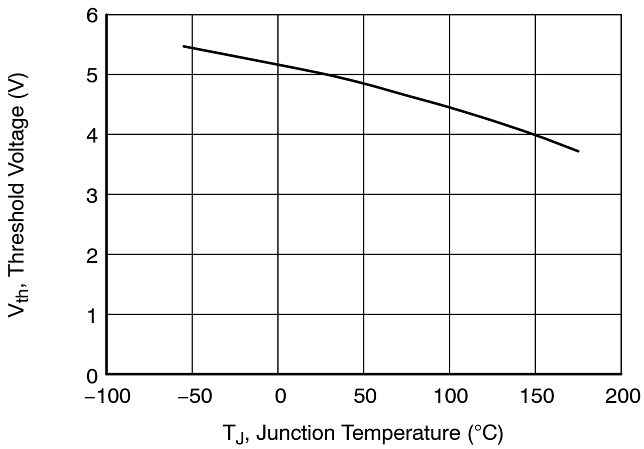


Figure 7. Threshold Voltage vs. Junction Temperature at V_{DS} = 5 V and I_D = 10 mA

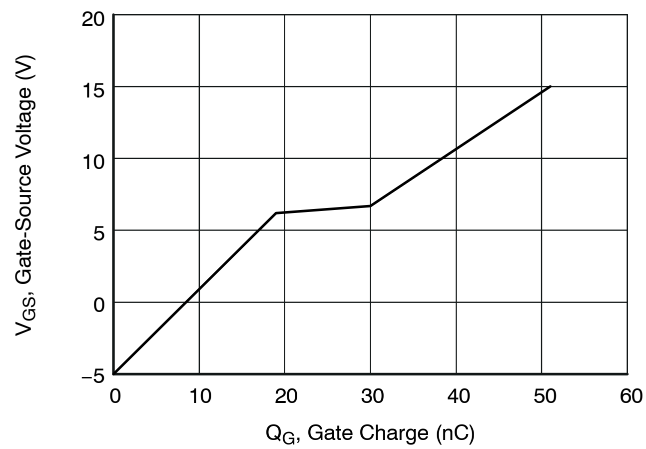


Figure 8. Typical Gate Charge at V_{DS} = 800 V and I_D = 20 A

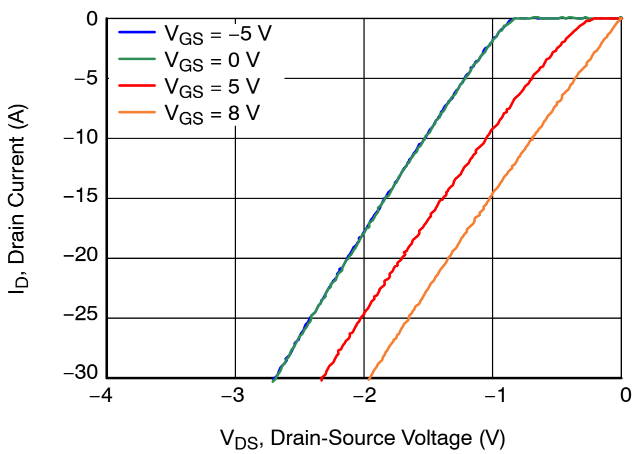


Figure 9. 3rd Quadrant Characteristics at T_J = −55 °C

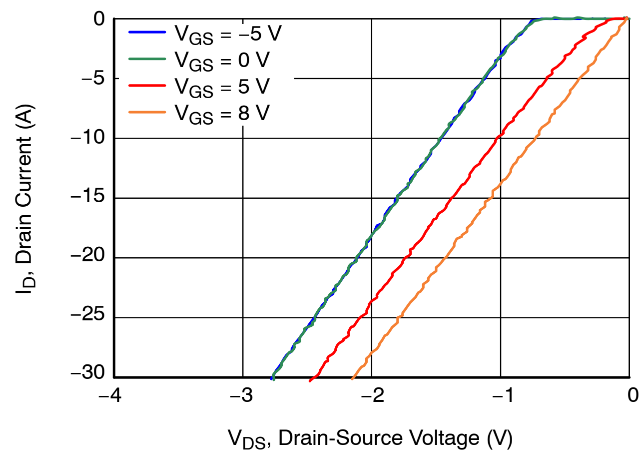


Figure 10. 3rd Quadrant Characteristics at T_J = 25 °C

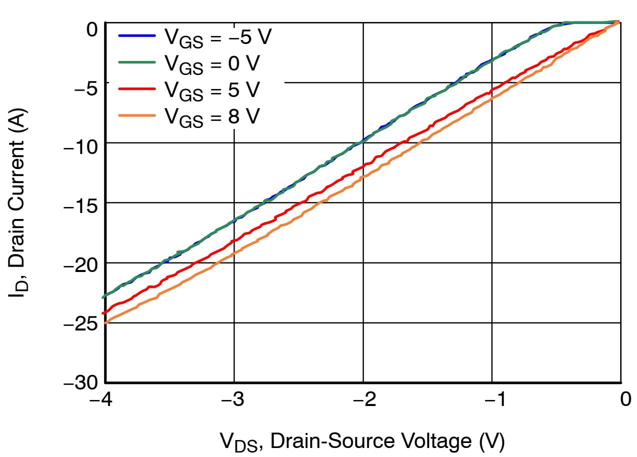


Figure 11. 3rd Quadrant Characteristics at T_J = 175 °C

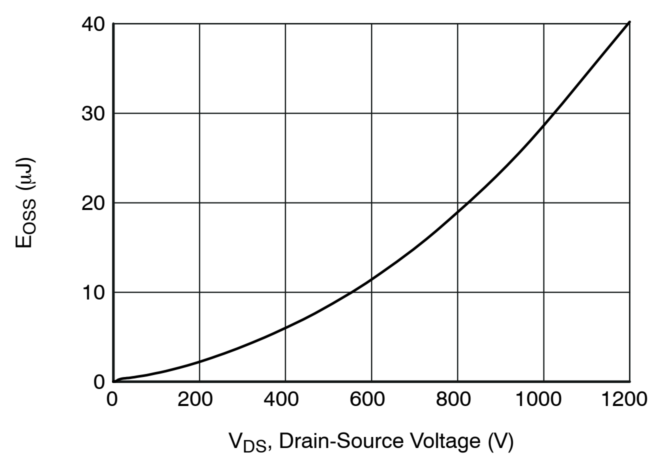


Figure 12. Typical Stored Energy in C_{OSS} at V_{GS} = 0 V

TYPICAL PERFORMANCE DIAGRAMS (continued)

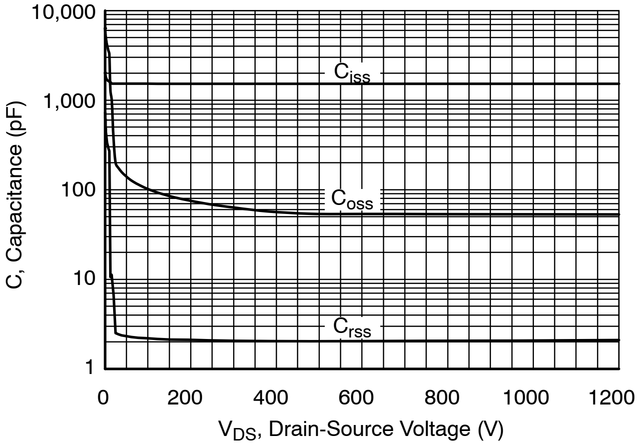


Figure 13. Typical Capacitances at f = 100 kHz and V_{GS} = 0 V

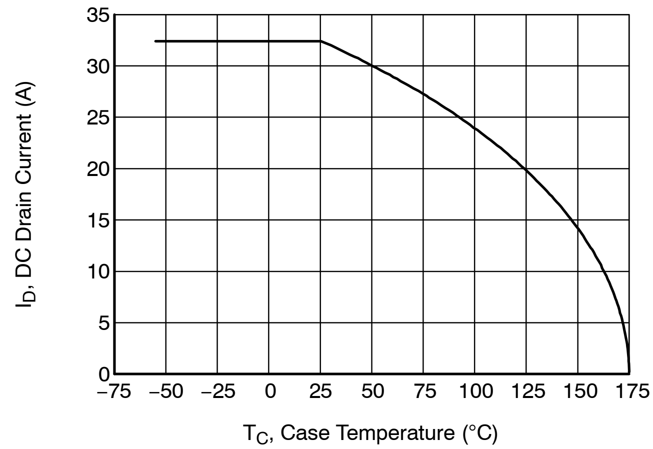


Figure 14. DC Drain Current Derating

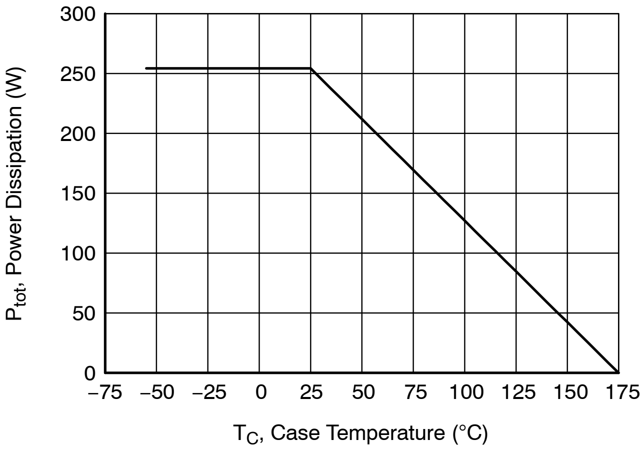


Figure 15. Total Power Dissipation

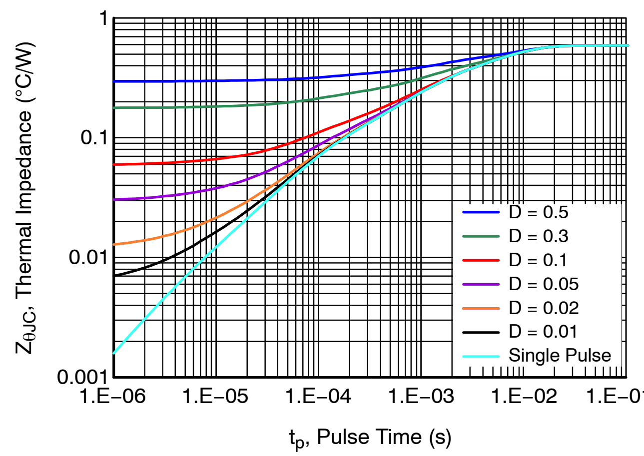


Figure 16. Maximum Transient Thermal Impedance

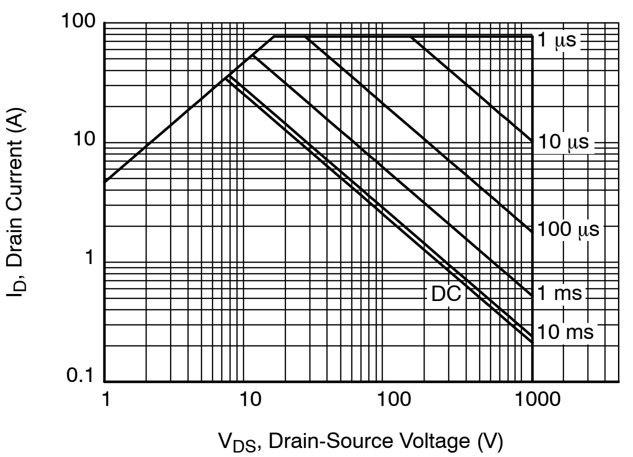


Figure 17. Safe Operation Area at T_C = 25 °C, D = 0, Parameter t_p

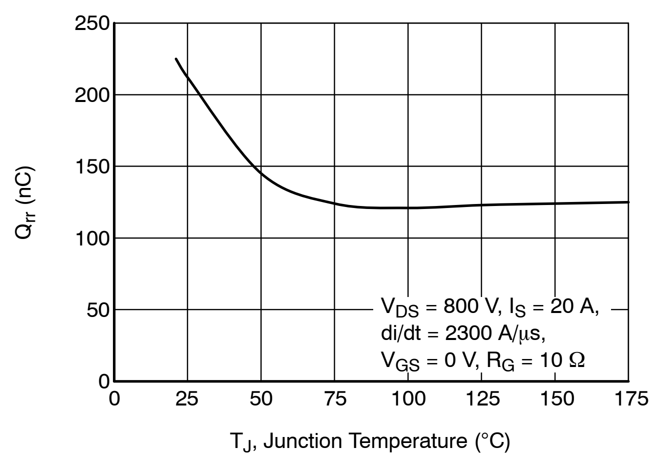


Figure 18. Reverse Recovery Charge Q_{rr} vs. Junction Temperature

TYPICAL PERFORMANCE DIAGRAMS (continued)

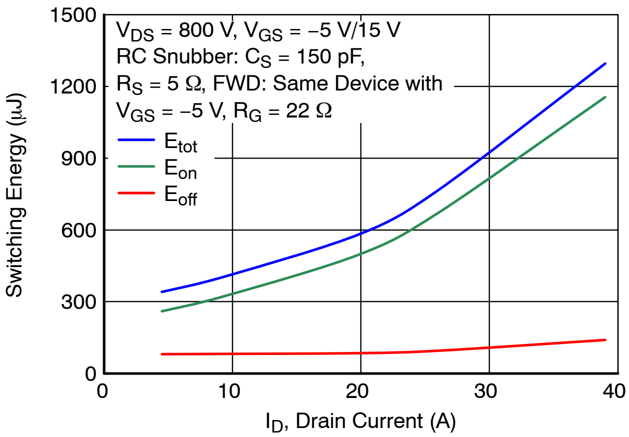


Figure 19. Clamped Inductive Switching Energy vs. Drain Current at T_J = 25 °C, Turn-on R_{G_EXT} = 1 Ω, and Turn-off R_{G_EXT} = 22 Ω

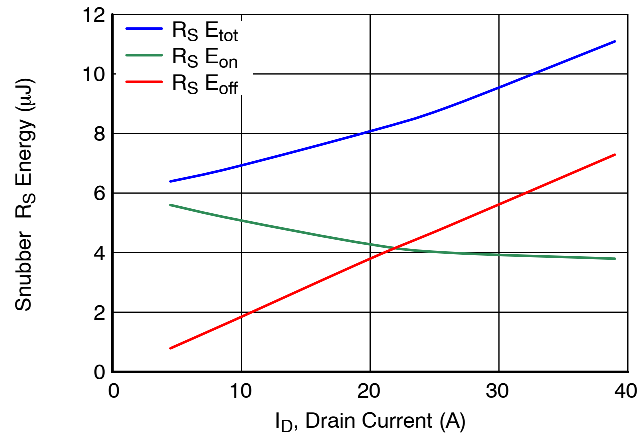


Figure 20. RC Snubber Energy Loss vs. Drain Current at the Test Conditions Shown in Figure 19

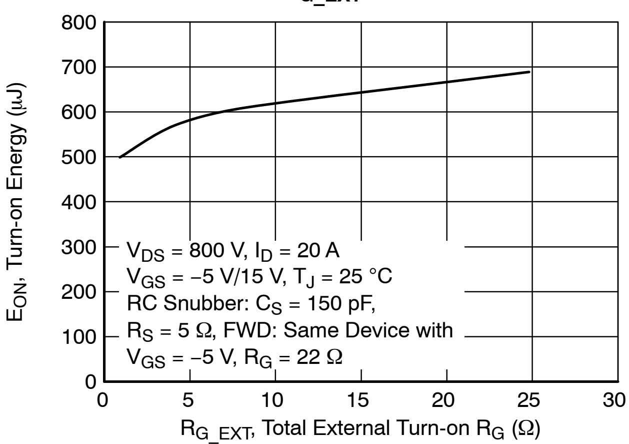


Figure 21. Clamped Inductive Switching Turn-on Energy Including RC Snubber Energy Loss as a Function of Total External Turn-on Gate Resistor R_{G_EXT}

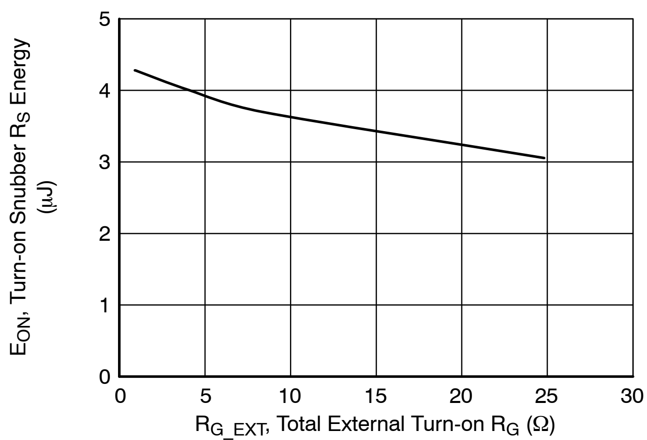


Figure 22. RC Snubber Energy Loss as a Function of Total External Turn-on Gate Resistor R_{G_EXT} at the Test Conditions Shown in Figure 21

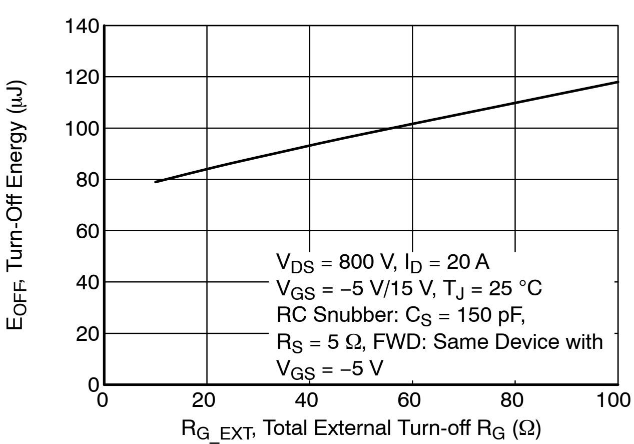


Figure 23. Clamped Inductive Switching Turn-off Energy Including RC Snubber Energy Loss as a Function of Total External Turn-off Gate Resistor R_{G_EXT}

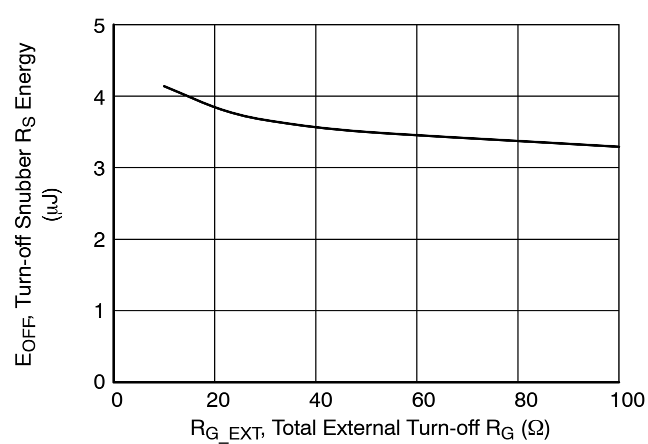


Figure 24. RC Snubber Energy Loss as a Function of Total External Turn-off Gate Resistor R_{G_EXT} at the Test Conditions Shown in Figure 23

TYPICAL PERFORMANCE DIAGRAMS (continued)

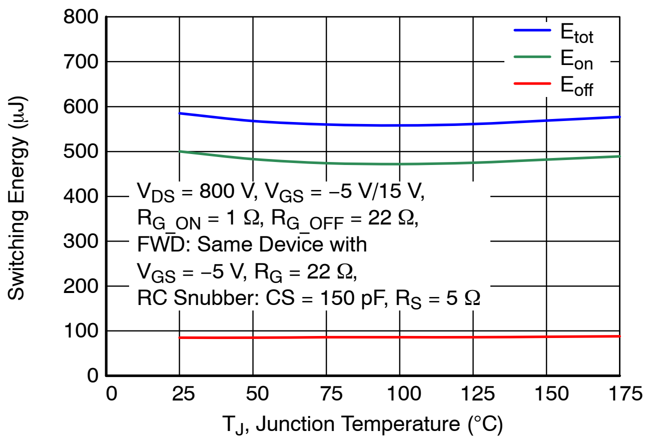


Figure 25. Clamped Inductive Switching Energy Including RC Snubber Energy Loss as a Function of Junction Temperature at I_D = 20 A

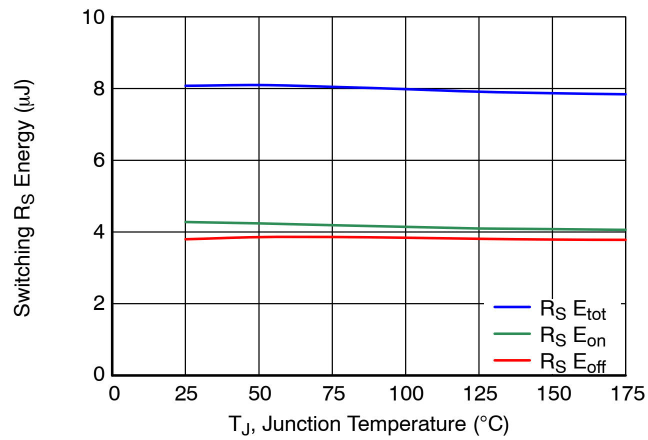


Figure 26. RC Snubber Energy Loss as a Function of Junction Temperature at the Test Conditions Shown in Figure 25

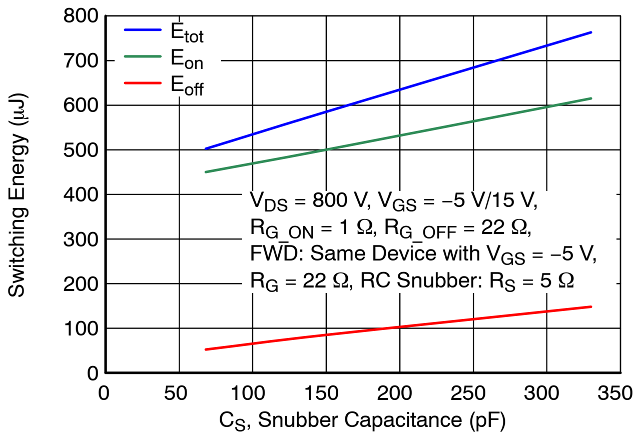


Figure 27. Clamped Inductive Switching Energy Including RC Snubber Energy Loss as a Function of Snubber Capacitance at I_D = 20 A and T_J = 25 °C

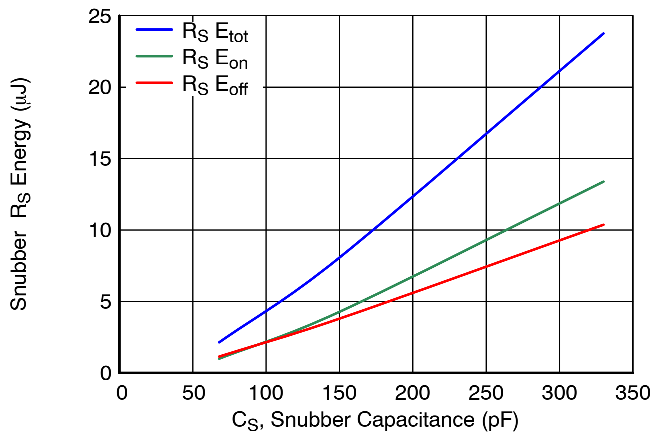


Figure 28. RC Snubber Energy Loss as a Function of Snubber Capacitance at the Test Conditions Shown in Figure 27

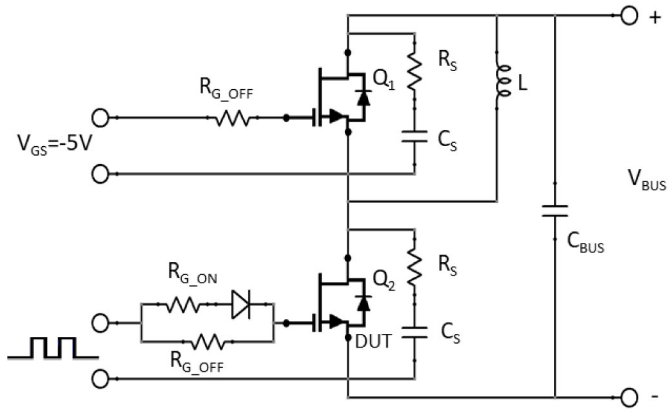


Figure 29. Clamped Inductive Load Switching Test Circuit An RC Snubber (RS = 5 Ω and CS = 150 pF) is Required to Improve the Turn-off Waveforms

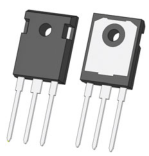
APPLICATIONS INFORMATION

SiC cascodes are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_g), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC cascodes also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.onsemi.com.

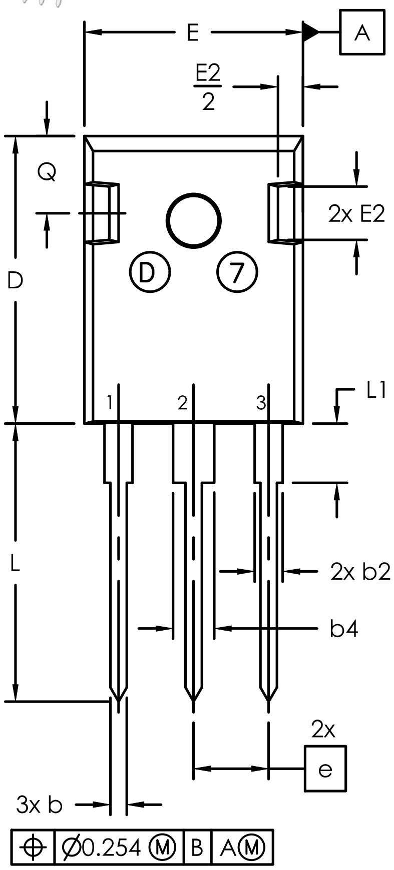
ORDERING INFORMATION

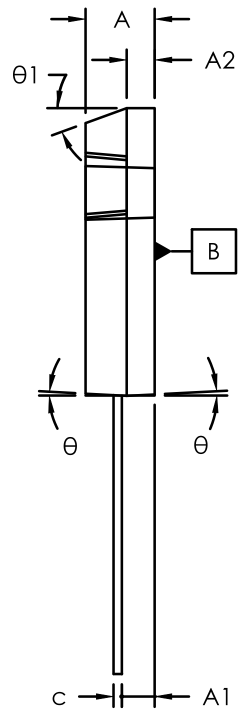
Part Number	Marking	Package	Shipping
UF3C120080K3S	UF3C120080K3S	TO247-3 (Pb-Free, Halogen Free)	600 / Tube

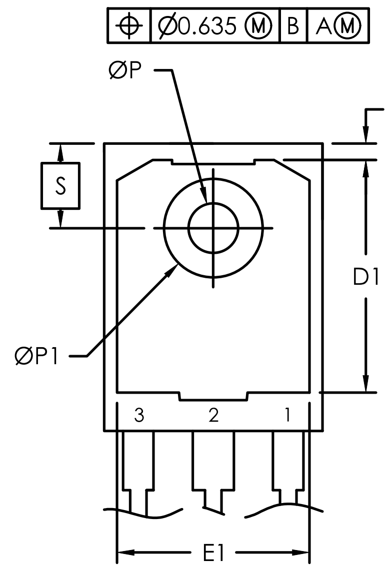


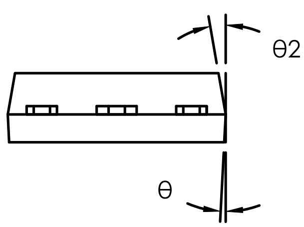
TO247−3 15.90x20.96x5.03, 5.44P
CASE 340AK
ISSUE A

DATE 12 FEB 2025









SYM	millimeters		
	MIN	NOM	MAX
A	4.70	5.03	5.31
A1	2.21	2.40	2.59
A2	1.50	2.03	2.49
b	0.99	1.20	1.40
b2	1.65	2.03	2.39
b4	2.59	3.00	3.43
c	0.38	0.60	0.89
D	20.70	20.96	21.46
D1	13.08	–	–
D2	0.51	1.19	1.35
E	15.49	15.90	16.26
e	5.44 BSC		
E1	13.00	14.02	13.60
E2	3.43	3.89	5.20
L	19.62	20.27	20.32
L1	–	–	4.50
ØP	3.40	3.60	3.80
ØP1	7.06	7.19	7.39
Q	5.38	5.62	6.20
S	6.15 BSC		
θ	3°		
θ1	20°		
θ2	10°		

NOTE:
1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Package Outline in compliance with JEDEC standard var. AD.
4. Dimensions D & E does not include mold flash.
5. ØP to have max draft angle of 1.7° to the top with max. hole diameter of 3.91mm.

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