LDO Regulator - 1 A, Ultra Low Dropout, CMOS, with Bias Rail

Product Preview

T30LMPSR131, T30LAPSR131

The T30LxPSR131 is a 1 A LDO equipped with an NMOS pass transistor and a separate bias supply voltage (V_{BIAS}). The T30LxPSR131 offers ultra-fast dynamic response and provides very stable output voltage with 1% accuracy over full temperature range. To optimize performance for battery operated portable applications, the T30LxPSR131 features an ultra-low bias current consumption. The device also features high PSRR across frequency range and ultra-low noise optimized for noise sensitive applications. The WLCSP6 1.145 mm x 0.75 mm, 0.4 mm pitch Chip Scale package is optimized for use in space constrained applications.

Features

- Best-in-Class Dropout: 25 mV (typ.) at 1 A
- ±1% Accuracy over −40 °C to 125 °C Temperature Range
- Ultra Low Bias Input Current of Typ. 85 μA
- Low Noise, 7.5 μV_{RMS} Typ.
- High PSRR across Frequency Range
  - 75 dB at 1 kHz
  - 34 dB at 100 kHz
- Input Voltage Range: up to 2.2 V
- Bias Voltage Range: up to 3.3 V
- Output Voltage Range: 0.5 V to 1.8 V (Fixed), Resolution 25 mV
- Excellent Load Transient Performance
- 1.2 V Logic Level Enable Input Compatibility
- Normal and Slow Turn-On Options Available
- Output Active Discharge Option Available

Typical Applications

- Battery-powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

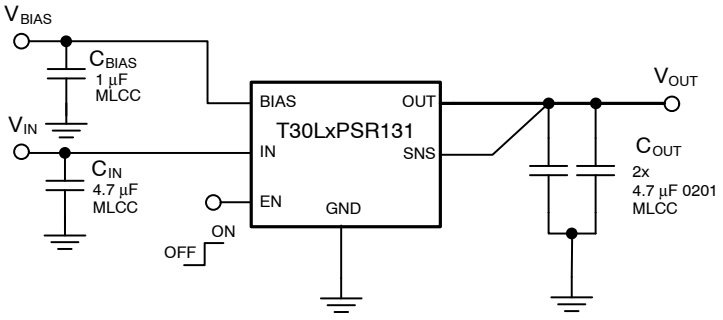
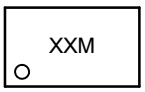


Figure 1. Application Schematic

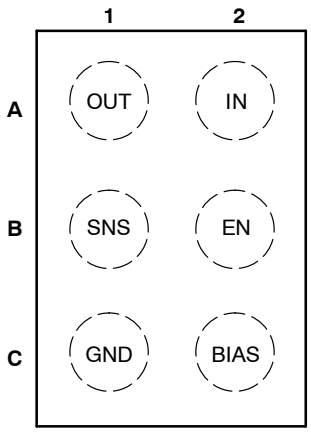
WLCSP6
1.145x0.75x0.33
CASE 567YX

MARKING DIAGRAM



XX = Specific Device Code
M = Month Code

PIN CONNECTIONS

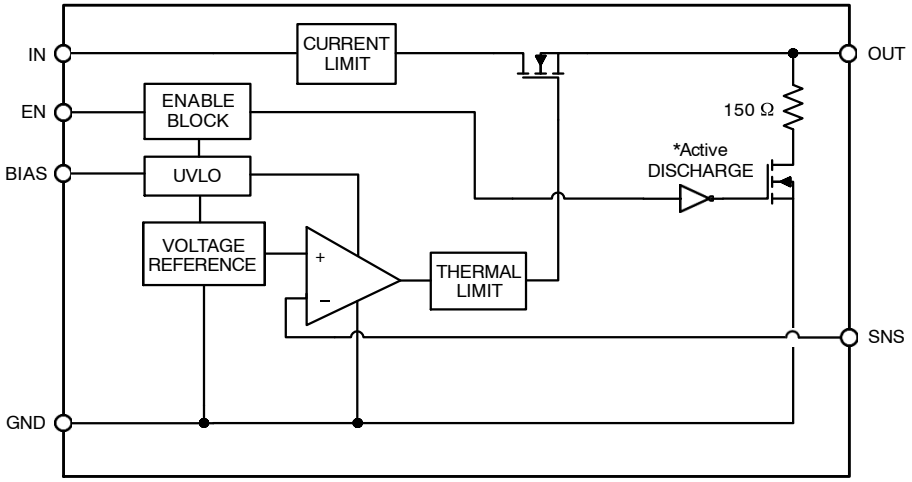


Top View

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.



*Active output discharge function is present only in “A” and “C” option devices.

Figure 2. Simplified Schematic Block Diagram - Fixed Version

PIN FUNCTION DESCRIPTION

Pin No. WLCSP6	Pin Name	Description
A1	OUT	Regulated Output Voltage pin
A2	IN	Input Voltage Supply pin
B1	SNS	Output voltage Sensing Input. Connect to Output on the PCB to output the voltage corresponding to the part version.
B2	EN	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode.
C1	GND	Ground pin
C2	BIAS	Bias voltage supply for internal control circuits.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 2.5	V
Output Voltage	V_{OUT}	−0.3 to (V_{IN} + 0.3) ≤ 2.5	V
Chip Enable, Bias and SNS Input	V_{EN}, V_{BIAS}, V_{SNS}	−0.3 to 3.6	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	750	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22-A114
   ESD Charged Device Model tested per JS-002-2018
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, WLCSP6 1.145 mm x 0.75 mm Thermal Resistance, Junction-to-Air (Note 3)	$R_{\theta JA}$	69	°C/W

3. This junction-to-ambient thermal resistance under natural convection was derived by thermal simulations based on the JEDEC JESD51 series standards methodology. Only a single device mounted at the center of a high_K (2s2p) 80 mm x 80 mm multilayer board with 1-ounce internal planes and 2-ounce copper on top and bottom. Top copper layer has a dedicated 1.6 mm2 copper area.

ELECTRICAL CHARACTERISTICS

(−40 °C ≤ T_J ≤ 125 °C; V_{BIAS} = 2.7 V or (V_{OUT} + 1.6 V), whichever is greater, V_{IN} = $V_{OUT(NOM)}$ + 0.1 V, I_{OUT} = 1 mA, V_{EN} = 1 V, C_{IN} = 4.7 μF, C_{OUT} = 10 μF, C_{BIAS} = 1 μF, unless otherwise noted.
Typical values are at T_J = +25 °C. Min/Max values are for −40 °C ≤ T_J ≤ 125 °C unless otherwise noted. (Note 4))

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage Range			V_{IN}	V_{OUT} + V_{DO}		2.2	V
Operating Bias Voltage Range			V_{BIAS}	(V_{OUT} + 1.50) ≥ 2.5		3.3	V
Undervoltage Lock-out	V_{BIAS} Rising Hysteresis		$UVLO_{(BIAS)}$		2.1 0.1		V
	V_{IN} Rising Hysteresis		$UVLO_{(IN)}$		0.8 x V_{OUT} 0.1		V
Output Voltage Accuracy	−40 °C ≤ T_J ≤ 85 °C, $V_{OUT(NOM)}$ + 0.1 V ≤ V_{IN} ≤ $V_{OUT(NOM)}$ + 1.0 V, 2.7 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is greater < V_{BIAS} < 3.3 V, 1 mA < I_{OUT} < 1 A		V_{OUT}	−0.8		+0.8	%
Output Voltage Accuracy	−40 °C ≤ T_J ≤ 125 °C, $V_{OUT(NOM)}$ + 0.1 V ≤ V_{IN} ≤ $V_{OUT(NOM)}$ + 1.0 V, 2.7 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is greater < V_{BIAS} < 3.3 V, 1 mA < I_{OUT} < 1 A			−1.0		+1.0	%
V_{IN} Line Regulation	$V_{OUT(NOM)}$ + 0.1 V ≤ V_{IN} ≤ 2.2 V		$Line_{Reg}$		0.01		%/V
V_{BIAS} Line Regulation	2.7 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is greater < V_{BIAS} < 3.3 V		$Line_{Reg}$		0.01		%/V
Load Regulation	I_{OUT} = 1 mA to 1 A		$Load_{Reg}$		1		mV
V_{IN} Dropout Voltage	I_{OUT} = 1 A (Note 5)		V_{DO}		25	60	mV
V_{BIAS} Dropout Voltage	I_{OUT} = 1 A, V_{IN} = V_{BIAS} (Notes 5, 6)		V_{DO}		1.1	1.5	V
Output Current Limit	V_{OUT} = 90% $V_{OUT(NOM)}$		I_{CL}	1250	1650	2000	mA
SNS Pin Operating Current			I_{SNS}		0.1	0.5	μA
Bias Pin Quiescent Current	V_{BIAS} = 3.3 V, I_{OUT} = 0 mA		I_{BIASQ}		85	130	μA
Bias Pin Disable Current	V_{EN} ≤ 0.325 V		$I_{BIAS(DIS)}$		0.5	TBD	μA
Input Pin Disable Current			$I_{VIN(DIS)}$		0.5	TBD	μA
EN Pin Threshold Voltage	EN Input Voltage “H”		$V_{EN(H)}$	0.825			V
	EN Input Voltage “L”		$V_{EN(L)}$			0.325	
EN Pull Down Current	V_{EN} = 3.3 V		I_{EN}		0.3	TBD	μA
Power Supply Rejection Ratio	V_{IN} to V_{OUT}, V_{IN} = V_{OUT} + 0.1 V, I_{OUT} = 450 mA, C_{OUT} = 2 x 4.7 μF 0201	f = 100 Hz	PSRR(V_{IN})		73		dB
		f = 1 kHz			73		
		f = 10 kHz			50		
		f = 100 kHz			33		
	V_{BIAS} to V_{OUT}, V_{IN} = V_{OUT} + 0.1 V	f = 1 kHz	PSRR(V_{BIAS})		80		dB
Output Noise Voltage	V_{IN} = V_{OUT} + 0.1 V, f = 10 Hz to 100 kHz	I_{OUT} = 10 mA	V_N		10		μV_{RMS}
		I_{OUT} = 1 A			7.5		
Thermal Shutdown Threshold	Temperature increasing				160		°C
	Temperature decreasing				140		

ELECTRICAL CHARACTERISTICS (continued)
($-40\ ^\circ C \le T_J \le 125\ ^\circ C$; V_{BIAS} = 2.7 V or (V_{OUT} + 1.6 V), whichever is greater, $V_{IN} = V_{OUT(NOM)}$ + 0.1 V, I_{OUT} = 1 mA, V_{EN} = 1 V, C_{IN} = 4.7 μF, C_{OUT} = 10 μF, C_{BIAS} = 1 μF, unless otherwise noted.
Typical values are at $T_J = +25\ ^\circ C$. Min/Max values are for $-40\ ^\circ C \le T_J \le 125\ ^\circ C$ unless otherwise noted. (Note 4))

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Output Discharge Pull-Down	$V_{EN} \le 0.325$ V, V_{OUT} = 0.5 V, Active Discharge Version Only		R_{DISCH}		150		Ω
Delay time	From assertion of V_{EN} to output voltage increase	"A" option	t_{DELAY}		120		μs
		"C" option			120		
Rise time	V_{OUT} rise from 10% to 90% $V_{OUT(NOM)}$	"A" option	t_{RISE}		21		
		"C" option			100		
Turn-On Time	From assertion of V_{EN} to V_{OUT} = 98% $V_{OUT(NOM)}$	"A" option	t_{ON}		140		
		"C" option			220		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_A = 25\ ^\circ C$. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(NOM)}$.
6. For fixed output voltages below 1.5 V, V_{BIAS} dropout does not apply due to a minimum Bias operating voltage of 2.5 V.

ORDERING INFORMATION

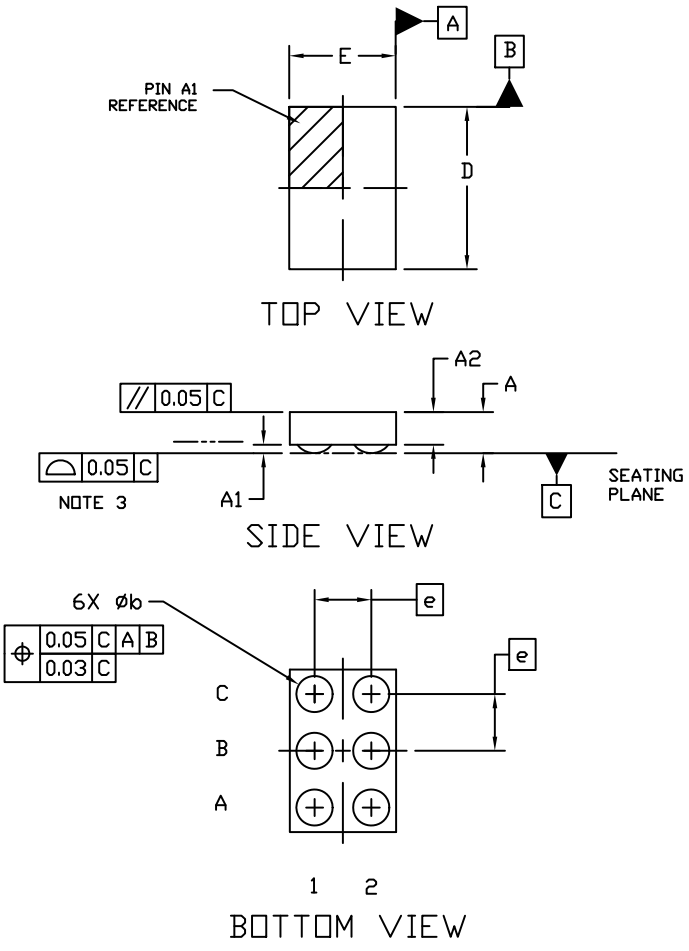
Device	Nominal Output Voltage	Marking	Option	Package	Shipping†
T30LMPSR131	TBD V	TBD	TBD	WLCSP6 Case 567YX (Pb-Free) UBM: 240 μm Bump Type: (98.2% Sn/1.8% Ag) Plate	10,000 / Tape & Reel
T30LAPSR131	TBD V	TBD			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

7. To order other package and voltage variants, please contact your **onsemi** sales representative.

WLCSP6 1.145x0.75x0.33
CASE 567YX
ISSUE O

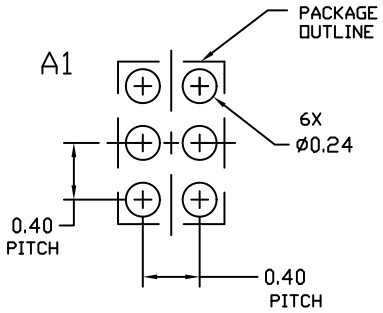
DATE 29 JAN 2020



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.

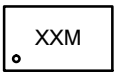
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	0.33
A1	0.04	0.06	0.08
A2	0.230 REF		
b	0.220	0.240	0.260
D	1.095	1.145	1.195
E	0.700	0.750	0.800
e	0.400 BSC		



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



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*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WLCSP6 1.145x0.75x0.33**	**PAGE 1 OF 1**

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