

# MOSFET - Power, Dual N-Channel

100 V, 26 mΩ, 28 A

## NVMFD027N10MCL

### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- NVMFWD027N10MCL – Wettable Flank Products
- These Devices are Pb-Free, Halogen Free/BFR Free, Beryllium Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter  | Symbol   | Value                     | Unit             |   |
|--|--|---------------------------|------------------|---|
| Drain-to-Source Voltage  | $V_{DSS}$                                      | 100                       | V                |   |
| Gate-to-Source Voltage   | $V_{GS}$                                       | $\pm 20$                  | V                |   |
| Continuous Drain Current $R_{\theta JC}$ (Note 1)                                  | Steady State                                   | $T_C = 25^\circ\text{C}$  | $I_D$ 28         | A |
|  |  | $T_C = 100^\circ\text{C}$ | 20               |   |
| Power Dissipation $R_{\theta JC}$ (Note 1)   | Steady State                                   | $T_C = 25^\circ\text{C}$  | $P_D$ 46         | W |
|  |  | $T_C = 100^\circ\text{C}$ | 23               |   |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)                              | Steady State                                   | $T_A = 25^\circ\text{C}$  | $I_D$ 7.4        | A |
|  |  | $T_A = 100^\circ\text{C}$ | 5.2              |   |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 2)                                     | Steady State                                   | $T_A = 25^\circ\text{C}$  | $P_D$ 3.1        | W |
|  |  | $T_A = 100^\circ\text{C}$ | 1.6              |   |
| Pulsed Drain Current   | $T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$ | $I_{DM}$ 115              | A                |   |
| Operating Junction and Storage Temperature Range                                   | $T_J, T_{stg}$                                 | -55 to +175               | $^\circ\text{C}$ |   |
| Source Current (Body Diode)  | $I_S$  | 35                        | A                |   |
| Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 1.3 \text{ A}$ )      | $E_{AS}$                                       | 154                       | mJ               |   |
| Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s) | $T_L$  | 260                       | $^\circ\text{C}$ |   |

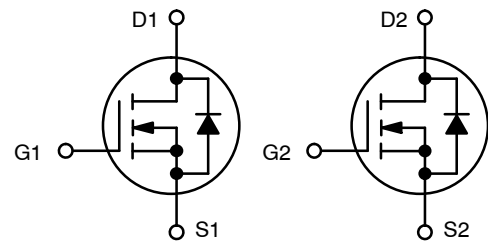
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE RATINGS

| Parameter                                   | Symbol          | Value | Unit                      |
|---|-----------------|-------|---------------------------|
| Junction-to-Case – Steady State (Note 1)    | $R_{\theta JC}$ | 3.29  | $^\circ\text{C}/\text{W}$ |
| Junction-to-Ambient – Steady State (Note 2) | $R_{\theta JA}$ | 48    |                           |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using 1 in<sup>2</sup> pad size, 2 oz. Cu pad.

| $V_{(BR)DSS}$ | $R_{DS(ON) MAX}$ | $I_D MAX$ |
|---------------|------------------|-----------|
| 100 V         | 26 mΩ @ 10 V     | 28 A      |
|               | 35 mΩ @ 4.5 V    |           |

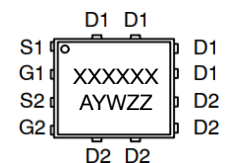


DUAL N-CHANNEL



DFN8 5x6 (SO8FL) CASE 506BT

### MARKING DIAGRAM



XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 W = Work Week  
 ZZ = Lot Traceability

### ORDERING INFORMATION

| Device                               | Package        | Shipping†          |
|--------------------------------------|----------------|--------------------|
| NVMFD027N10MCLT1G                    | DFN8 (Pb-Free) | 1500 / Tape & Reel |
| NVMFWD027N10MCLT1G (Wettable Flanks) |                |                    |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NVMFD027N10MCL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

### OFF CHARACTERISTICS

|   |                                      |   |                        |    |     |       |
|---|--------------------------------------|---|------------------------|----|-----|-------|
| Drain-to-Source Breakdown Voltage                         | V <sub>(BR)DSS</sub>                 | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA    | 100                    |    |     | V     |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | V <sub>(BR)DSS</sub> /T <sub>J</sub> |   |                        | 50 |     | mV/°C |
| Zero Gate Voltage Drain Current                           | I <sub>DSS</sub>                     | V <sub>GS</sub> = 0 V,<br>V <sub>DS</sub> = 100 V | T <sub>J</sub> = 25°C  |    | 1.0 | μA    |
|   |                                      |   | T <sub>J</sub> = 125°C |    | 100 |       |
| Gate-to-Source Leakage Current                            | I <sub>GSS</sub>                     | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V     |                        |    | 100 | nA    |

### ON CHARACTERISTICS

|                                   |                                     |  |   |      |    |       |
|-----------------------------------|-------------------------------------|--|---|------|----|-------|
| Gate Threshold Voltage            | V <sub>GS(TH)</sub>                 | V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 38 μA | 1 |      | 3  | V     |
| Threshold Temperature Coefficient | V <sub>GS(TH)</sub> /T <sub>J</sub> |  |   | -5.4 |    | mV/°C |
| Drain-to-Source On Resistance     | R <sub>DS(on)</sub>                 | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7 A               |   | 21   | 26 | mΩ    |
|                                   |                                     | V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A              |   | 28   | 35 |       |
| Forward Transconductance          | g <sub>FS</sub>                     | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 7 A               |   | 27   |    | S     |

### CHARGES & CAPACITANCES

|                              |                     |   |  |     |  |    |
|------------------------------|---------------------|---|--|-----|--|----|
| Input Capacitance            | C <sub>ISS</sub>    | V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 50 V              |  | 720 |  | pF |
| Output Capacitance           | C <sub>OSS</sub>    |   |  | 300 |  |    |
| Reverse Transfer Capacitance | C <sub>RSS</sub>    |   |  | 6   |  |    |
| Total Gate Charge            | Q <sub>G(TOT)</sub> | V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 50 V, I <sub>D</sub> = 7 A |  | 5.5 |  | nC |
| Total Gate Charge            | Q <sub>G(TOT)</sub> | V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 50 V, I <sub>D</sub> = 7 A  |  | 11  |  |    |
| Threshold Gate Charge        | Q <sub>G(TH)</sub>  |   |  | 1.1 |  |    |
| Gate-to-Source Charge        | Q <sub>GS</sub>     |   |  | 2   |  |    |
| Gate-to-Drain Charge         | Q <sub>GD</sub>     |   |  | 1.4 |  |    |
| Plateau Voltage              | V <sub>GP</sub>     |   |  | 2.5 |  |    |

### SWITCHING CHARACTERISTICS (Note 3)

|                     |                     |   |  |     |  |    |
|---------------------|---------------------|---|--|-----|--|----|
| Turn-On Delay Time  | t <sub>d(ON)</sub>  | V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 50 V,<br>I <sub>D</sub> = 7 A, R <sub>G</sub> = 6 Ω |  | 7   |  | ns |
| Rise Time           | t <sub>r</sub>      |   |  | 2.5 |  |    |
| Turn-Off Delay Time | t <sub>d(OFF)</sub> |   |  | 19  |  |    |
| Fall Time           | t <sub>f</sub>      |   |  | 3.2 |  |    |

### DRAIN-SOURCE DIODE CHARACTERISTICS

|                         |                 |  |                        |      |      |     |   |
|-------------------------|-----------------|--|------------------------|------|------|-----|---|
| Forward Diode Voltage   | V <sub>SD</sub> | V <sub>GS</sub> = 0 V,<br>I <sub>S</sub> = 7 A                                 | T <sub>J</sub> = 25°C  |      | 0.84 | 1.3 | V |
|                         |                 |  | T <sub>J</sub> = 125°C |      | 0.73 |     |   |
| Reverse Recovery Time   | t <sub>RR</sub> | V <sub>GS</sub> = 0 V, di <sub>S</sub> /dt = 100 A/μs,<br>I <sub>S</sub> = 3 A |                        | 28   |      | ns  |   |
| Reverse Recovery Charge | Q <sub>RR</sub> |  |                        | 17   |      | nC  |   |
| Charge Time             | t <sub>a</sub>  |  |                        | 13.9 |      | ns  |   |
| Discharge Time          | t <sub>b</sub>  |  |                        | 14.2 |      | ns  |   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

# NVMFD027N10MCL

## TYPICAL CHARACTERISTICS

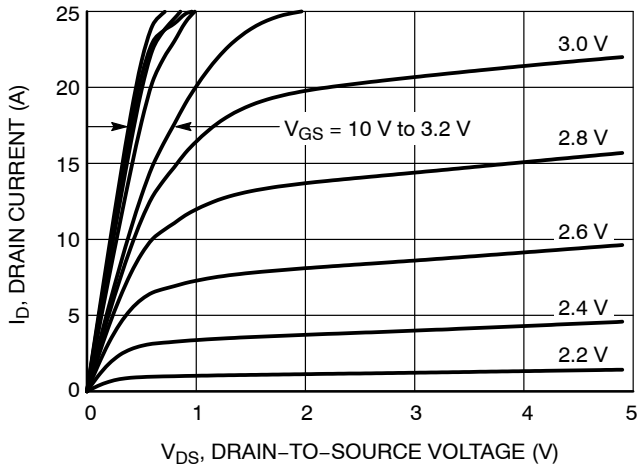


Figure 1. On-Region Characteristics

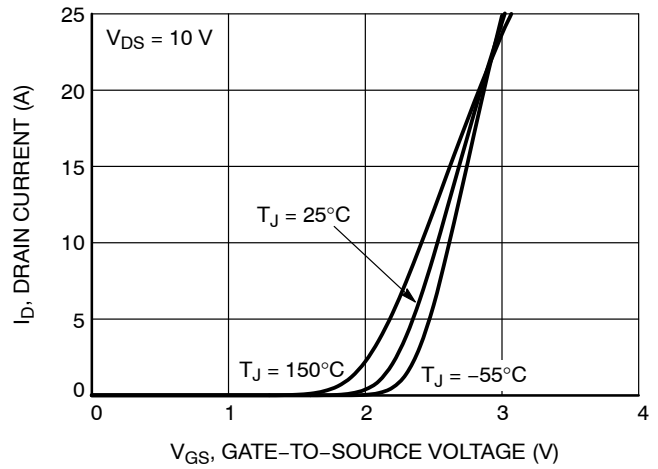


Figure 2. Transfer Characteristics

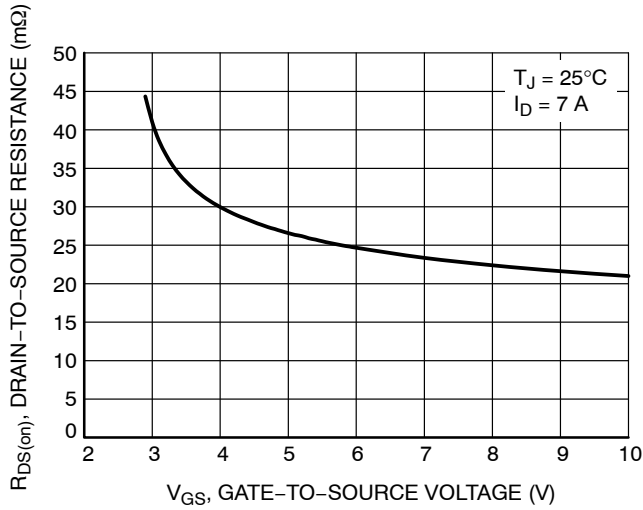


Figure 3. On-Resistance vs. Gate-to-Source Voltage

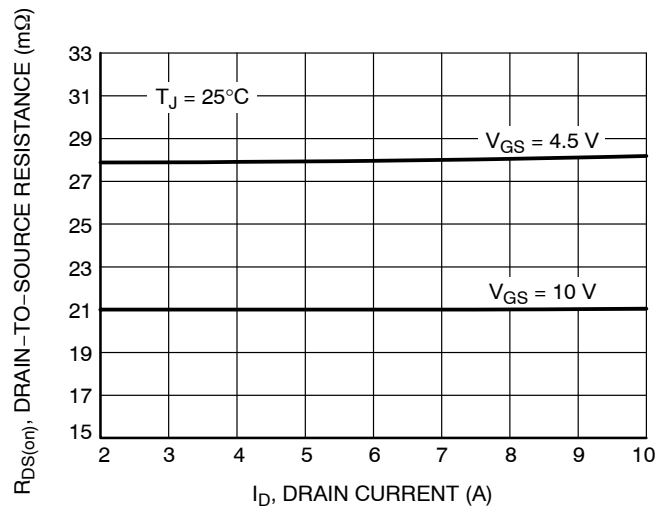


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

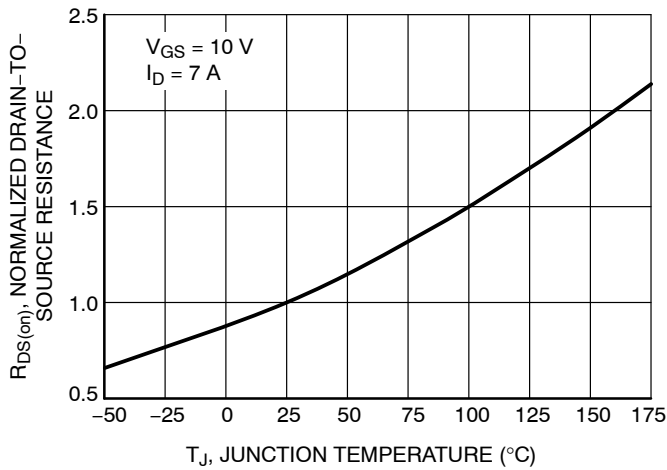


Figure 5. On-Resistance Variation with Temperature

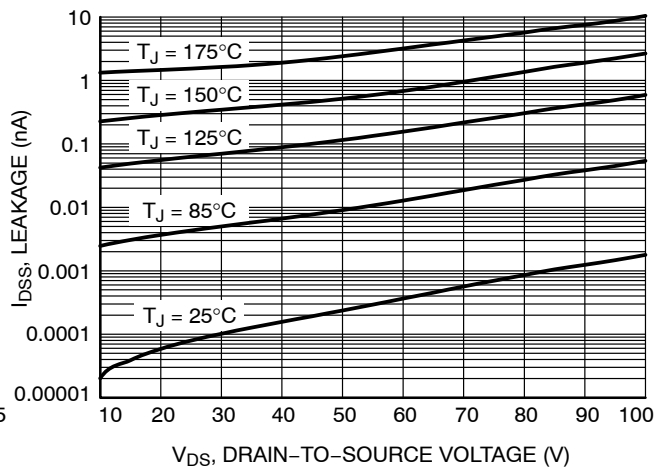


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NVMFD027N10MCL

## TYPICAL CHARACTERISTICS

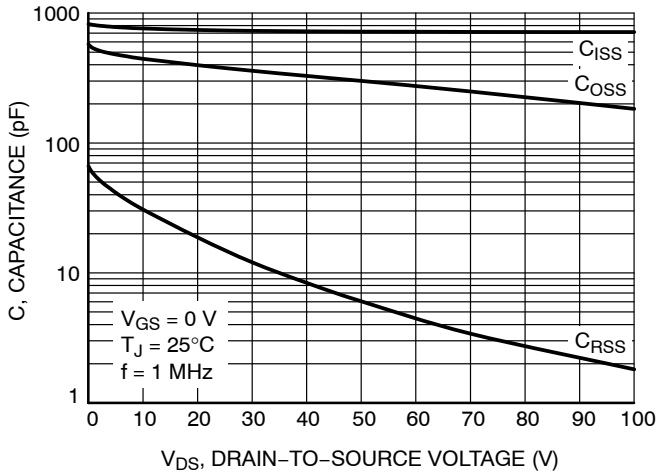


Figure 7. Capacitance Variation

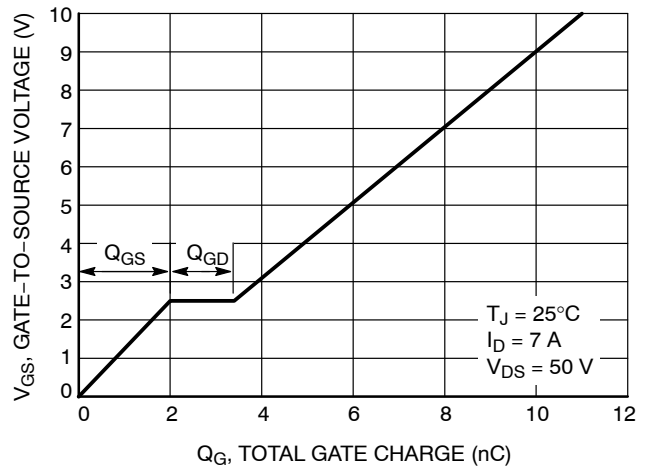


Figure 8. Gate-to-Source Voltage vs. Total Charge

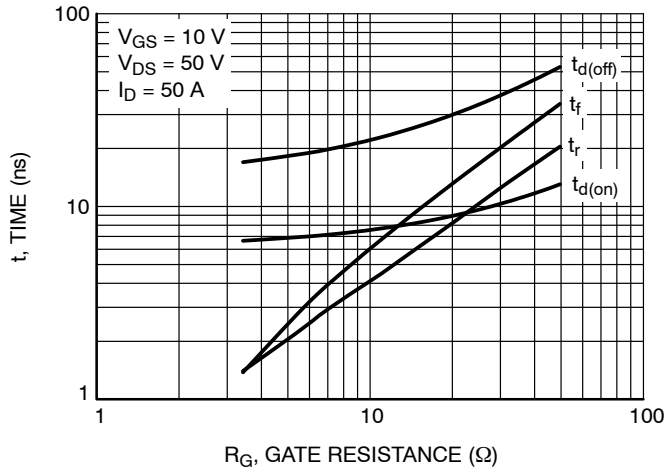


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

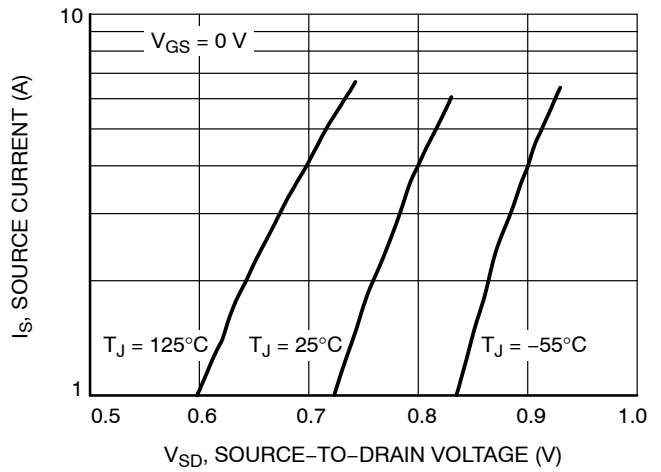


Figure 10. Diode Forward Voltage vs. Current

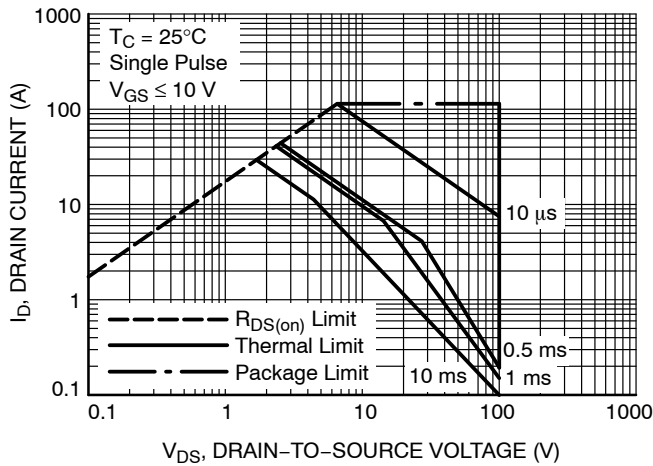


Figure 11. Maximum Rated Forward Biased Safe Operating Area

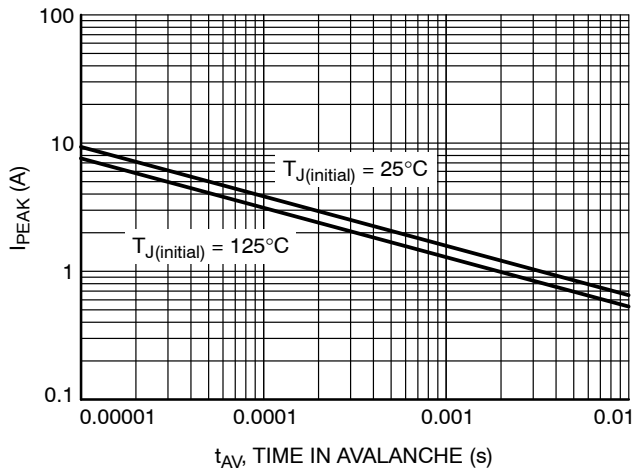


Figure 12. Maximum Drain Current vs. Time in Avalanche

# NVMFD027N10MCL

## TYPICAL CHARACTERISTICS

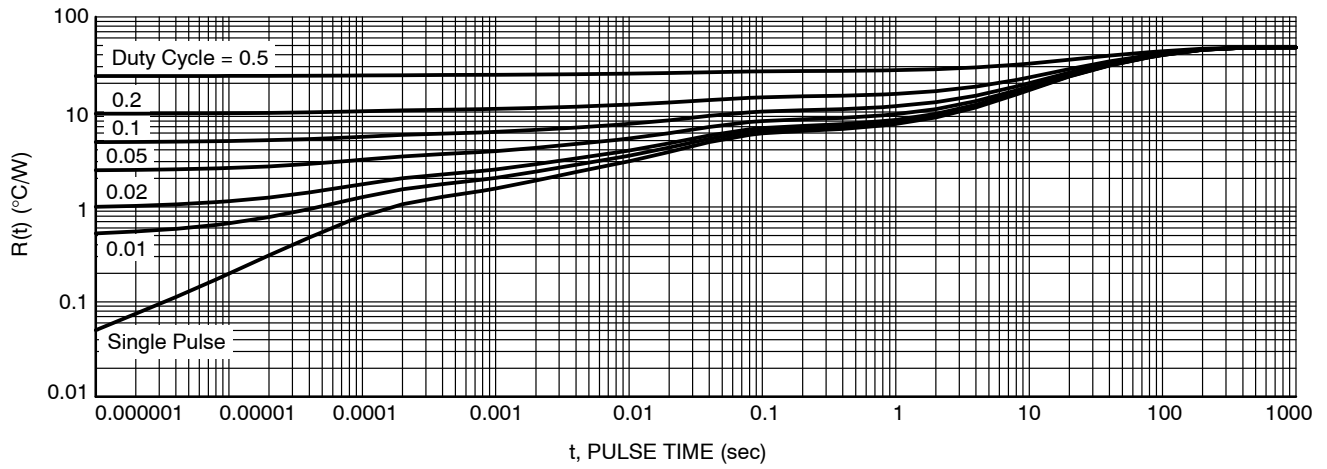
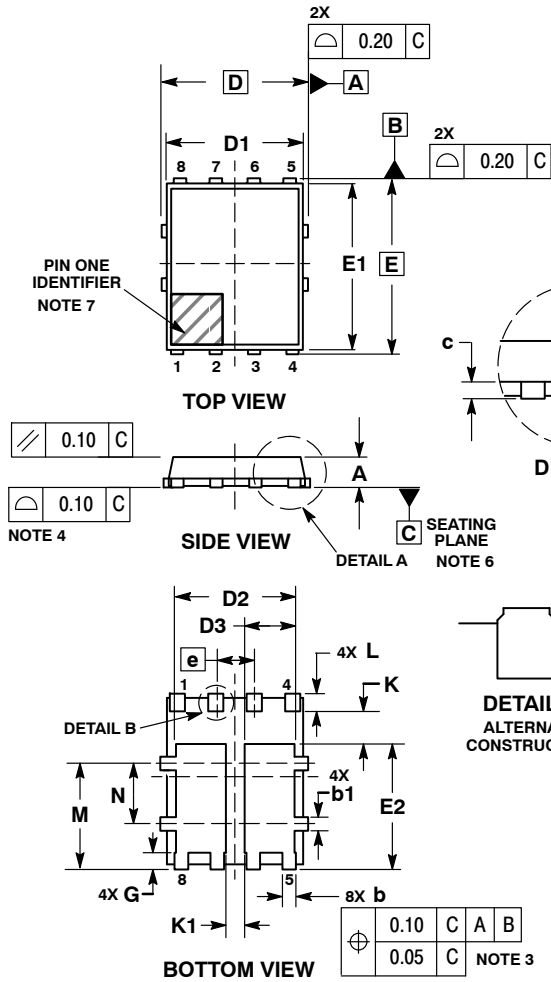


Figure 13. Transient Thermal Impedance

# NVMFD027N10MCL

## PACKAGE DIMENSIONS

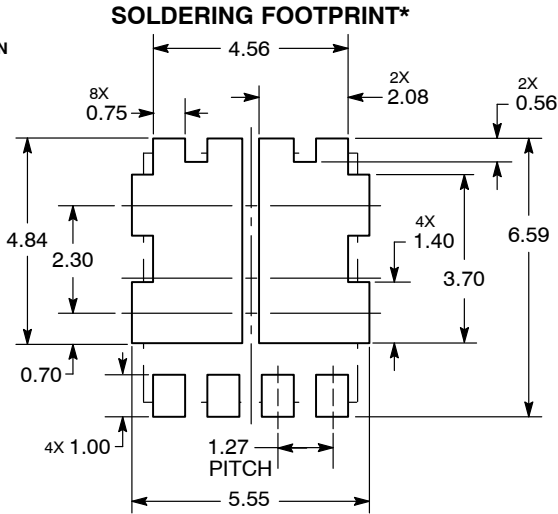
### DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual) CASE 506BT ISSUE E



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN         | MAX  | MAX  |
| A   | 0.90        | ---- | 1.10 |
| A1  | ----        | ---- | 0.05 |
| b   | 0.33        | 0.42 | 0.51 |
| b1  | 0.33        | 0.42 | 0.51 |
| c   | 0.20        | ---- | 0.33 |
| D   | 5.15 BSC    |      |      |
| D1  | 4.70        | 4.90 | 5.10 |
| D2  | 3.90        | 4.10 | 4.30 |
| D3  | 1.50        | 1.70 | 1.90 |
| E   | 6.15 BSC    |      |      |
| E1  | 5.70        | 5.90 | 6.10 |
| E2  | 3.90        | 4.15 | 4.40 |
| e   | 1.27 BSC    |      |      |
| G   | 0.45        | 0.55 | 0.65 |
| h   | ----        | ---- | 12 ° |
| K   | 0.51        | ---- | ---- |
| K1  | 0.56        | ---- | ---- |
| L   | 0.48        | 0.61 | 0.71 |
| M   | 3.25        | 3.50 | 3.75 |
| N   | 1.80        | 2.00 | 2.20 |



DIMENSION: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NVMFD027N10MCL

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi** Website: [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**  
Voice Mail: 1 800-282-9855 Toll Free USA/Canada  
Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative