8/7/6/5/4/3/2/1 Phase Buck Controller with PWM_VID and I²C Interface

NCV81275A

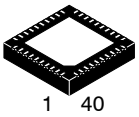
The NCV81275A is a multiphase synchronous controller optimized for new generation computing and graphics processors. The device is capable of driving up to 8 phases and incorporates differential voltage and phase current sensing, adaptive voltage positioning and PWM_VID interface to provide and accurately regulated power for computer or graphic controllers. The integrated power saving interface (PSI) allows for the processors to set the controller in one of three modes, i.e. all phases on, dynamic phases shedding or fixed low phase count mode, to obtain high efficiency in light-load conditions. The dual edge PWM multiphase architecture ensures fast transient response and good dynamic current balance.

Features

- Compliant with NVIDIA® OVR4+ Specifications
- Supports Up to 8 Phases
- 4.5 V to 20 V Supply Voltage Range
- 250 kHz to 1.2 MHz Switching Frequency (8 Phase)
- Power Good Output
- Under Voltage Protection (UVP)
- Over Voltage Protection (OVP)
- Over Current Protection (OCP)
- Per Phase Over Current Protection
- Startup into Pre-Charged Loads while Avoiding False OVP
- Configurable Adaptive Voltage Positioning (AVP)
- High Performance Operational Error Amplifier
- True Differential Current Balancing Sense Amplifiers for Each Phase
- Phase-to-Phase Dynamic Current Balancing
- Current Mode Dual Edge Modulation for Fast Initial Response to Transient Loading
- Power Saving Interface (PSI)
- Automatic Phase Shedding with User Settable Thresholds
- PWM_VID and I²C Control Interface
- Compact 40 Pin QFN Wettable Flank Package
- Operating Temperature Range: −40°C to +105°C
- AEC−Q100 Grade 2 Approved
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

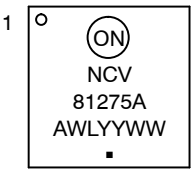
Typical Applications

- GPU and CPU Power
- Automotive Applications



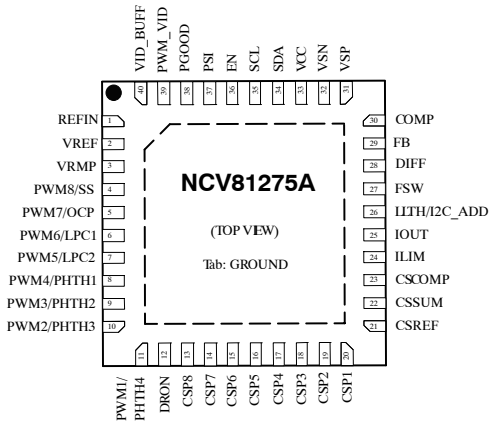
QFNW40
CASE 484AK

MARKING DIAGRAM



NCV81275A = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCV81275AMNTXG	QFNW40 (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

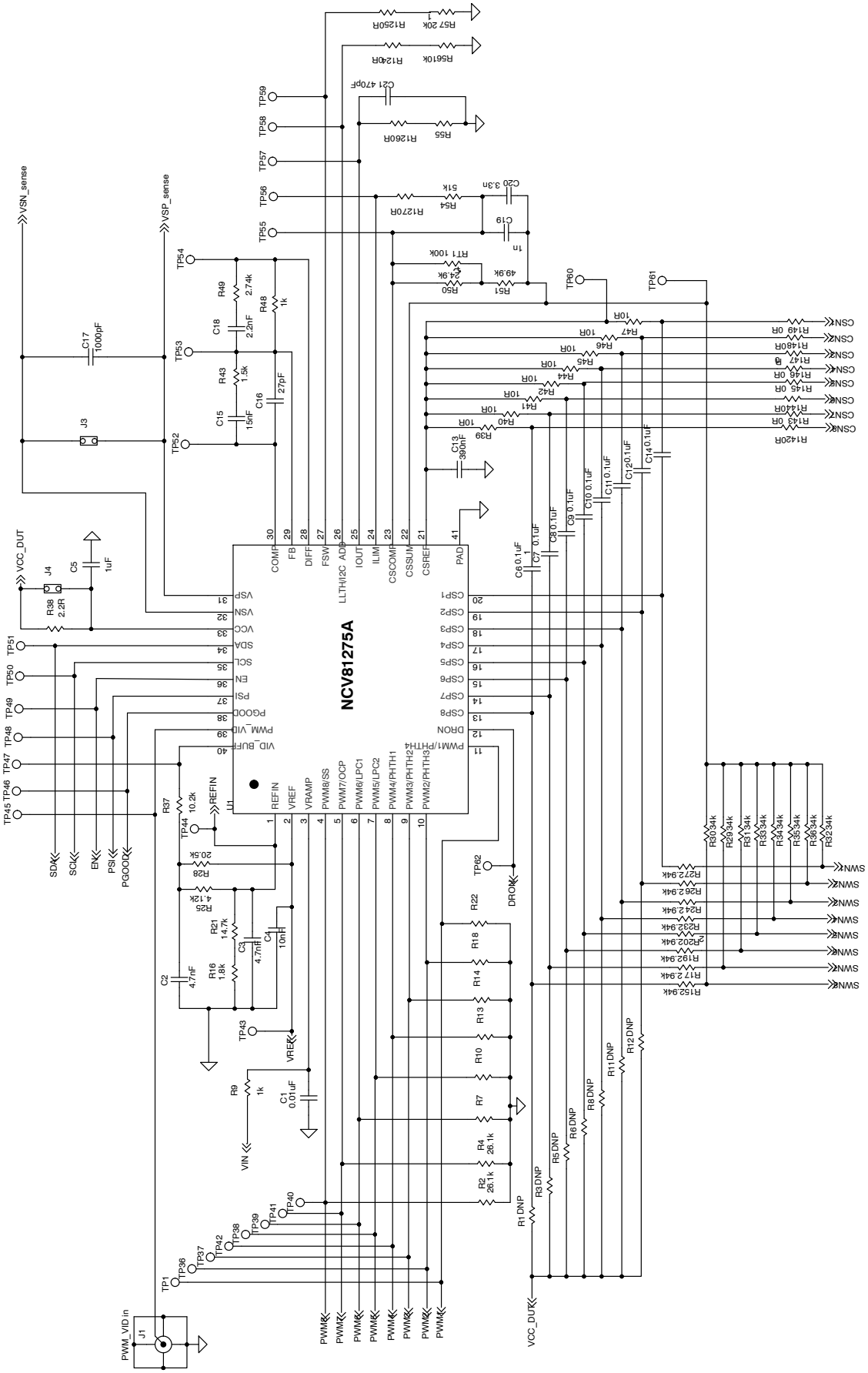


Figure 1. Typical Controller Application Circuit

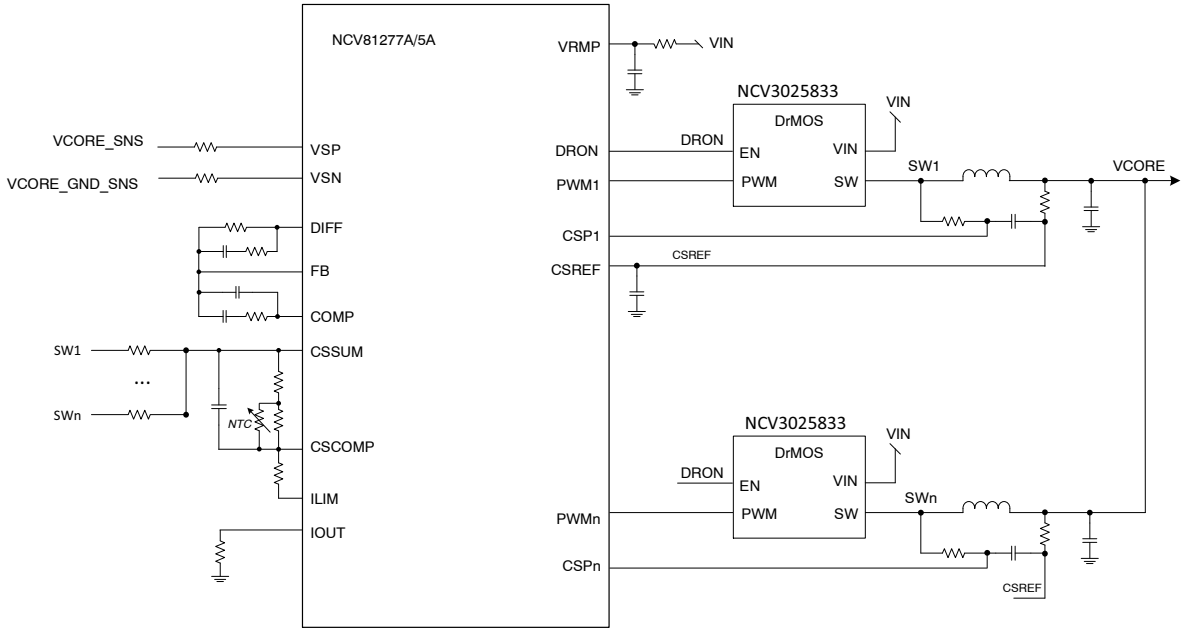


Figure 2. Typical Phase Application Circuit (5x5 DrMOS with no IMON)

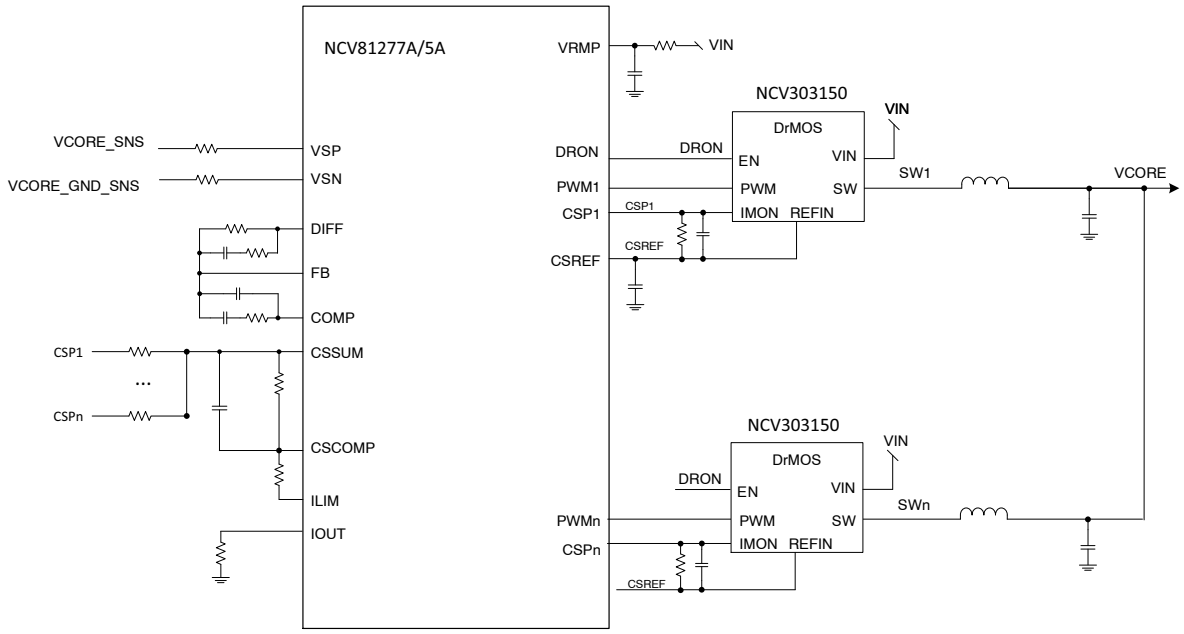


Figure 3. Typical Phase Application Circuit (6x5 DrMOS with IMON)

Table 1. PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Pin Type	Description
1	REFIN	I	Reference voltage input for output voltage regulation.
2	VREF	O	2.0 V output reference voltage. A 10 nF ceramic capacitor is required to connect this pin to ground.
3	VRMP	I	Feed-forward input of VIN for the ramp slope compensation. The current fed into this pin is used to control of the ramp of PWM slope.
4	PWM8/SS	I/O	PWM 8 output/Soft Start setting. During startup it is used to program the soft start time with a resistor to ground.
5	PWM7/OCP	I/O	PWM 7 output/Per OCP setting. During startup it is used to program the OCP level per phase and latch off time with a resistor to ground.
6	PWM6/LPC1	I/O	PWM 6 output/Low phase count 1. During startup it is used to program the power zone (PSI set low) with a resistor to ground.
7	PWM5/LPC2	I/O	PWM 5 output/Low phase count 2. During startup it is used to program boot-up power zone (PSI set low) with a resistor to ground.
8	PWM4/PHTH1	I/O	PWM 4 output/Phase Shedding Threshold 1. During startup it is used to program the phase shedding threshold 1 (PSI set to mid state) with a resistor to ground.
9	PWM3/PHTH2	I/O	PWM 3 output/Phase Shedding Threshold 2. During startup it is used to program the phase shedding threshold 2 (PSI set to mid state) with a resistor to ground.
10	PWM2/PHTH3	I/O	PWM 2 output/Phase Shedding Threshold 3. During startup it is used to program the phase shedding threshold 3 (PSI set to mid state) with a resistor to ground.
11	PWM1/PHTH4	I/O	PWM 1 output/Phase Shedding Threshold 4. During startup it is used to program the phase shedding threshold 4 (PSI set to mid state) with a resistor to ground.
12	DRON	I/O	Bidirectional gate driver enable for external drivers.
13	CSP8	I	Non-inverting input to current balance sense amplifier for phase 8. Pull-up to VCC via a 2K to disable the PWM8 output.
14	CSP7	I	Non-inverting input to current balance sense amplifier for phase 7. Pull-up to VCC via a 2K to disable the PWM7 output.
15	CSP6	I	Non-inverting input to current balance sense amplifier for phase 6. Pull-up to VCC via a 2K to disable the PWM6 output.
16	CSP5	I	Non-inverting input to current balance sense amplifier for phase 5. Pull-up to VCC via a 2K to disable the PWM5 output.
17	CSP4	I	Non-inverting input to current balance sense amplifier for phase 4. Pull-up to VCC via a 2K to disable the PWM4 output.
18	CSP3	I	Non-inverting input to current balance sense amplifier for phase 3. Pull-up to VCC via a 2K to disable the PWM3 output.
19	CSP2	I	Non-inverting input to current balance sense amplifier for phase 2. Pull-up to VCC via a 2K to disable the PWM2 output.
20	CSP1	I	Non-inverting input to current balance sense amplifier for phase 1. Pull-up to VCC via a 2K to disable the PWM1 output.
21	CSREF	I	Total output current sense amplifier reference voltage input.
22	CSSUM	I	Inverting input of total current sense amplifier.
23	CSCOMP	O	Output of total current sense amplifier.
24	ILIM	O	Over current shutdown threshold setting output. The threshold is set by a resistor between ILIM and to CSCOMP pins.
25	IOUT	O	Total output current. A resistor to GND is required to provide a voltage drop of 2 V at the maximum output current.
26	LLTH/I2C_ADD	I	Load line selection from 0% to 100% and I^2C address pin.
27	FSW	I	Resistor to ground form this pin sets the operating frequency of the regulator.
28	DIFF	O	Output of the regulators differential remote sense amplifier.

Table 1. PIN FUNCTION DESCRIPTION (continued)

Pin Number	Pin Name	Pin Type	Description
29	FB	I	Error amplifier inverting (feedback) input.
30	COMP	O	Output of the error amplifier and the inverting input of the PWM comparator.
31	VSP	I	Differential Output Voltage Sense Positive terminal.
32	VSN	I	Differential Output Voltage Sense Negative terminal.
33	VCC	I	Power for the internal control circuits. A 1 μF decoupling capacitor is requires from this pin to ground.
34	SDA	I/O	Serial Data bi-directional pin, requires pull-up resistor to VCC.
35	SCL	I	Serial Bus clock pin, requires pull-up resistor to VCC.
36	EN	I	Logic input. Logic high enables regulator output logic low disables regulator output.
37	PSI	I	Power Saving Interface control pin. This pin can be set low, high or left floating. Use a current limiting resistor of 100 kΩ when driving the pin with 5 V logic.
38	PGOOD	O	Open Drain power good indicator.
39	PWM_VID	I	PWM_VID buffer input.
40	VID_BUFF	O	PWM_VID pulse output from internal buffer.
41	AGND	GND	Analog ground and thermal pad, connected to system ground.

Table 2. MAXIMUM RATINGS

Rating	Pin Symbol	Min	Typ	Max	Unit
Pin Voltage Range (Note 1)	VSN	GND−0.3		GND + 0.3	V
	VCC	−0.3		6.5	V
	VRMP	−0.3		25	V
	PWM_VID	−0.3 (−2, < 50 ns)		VCC + 0.3	V
	All Other Pins with the	−0.3		VCC + 0.3	V
Pin Current Range	COMP	−2		2	mA
	CSCOMP				
	DIFF				
	PGOOD				
	VSN	−1		1	mA
Moisture Sensitivity Level	MSL		1		–
Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions (Note 2)	T_{SLD}		260		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All signals referenced to GND unless noted otherwise.
2. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Min	Typ	Max	Unit
Thermal Characteristics, (QFN40, 5 × 5 mm) Thermal Resistance, Junction-to-Air (Note 1)	$R_{\theta JA}$	–	68	–	°C/W
Process Junction Temperature Range (Note 2)	T_J	−40	–	150	°C
Operating Ambient Temperature Range	T_A	−40	–	105	°C
Maximum Storage Temperature Range	T_{STG}	−55	–	150	°C

1. JESD 51−5 (1S2P Direct-Attach Method) with 0 LFM.
2. JESD 51−7 (1S2P Direct-Attach Method) with 0 LFM.

Table 4. ELECTRICAL CHARACTERISTICS

(Unless otherwise stated: −40°C < T_A < 105°C; 4.6 V < VCC < 5.4 V; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VRMP						
Supply Range		VRMP	4.5		20	V
UVLO	VRMP Rising	$V_{RMPrise}$			4.2	V
	VRMP Falling	$V_{RMPfall}$	3			V
VRMP UVLO Hysteresis		$V_{RMPhyst}$		800		mV
BIAS SUPPLY						
Supply Voltage Range		VCC	4.6		5.4	V
VCC Quiescent current	Enable Low	ICC			40	μA
	8 Phase Operation			50		mA
	1 Phase-DCM Operation			10		mA
UVLO Threshold	VCC Rising	$UVLO_{Rise}$			4.5	V
	VCC Falling	$UVLO_{Fall}$	4			V
VCC UVLO Hysteresis		$UVLO_{Hyst}$		200		mV
SWITCHING FREQUENCY						
Switching Frequency Range	8 Phase Configuration	F_{SW}	250		1200	kHz
Switching Frequency Accuracy	F_{SW} = 810 kHz	ΔF_{SW}	−4		+4	%
			−10		−10	
ENABLE INPUT						
Input Leakage	EN = 0 V or VCC	I_L	−1.0		1.0	μA
Upper Threshold		V_{IH}	1.2			V
Lower Threshold		V_{IL}			0.6	V
DRON						
Output High Voltage	Sourcing 500 μA	V_{OH}	3.0			V
Output Low Voltage	Sinking 500 μA	V_{OL}			0.1	V
Rise Time	Cl(PCB) = 20 pF, ΔV_O = 10% to 90%	t_R		160		ns
Fall Time	Cl(PCB) = 20 pF, ΔV_O = 10% to 90%	t_F		3		ns
Internal Pull-up Resistance		$R_{PULL-UP}$		2.0		kΩ
Internal Pull-down Resistance	VCC = 0 V	R_{PULL_DOWN}		70		kΩ

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(Unless otherwise stated: −40°C < T_A < 105°C; 4.6 V < VCC < 5.4 V; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
PGOOD						
Output Low Voltage	I_{PGOOD} = 10 mA (Sink)	V_{OL}			0.4	V
Leakage Current	P_{GOOD} = 5 V	I_L			0.2	μA
Output Voltage Initialization Time	From EN to DRON	T_init			1.5	ms
Minimum Output Voltage Ramp Time	REFIN = .1.0 V	T_ramp_{MIN}		0.15		ms
Maximum Output Voltage Ramp Time	REFIN = 1.0 V	T_ramp_{MAX}		10		ms
PROTECTION-OCP, OVP, UVP						
Under Voltage Protection (UVP) Threshold	Relative to REFIN Voltage	UVP	250	300	350	mV
Under Voltage Protection (UVP) Delay		T_{UVP}		5		μs
Over Voltage Protection (OVP) Threshold	Relative to REFIN Voltage	OVP	360	400	430	mV
Over Voltage Protection (OVP) Delay		T_{OVP}		5		μs
Over Current Protection (ILIM)	internal current source	$ILIM_{th}$	9.5	10	10.5	μA
PWM OUTPUTS						
Output High Voltage	Sourcing 500 μA	V_{OH}	VCC − 0.2			V
Output Mid Voltage		V_{MID}	1.9	2.0	2.1	V
Output Low Voltage	Sinking 500 μA	V_{OL}			0.7	V
Rise and Fall Time	C_L(PCB) = 50 pF, ΔV_O = 10% to 90% of VCC	t_R, t_F		10		ns
Tri-state Output Leakage	G_x = 2.0 V, x = 1−8, EN = Low	I_L	−1.0		1.0	μA
Minimum On Time	FSW = 600 kHz	Ton		12		ns
0% Duty Cycle	Comp Voltage when PWM Outputs Remain LOW	$VCOMP_{0\%}$		1.3		V
100% Duty Cycle	Comp Voltage when PWM Outputs Remain HIGH	$VCOMP_{100\%}$		2.5		V
PWM Phase Angle Error	Between Adjacent Phases	ø		±15		°
PHASE DETECTION						
Phase Detection Threshold Voltage	CSP2 to CSP8	V_{PHDET}			VCC − 0.1	V
Phase Detect Timer	CSP2 to CSP8	T_{PHDET}		1.1		ms
ERROR AMPLIFIER						
Input Bias Current		I_{BIAS}	−400		400	nA
Open Loop DC Gain	C_L = 20 pF to GND, R_L = 10 kΩ to GND	G_{OL}		80		dB
Open Loop Unity Gain Bandwidth	C_L = 20 pF to GND, R_L = 10 kΩ to GND	GBW		20		MHz
Slew Rate	ΔV_{IN} = 100 mV, G = −10 V/V, ΔV_{OUT} = 0.75−1.52 V, C_L = 20 pF to GND, R_L = 10 kΩ to GND	SR		5		V/μs
Maximum Output Voltage	I_{SOURCE} = 2 mA	V_{OUT}	3.5			V
Minimum Output Voltage	I_{SINK} = 2 mA	V_{OUT}			1	V

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(Unless otherwise stated: −40°C < T_A < 105°C; 4.6 V < VCC < 5.4 V; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
DIFFERENTIAL SUMMING AMPLIFIER						
Input Bias Current		I_{BIAS}	−400		400	nA
VSP Input Voltage		V_{IN}	0		2	V
VSN Input Voltage		V_{IN}	−0.3		0.3	V
−3dB Bandwidth	C_L = 20 pF to GND, R_L = 10 kΩ to GND	BW		12		MHz
Closed Loop DC Gain (VSP−VSN to DIFF)	VSP to VSN = 0.5 to 1.3 V	G		1		V/V
Droop accuracy	CSREF − DROOP = 80 mV, V_{REFIN} = 0.8 V to 1.2 V	ΔDROOP	78		82	mV
Maximum Output Voltage	I_{SOURCE} = 2 mA	V_{OUT}	3			V
Minimum Output Voltage	I_{SINK} = 2 mA	V_{OUT}			0.8	V
CURRENT SUMMING AMPLIFIER						
Offset Voltage		V_{OS}	−500		500	μV
Input Bias Current	CSSUM = CSREF = 1 V	I_L	−7.5		7.5	μA
Open Loop Gain		G		80		dB
Current sense Unity Gain Bandwidth	C_L = 20 pF to GND, R_L = 10 kΩ to GND	GBW		10		MHz
Maximum CSCOMP Output Voltage	I_{SOURCE} = 2 mA	V_{OUT}	3.5			V
Minimum CSCOMP Output Voltage	I_{SINK} = 2 mA	V_{OUT}			0.1	V
CURRENT BALANCE AMPLIFIER						
Input Bias Current	CSP_X − CSP_{X+1} = 1.2 V	I_{BIAS}	−50		50	nA
Common Mode Input Voltage Range	CSP_X = CSREF	V_{CM}	0		2	V
Differential Mode Input Voltage Range	CSREF = 1.2 V	V_{DIFF}	−100		100	mV
Closed Loop Input Offset Voltage Matching	CSP_X = 1.2 V, Measured from the Average		−1.5		1.5	mV
Current Sense Amplifier Gain	0 V < CSP_X < 0.1 V	G	5.7	6.0		V/V
Multiphase Current Sense Gain Matching	CSREF = CSP = 10 mV to 30 mV	ΔG	−3		3	%
−3dB Bandwidth		BW		8		MHz
IOUT						
Input Reference Offset Voltage	ILIM to CSREF	V_{OS}	−3		+3	mV
Output Current Max	ILIM Sink Current 20 μA	I_{OUT}		200		μA
Current Gain	IOUT/ILIM, R_{LIM} = 20 kΩ, R_{IOUT} = 5 kΩ	G	9.5	10	10.5	A/A
VOLTAGE REFERENCE						
VREF Reference Voltage	I_{REF} = 1 mA	VREF	1.98	2	2.02	V
VREF Reference accuracy	T_{JMIN} < T_J < T_{JMAX}	ΔVREF		1		%

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(Unless otherwise stated: −40°C < T_A < 105°C; 4.6 V < VCC < 5.4 V; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
PSI						
PSI High Threshold		V_{IH}	1.45			V
PSI Mid threshold		V_{MID}	0.8		1	V
PSI Low threshold		V_{IL}			0.575	V
PSI Input Leakage Current	V_{PSI} = 0 V	I_L	−1		1	μA
PWM_VID BUFFER						
Upper Threshold		V_{IH}	1.21			V
Lower Threshold		V_{IL}			0.575	V
PWM_VID Switching Frequency		F_{PWM_VID}	400		5000	kHz
Output Rise Time		t_R		3		ns
Output Fall Time		t_F		3		ns
Rising and Falling Edge Delay	$\Delta t = t_R - t_F$	Δt		0.5		ns
Propagation Delay	$t_{PD} = t_{PDHL} = t_{PDLH}$	t_{PD}		8		ns
Propagation Delay Error	$\Delta t_{PD} = t_{PDHL} - t_{PDLH}$	Δt_{PD}		0.5		ns
REFIN						
REFIN Discharge Switch ON-Resistance	$I_{REEFIN(SINK)}$ = 2 mA	R_{DISCH}		10		Ω
Ratio of Output Voltage Ripple Transferred from REFIN/REFIN Voltage Ripple	F_{PWM_VID} = 400 kHz, $F_{SW} \leq$ 600 kHz	$V_{ORP/VREFIN}$		10		%
	F_{PWM_VID} = 1000 kHz, $F_{SW} \leq$ 600 kHz	$V_{ORP/VREFIN}$		30		
I²C						
Logic High Input Voltage	From 10% to 90%	V_{IH}	1.7			V
Logic Low Input Voltage	From 10% to 90%	V_{IL}			0.5	V
Hysteresis (Note 4)				80		mV
Output Low Voltage	I_{SDA} = −6 mA	V_{OL}			0.4	V
Input Current		I_L	−1		1	μA
Input Capacitance (Note 4)		C_{SDA}, C_{SCL}		5		pF
Clock Frequency	See Figure 4	f_{SCL}			400	kHz
SCL Low Period (Note 4)		t_{LOW}	1.3			μs
SCL High Period (Note 4)		t_{HIGH}	0.6			μs
SCL/SDA Rise Time (Note 4)		t_R			300	ns
SCL/SDA Fall Time (Note 4)		t_F			300	ns
Start Condition Setup Time (Note 4)		$t_{SU;STA}$	600			ns
Start Condition Hold Time (Note 1, 4)		$t_{HD;STA}$	600			ns
Data Setup Time (Note 2, 4)		$t_{SU;DAT}$	100			ns
Data Hold Time (Note 2, 4)		$t_{HD;DAT}$	300			ns
Stop Condition Setup Time (Note 3, 4)		$t_{SU;STO}$	600			ns
Bus Free Time between Stop and Start (Note 4)		t_{BUF}	1.3			μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Time from 10% of SDA to 90% of SCL.
2. Time from 10% or 90%of SDA to 10% of SCL.
3. Time from 90% of SCL to 10% of SDA.
4. Guaranteed by design, not production tested.

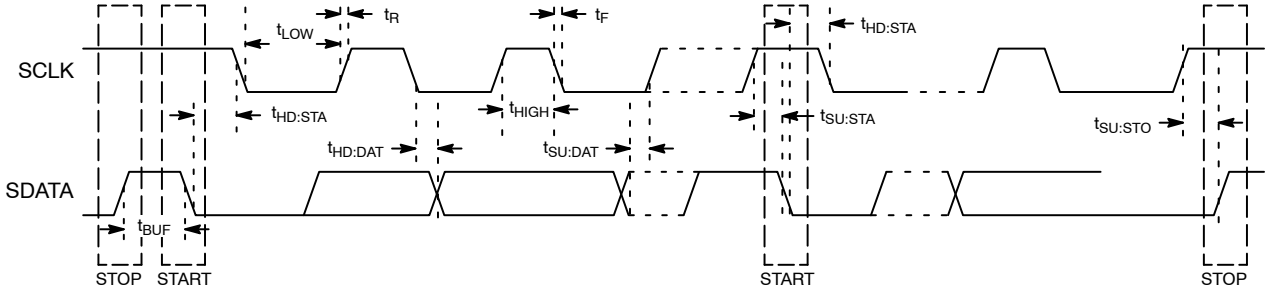


Figure 4. I²C Timing Diagram

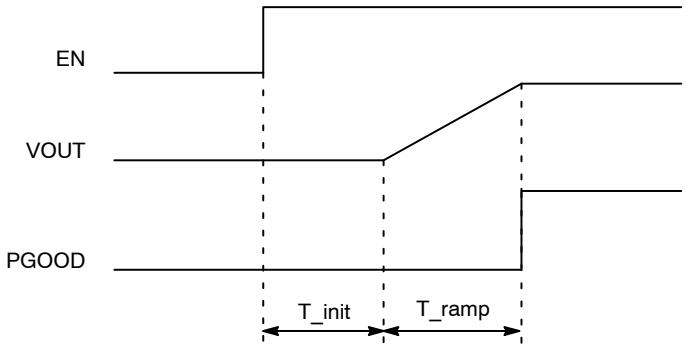


Figure 5. Soft Start Timing Diagram

Applications Information

The NCV81275A is a buck converter controller optimized for the next generation computing and graphic processor applications. It contains eight PWM channels which can be individually configured to accommodate buck converter configurations up to eight phases. The controller regulates the output voltage all the way down to 0 V with no load. Also, the device is functional with input voltages as low as 3.3 V.

The output voltage is set by applying a PWM signal to the PWM_VID input of the device. The controller converts the PWM_VID signal with variable high and low levels into a constant amplitude PWM signal which is then applied to the REFIN pin. The device calculates the average value of this PWM signal and sets the regulated voltage accordingly.

The output voltage is differentially sensed and subtracted from the REFIN average value. The result is biased up to 1.3 V and applied to the error amplifier. Any difference between the sensed voltage and the REFIN pin average voltage will change the PWM outputs duty cycle until the two voltages are identical. The load current is current is continuously monitored on each phase and the PWM outputs are adjusted to ensure adjusted to ensure even distribution of the load current across all phases. In addition, the total load current is internally measured and used to implement a programmable adaptive voltage positioning mechanism.

The device incorporates overcurrent, under and overvoltage protections against system faults.

The communication between the NCV81275A and the user is handled with two interfaces, PWM_VID to set the output voltage and I²C to configure or monitor the status of the controller. The operation of the internal blocks of the device is described in more details in the following sections.

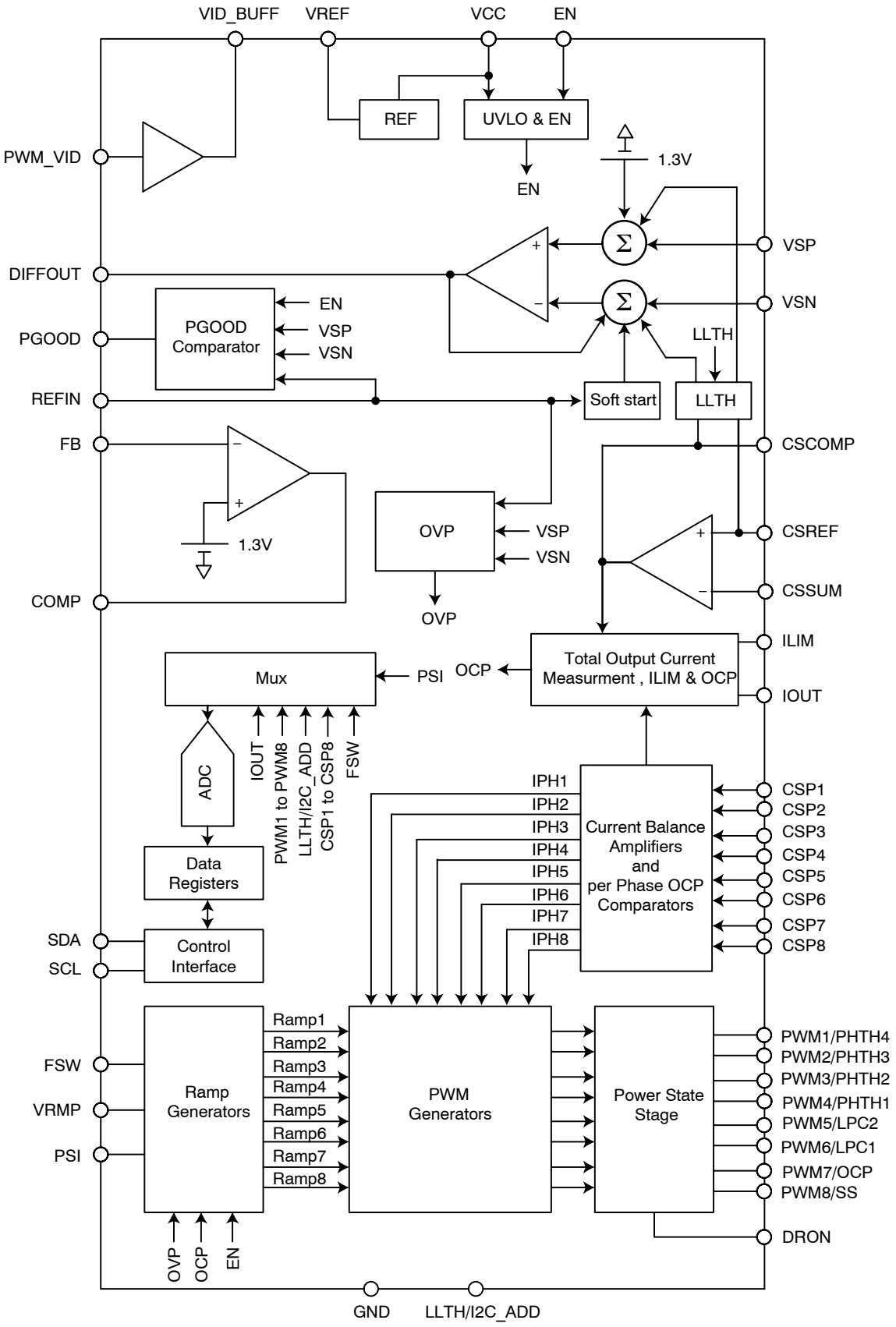


Figure 6. NCV81275A Functional Block Diagram

PWM_VID Interface

PWM_VID is a single wire dynamic voltage control interface where the regulated voltage is set by the duty cycle of the PWM signal applied to the controller.

The device controller converts the variable amplitude PWM signal into a constant 2 V amplitude PWM signal while preserving the duty cycle information of the input signal. In addition, if the PWM_VID input is left floating, the VID_BUFF output is tri-stated (floating).

The constant amplitude PWM signal is then connected to the REFIN pin through a scaling and filtering network (see Figure 7). This network allows the user to set the minimum and maximum REFIN voltages corresponding to 0% and 100% duty cycle values.

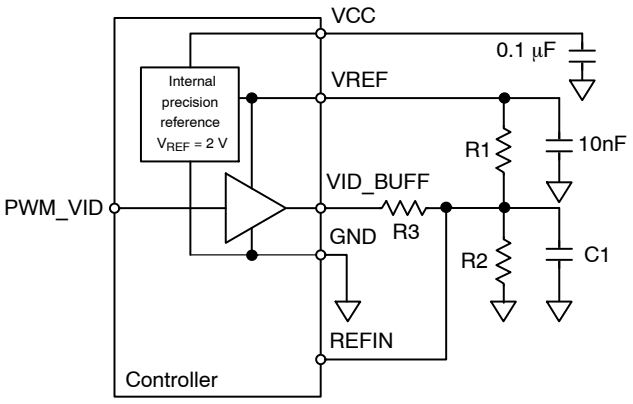


Figure 7. PWM_VID Interface

The minimum (0% duty cycle), maximum (100% duty cycle) and boot (PWM_VID input floating) voltages can be calculated with the following formulas:

$$V_{MAX} = V_{REF} \cdot \frac{1}{1 + \frac{R_1 \cdot R_3}{R_2 \cdot (R_1 + R_3)}} \quad \text{(eq. 1)}$$

$$V_{MIN} = V_{REF} \cdot \frac{1}{1 + \frac{R_1 \cdot (R_2 + R_3)}{R_2 \cdot R_3}} \quad \text{(eq. 2)}$$

$$V_{BOOT} = V_{REF} \cdot \frac{1}{1 + \frac{R_1}{R_2}} \quad \text{(eq. 3)}$$

Soft Start

Soft start is defined as the transition from Enable assertion high to the assertion of Power good as shown in Figure 5.

The output is set to the desired voltage in two steps, a fixed initialization step of 1.5 ms followed by a ramp-up step where the output voltage is ramped to the final value set by the PWM_VID interface. During the soft start phase, PGOOD pin is initially set low and will be set high when the output voltage is within regulation and the soft start ramp is complete. The PGOOD signal only de-asserts (pull low) when the controller shuts down due to a fault condition (UVLO, OVP or OCP event).

The output voltage ramp-up time is user settable by connecting a resistor between pin PWM8/SS and GND. The controller will measure the resistance value at power-up by sourcing a 10 μA current through this resistor and set the ramp time (t_{ramp}) as shown in Table 16. When a fast SS ramp is selected, external filtering should ensure REFIN signal settled before the PGOOD signal asserted.

Remote Voltage Sense

A high performance true differential amplifier allows the controller to measure the output voltage directly at the load using the VSP (VOUT) and VSN (GND) pins. This keeps the ground potential differences between the local controller ground and the load ground reference point from affecting regulation of the load. The output voltage of the differential amplifier is set by the following equation:

$$V_{DIFOUT} = (V_{VSP} - V_{VSN}) + (1.3\ V - V_{REFIN}) + \\ + (V_{DROOP} + V_{CSREF}) \quad \text{(eq. 4)}$$

Where:

V_{DIFOUT} is the output voltage of the differential amplifier.

$V_{VSP} - V_{VSN}$ is the regulated output voltage sensed at the load.

V_{REFIN} is the voltage at the output pin set by the PWM_VID interface.

$V_{DROOP} - V_{CSREF}$ is the expected drop in the regulated voltage as a function of the load current (load-line).

1.3 V is an internal reference voltage used to bias the amplifier inputs to allow both positive and negative output voltage for V_{DIFOUT}.

Error Amplifier

A high performance wide bandwidth error amplifier is provided for fast response to transient load events. Its inverting input is biased internally with the same 1.3 V reference voltage as the one used by the differential sense amplifier to ensure that both positive and negative error voltages are correctly handled.

An external compensation circuit should be used (usually type III) to ensure that the control loop is stable and has adequate response.

Ramp Feed-Forward Circuit

The ramp generator circuit provides the ramp used to generate the PWM signals using internal comparators (see Figure 8) The ramp generator provides voltage feed-forward control by varying the ramp magnitude with respect to the VRMP pin voltage. The PWM ramp time is changed according to the following equation:

$$V_{RAMPpk=pk_{pp}} = 0.1 \cdot V_{VRMP} \quad \text{(eq. 5)}$$

The VRMP pin also has a UVLO function. The VRMP UVLO is only active after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled.

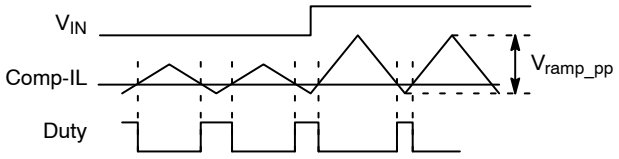


Figure 8. Ramp Feed-Forward Circuit

PWM Output Configuration

By default the controller operates in 8 phase mode, however with the use of the CSP pins the phases can be disabled by connecting the CSP pin to VCC. At power-up the NCV81275A measures the voltage present at each CSP pin and compares it with the phase detection threshold. If the voltage exceeds the threshold, the phase is disabled. The phase configurations that can be achieved by the device are listed in Table 6. The active phase (PWM_X) information is also available to the user in the phase status register.

PSI, LPC_X, $PHTH_X$

The NCV81275A incorporates a power saving interface (PSI) to maximize the efficiency of the regulator under various loading conditions. The device supports up to six distinct operation modes, called power zones using the PSI, LPC_X and $PHTH_X$ pins (see Table 7). At power-up the controller reads the PSI pin logic state and sources a 10 μA current through the resistors connected to the LPC_X and $PHTH_X$ pins, measures the voltage at these pins and configures the device accordingly.

The configuration can be changed by the user by writing to the LPC_X and $PHTH_X$ configuration registers.

After EN is set high, the NCV81275A ignores any change in the PSI pin logic state until the output voltage reaches the nominal regulated voltage.

When PSI = High, the controller operates with all active phases enabled regardless of the load current. If PSI = Mid, the NCV81275A operates in dynamic phase shedding mode where the voltage present at the IOUT pin (the total load current) is measured every 10 μs and compared to the $PHTH_X$ thresholds to determine the appropriate power zone.

The resistors connected between the $PHTH_X$ and GND should be picked to ensure that a 10 μA current will match the voltage drop at the IOUT pin at the desired load current. Please note that the maximum allowable voltage at the IOUT pin at the maximum load current is 2 V. Any $PHTH_X$ threshold can be disabled if the voltage drop across the $PHTH_X$ resistor is ≥ 2 V for a 10 μA current, the pin is left floating or 0xFF is written to the appropriate $PHTH_X$ configuration register.

At power-up, the automatic phase shedding mode is only enabled after the output voltage reaches the nominal regulated voltage.

When PSI = Low, the controller is set to a fixed power zone regardless of the load current. The LPC2 hardware setting controls the power zone when EN is turned on and PSI=low. If PSI stays low, its power zone can be further changed by the I2C register 0x36, Bit[5:3] if the secondary function is enabled. If PSI transitions to other levels (Mid or High) and back to Low level when the device is enabled, the power zone control will switch to LPC1 configuration hardware setting or I2C register 0x36, Bit[2:0] if the secondary function is enabled.

LLTH/I2C_ADD

The LLTH/I2C_ADD pin enables the user to change the percentage of the externally programmed droop that takes effect on the output. In addition, the LLTH/I2C_ADD pin sets the I^2C slave address of the NCV81275A. The maximum load line is controlled externally by setting the gain of the current sense amplifier. On power up a 10 μA current is sourced from the LLTH/I2C_ADD pin through a resistor and the resulting voltage is measured. The load line and I^2C slave address configurations achievable using the external resistor is listed in the table below. The percentage load line can be fine-tuned over the I^2C interface by writing to the LL configuration register.

Table 5. LLTH/I2C_ADD PIN SETTING

Resistor (kΩ)	Load Line (%)	Slave Address (Hex)
10	100	0x20
23.2	0	0x20
37.4	100	0x30
54.9	0	0x30
78.7	100	0x40
110	0	0x40
147	100	0x50
249	0	0x50

NOTE: 1% tolerance.

Table 6. PWM OUTPUT CONFIGURATION

Configuration	Phase Configuration	CSP Pin Configuration (✓ = Normal Connection, X = Tied to VCC)								Enabled PWM Outputs (PWM_X Pins)
		CSP1	CSP2	CSP3	CSP4	CSP5	CSP6	CSP7	CSP8	
1	8 Phase	✓	✓	✓	✓	✓	✓	✓	✓	1, 2, 3, 4, 5, 6, 7, 8
2	7 Phase	✓	✓	✓	✓	✓	✓	✓	X	1, 2, 3, 4, 5, 6, 7
3	6 Phase	✓	✓	✓	✓	✓	✓	X	X	1, 2, 3, 4, 5, 6
4	5 Phase	✓	✓	✓	✓	✓	X	X	X	1, 2, 3, 4, 5
5	4 Phase	✓	✓	✓	✓	X	X	X	X	1, 2, 3, 4
6	3 Phase	✓	✓	✓	X	X	X	X	X	1, 2, 3
7	2 Phase	✓	✓	X	X	X	X	X	X	1, 2
8	1 Phase	✓	X	X	X	X	X	X	X	1

Table 7. PSI, LPC_X, $PHTH_X$ CONFIGURATION (Note 1)

PSI Logic State	LPC_X Resistor (kΩ)	IOUT vs. $PHTH_X$ Comparison	Power Zone (Note 2)							
			8 Phase	7 Phase	6 Phase	5 Phase	4 Phase	3 Phase	2 Phase	1 Phase
High	Disabled	Function Disabled	0	0	0	0	0	0	0	0
Low	10		0	0	0	0	0	0	0	0
	23.2		1	0	0	0	0	0	0	0
	37.4		2	0	2	0	2	0	0	0
	54.9		3	3	3	3	3	3	3	0
	78.7		4	4	4	4	4	4	4	4
Mid	Function Disabled	IOUT > PHTH4	0	0	0	0	0	0	0	0
		PTHT4 > IOUT > PHTH3	1	0	0	0	0	0	0	0
		PHTH3 > IOUT > PHTH2	2	0	2	0	2	0	0	0
		PHTH2 > IOUT > PHTH1	3	3	3	3	3	3	3	0
		IOUT < PHTH1	4	4	4	4	4	4	4	4

1. 1% tolerance.
2. Power zone 4 is DCM @100 kHz switching frequency, while zones 0 to 3 are CCM.

Table 8. PHASE SHEDDING CONFIGURATIONS

Power Zone	PWM Output Configuration	PWM Output Status (✓ = Enabled, X = Disabled)							
		PWM1	PWM2	PWM3	PWM4	PWM5	PWM6	PWM7	PWM8
0	8 Phase	✓	✓	✓	✓	✓	✓	✓	✓
1		✓	X	✓	X	✓	X	✓	X
2		✓	X	X	X	✓	X	X	X
3		✓	X	X	X	X	X	X	X
4		✓	X	X	X	X	X	X	X
0	7 Phase	✓	✓	✓	✓	✓	✓	✓	X
3		✓	X	X	X	X	X	X	X
4		✓	X	X	X	X	X	X	X
0	6 Phase	✓	✓	✓	✓	✓	✓	X	X
2		✓	X	✓	X	✓	X	X	X
3		✓	X	X	X	X	X	X	X
4		✓	X	X	X	X	X	X	X

Table 8. PHASE SHEDDING CONFIGURATIONS (continued)

Power Zone	PWM Output Configuration	PWM Output Status (✓ = Enabled, X = Disabled)							
		PWM1	PWM2	PWM3	PWM4	PWM5	PWM6	PWM7	PWM8
0	5 Phase	✓	✓	✓	✓	✓	X	X	X
3		✓	X	X	X	X	X	X	X
4		✓	X	X	X	X	X	X	X
0	4 Phase	✓	✓	✓	✓	X	X	X	X
2		✓	X	✓	X	X	X	X	X
3		✓	X	X	X	X	X	X	X
4		✓	X	X	X	X	X	X	X
0	3 Phase	✓	✓	✓	X	X	X	X	X
3		✓	X	X	X	X	X	X	X
4		✓	X	X	X	X	X	X	X
0	2 Phase	✓	✓	X	X	X	X	X	X
3		✓	X	X	X	X	X	X	X
4		✓	X	X	X	X	X	X	X
0	1 Phase	✓	X	X	X	X	X	X	X
4		✓	X	X	X	X	X	X	X

Power Zone Transition/Phase Shedding

The power zones supported by the NCV81275A are set by the resistors connected to the LPC_X pins (PSI = Low) or $PHTH_X$ pins (PSI = Mid).

When PSI is set to the Mid-state, the NCV81275A employs a phase shedding scheme where the power zone is automatically adjusted for optimal efficiency by continuously measuring the total output current (voltage at the IOUT pin) and compare it with the $PHTH_X$ thresholds. When the comparison result indicates that a lower power zone number is required (an increase in the IOUT value), the controller jumps to the required power zone immediately. A decrease in IOUT that indicates that the controller needs to switch into a higher power zone number, the transition will be executed with a delay of 200 μs set by the phase shed delay configuration register. The value of the delay can be adjusted by the user in steps of 10 μs if required. To avoid excessive ripple on the output voltage, all power zone changes are gradual and include all intermediate power zones between the current zone and the target zone set by the comparison of the output current with the $PHTH_X$ thresholds, each transition introducing a programmable 200 μs delay. To avoid false changes from one power zone to another caused by noise or short IOUT transients, the comparison between IOUT and $PHTH_X$ threshold uses hysteresis. The switch to a lower power zone is executed if IOUT exceeds the $PHTH_X$ threshold values while a transition to a higher power zone number is only executed if IOUT is below $PHTH_X$-Hysteresis value. The hysteresis value is set to 0x10h and can be changed by the user by writing to the phase shedding configuration register. If a power zone/$PHTH_X$ threshold is disabled, the controller will skip it during the power zone transition process.

When PSI = Low and the user requires to change the power zone, the transition to the new power zone is identical to the transition process used when PSI is set to the Mid-state. The only exception is when the target power zone is disabled in automatic phase shedding mode. In this case, the controller will automatically enable the target power zone and allow the transition. When the controller is set to automatic phase shedding, the power zone will be automatically disabled.

Switching Frequency

A programmable precision oscillator is provided. The clock oscillator serves as the master clock to the ramp generator circuit. This oscillator is programmed by a resistor to ground on the FSW pin. The FSW pin provides approximately 2 V out and the source current is mirrored into the internal ramp oscillator. The oscillator frequency is approximately proportional to the current flowing in the resistor. Table 19 lists the switching frequencies that can be set using discrete resistor values for each phase configuration. Also, the switching frequency information is available in the FSW configuration register and it can be changed by the user by writing to the FSW configuration register.

Total Current Sense Amplifier

The controller uses a patented approach to sum the phase currents into a single temperature compensated total current signal (Figure 9).

This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The total current signal is floating with respect to CSREF. The current signal is the difference between

CSCOMP and CSREF. The REF(n) resistors sum the signals from the output side of the inductors to create a low impedance virtual ground.

The amplifier actively filters and gains up the voltage applied across the inductors to recover the voltage drop across the inductor series resistance (DCR). RTH is placed near an inductor to sense the temperature of the inductor. This allows the filter time constant and gain to be a function of the NTC's resistance (RTH) and compensate for the change in the DCR with temperature.

The DC gain equation for the current sensing:

$$V_{CSCOMP-CSREF} = -\frac{RCS2 + \frac{RCS1 \cdot RTH}{RCS1 + RTH}}{RPH} \cdot I_{OUT_{Total}} \cdot DCR \quad \text{(eq. 6)}$$

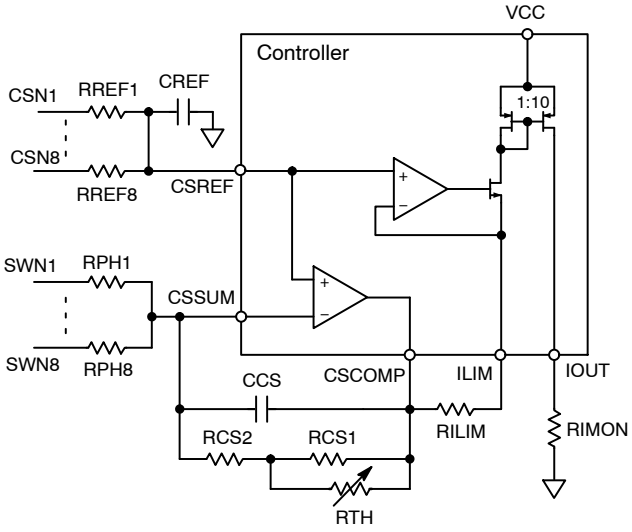


Figure 9. Total Current Summing Amplifier

Set the gain by adjusting the value of the RPH resistors. The DC gain should be set to the output voltage droop. If the voltage from CSCOMP to CSREF is less than 100 mV at the maximum output current $IOUT_{MAX}$ then it is recommend increasing the gain of the CSCOMP amp. This is required to provide a good current signal to offset voltage ratio for the ILIMIT pin. The NTC should be placed near the inductor used by phase 1. The output voltage droop should be set with the droop filter divider.

The pole frequency in the CSCOMP filter should be set equal to the zero from the output inductor. This allows the circuit to recover the inductor DCR voltage drop current signal. It is best to fine tune this filter during transient testing.

$$F_Z = \frac{DCR@25C}{2 \cdot \pi \cdot L_{Phase}} \quad \text{(eq. 7)}$$

Programming the Current Limit ILIM

The current limit thresholds are programmed with a resistor between the ILIMIT and CSCOMP pins. The ILIMIT pin mirrors the voltage at the CSREF pin and mirrors the sink current internally to IOUT (reduced by the IOUT Current Gain) and the current limit comparators. The 100% current limit (CLIM1) trips if the ILIMIT sink current exceeds 10 μA for 50 μs. The 150% current limit (CLIM2) trips with minimal delay if the ILIMIT sink current exceeds 15 μA. Set the value of the current limit resistor based on the CSCOMP−CSREF voltage as shown below.

$$RILIM = \frac{V_{CSCOMP-CSREF@ILIMIT}}{10\ \mu A} \quad \text{(eq. 8)}$$

or

$$RILIM = \frac{RCS2 + \frac{RCS1 \cdot RTH}{RCS1 + RTH}}{RPH} \cdot I_{OUT_{LIMIT}} \cdot DCR}{10\ \mu A} \quad \text{(eq. 9)}$$

When PSI=low, current limit threshold will be scaled down according to its remaining phase count in the power zone: e.g. Iout_limit_2ph=2*Iout_limit/N. In this case total phase number N=8.

Programming DROOP

The signals CSCOMP and CSREF are differentially summed with the output voltage feedback to add precision voltage droop to the output voltage.

$$Droop = DCR \cdot \frac{(RCS1 \parallel RTH) + RCS2}{RPH} \quad \text{(eq. 10)}$$

Programming IOUT

The IOUT pin sources a current in proportion to the ILIMIT sink current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to system max current generates a 2 V signal on IOUT. A pull-up resistor to VCC can be used to offset the IOUT signal positive if needed.

$$R_{IOUT} = \frac{2.0\ V \cdot RILIM}{10 \cdot \frac{RCS2 + \frac{RCS1 \cdot RTH}{RCS1 + RTH}}{RPH} \cdot I_{OUT_{MAX}} \cdot DCR} \quad \text{(eq. 11)}$$

PROTECTIONS

OCP

The device incorporates an over current protection mechanism to shut down and latch off to protect against damage due to an over current event. The current limit threshold set by the ILIM pin on a full system basis.

The current limit thresholds are programmed with a resistor between the ILIMIT and CSCOMP pins. The ILIMIT pin mirrors the voltage at the CSREF pin and mirrors the sink current internally to IOUT (reduced by the IOUT Current Gain) and the current limit comparators. Set the value of the current limit resistor based on the CSCOMP−CSREF voltage as shown in the Programming the Current Limit ILIM section.

In addition to the total current protection, the device incorporates an OCP function on a per phase basis (CLIM_phase) by continuously monitoring the CSPX−CSREF voltage. The per-phase OCP limit is selected on startup when a 10 μA current is sourced from the PWM6/OCP. The resulting voltage read on the pin selects both the max per phase current and delay time (see Table 9). These can also be programmed over I^2C (see Table 17).

Table 9. PER PHASE OCP SETTINGS

Resistance (kΩ)	Per Phase Voltage (mV)	Latch Off Delay (ms)
10	65	4
14.7	75	4
20	100	4
26.1	134	4
33.2	65	6
41.2	75	6
49.9	100	6
60.4	134	6
71.5	65	8
84.5	75	8
100	100	8
118.3	134	8
136.6	65	10
157.7	75	10
182.1	100	10
249	134	10

NOTE: 1% tolerance.

Under Voltage Lock-Out (VCC UVLO)

VCC is constantly monitored for the under voltage lockout (UVLO) During power up both the VRMP and the VCC pin are monitored Only after both pins exceed their individual UVLO threshold will the full circuit be activated and ready for the soft start ramp.

Over Voltage Protection

An output voltage monitor is incorporated into the controller. Over voltage protection will be tripped under the following situations: for REFIN below 1.6V, if the output voltage is 400 mV over the REFIN value; for REFIN over 1.6 V, as long as the output is above 2 V, the output will be clamped to 2 V before being discharged. Once the over voltage protection trips, the PGOOD pin will be pulled low, but DRON will stay high. PWM outputs will only be allowed to toggle between mid and low to discharge the output. The PWM output high will remain disabled until the power is cycled or the EN pin is toggled.

Under Voltage Protection

An under voltage protection will be tripped if the output is 300 mV below the REFIN voltage. When under voltage protection trips, the PGOOD pin will be pulled low, the DRON will stay high. PWM outputs will only be allowed to toggle between mid and low to discharge the output. The PWM output high will remain disabled until the power is cycled or the EN pin is toggled.

I^2C Interface

The controller is connected to this bus as a slave device, under the control of a master controller.

Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high might be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high-to-low transition on the serial data line SDA while the serial clock line, SCL, remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/W bit, which determines the direction of the data transfer, i.e., whether data will be written to or read from the slave device. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is a 0, the master will write to the slave device. If the R/W bit is a 1, the master will read from the slave device.
2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an Acknowledge Bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low-to-high transition when the clock is high may be interpreted as a STOP signal. The number of data bytes that can be transmitted over the serial bus in a single READ or WRITE operation is limited only by what the master and slave devices can handle.
3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10^{th} clock pulse to assert a STOP condition. In READ mode, the master device will override the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the tenth clock pulse, then high during the tenth clock pulse to assert a STOP condition.
4. Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation. To write data to one of the device data registers or read data from it, the Address

Pointer Register must be set so that the correct data register is addressed, and then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the Address Pointer Register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register. The device address is sent over the bus followed by R/W set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the Address Pointer Register. The second data byte is the data to be written to the internal data register.

READ A SINGLE WORD

The master device asserts the start condition. The master then sends the 7-bit slave address. It is followed by a R/W bit that indicates the direction of operation, which will be a write operation in this case. The slave whose address is on the bus acknowledges it by an ACK signal on the bus (by holding SDA line low). The master then sends register address on the bus. The slave device accepts it by an ACK. The master then asserts a repeated start condition followed by a 7-bit slave address. The master then sends a direction bit R/W which is Read for this case. Controller acknowledges it by an ACK signal on the bus. This will start the read operation and controller sends the high byte of the register on the bus. Master reads the high byte and asserts an ACK on the SDA line. Controller now sends the low byte of the register on the SDA line. The master acknowledges it by a no acknowledge NACK on the SDA line. The master then asserts the stop condition to end the transaction.

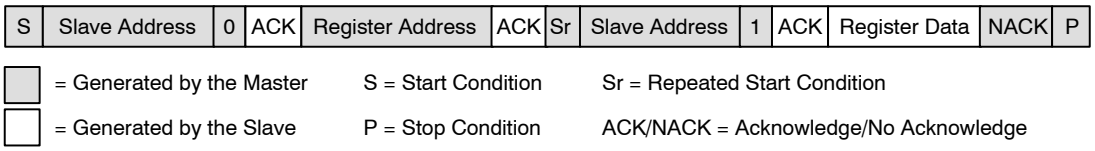


Figure 10. Single Register Read Operation

READING THE SAME REGISTERS MULTIPLE TIMES

The master device asserts the start condition. The master then sends the 7-bit slave address. It is followed by a R/W bit that indicates the direction of operation, which will be a write operation in this case. The slave whose address is on the bus acknowledges it by an ACK signal on the bus (holding SDA line low). The master then sends register address on the bus. The slave device accepts it by an ACK. The master then asserts a repeated start condition followed by a 7-bit slave address. The master then sends a direction bit R/W which is Read for this case. Slave device acknowledges it by an ACK signal on the bus. This will start the read operation:

1. The slave device sends the high byte of the register on the bus.
2. The master reads the high byte and asserts an ACK on the SDA line.
3. The slave device now sends the low byte of the register on the SDA line.
4. The master acknowledges it by an ACK signal on the SDA line.
5. The master and slave device keeps on repeating steps 1–4 until the low byte of the last reading is transferred. After receiving the low byte of the last register, the master asserts a not acknowledge NACK on the SDA. The master then asserts a stop condition to end the transaction.

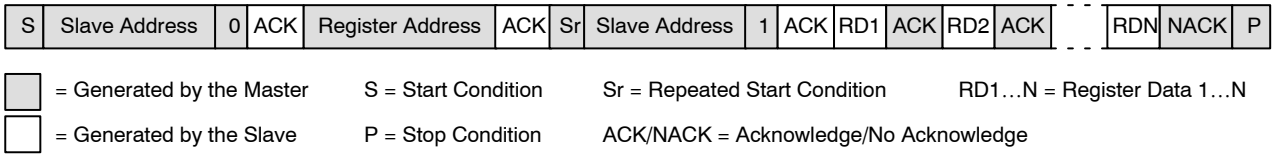


Figure 11. Multiple Register Read Operation

WRITING A SINGLE WORD

The master device asserts the start condition. The master then sends the 7-bit to the slave address. It is followed by a R/W bit that indicates the direction of operation, which will be a write operation in this case. The slave whose address is on the bus acknowledges it by an ACK signal on the bus (by holding SDA line low). The master then sends register address on the bus. The slave device accepts it by an ACK. The master then sends a data byte of the high byte of the register. The slave device asserts an acknowledge ACK on the SDA line. The master then sends a data byte of the low

byte of the register. The slave device asserts an acknowledge ACK on the SDA line. The master asserts a stop condition to end the transaction.

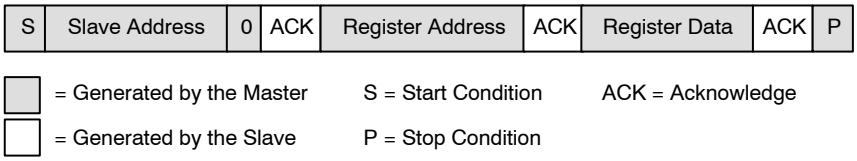


Figure 12. Single Register Write Operation

WRITING MULTIPLE WORDS TO DIFFERENT REGISTERS

The master device asserts the start condition. The master then sends the 7-bit slave address. It is followed by a bit (R/W) that indicates the direction of operation, which will be a write operation in this case. The slave whose address is on the bus acknowledges it by an ACK signal on the bus (by holding SDA line low).

The master then sends first register address on the bus. The slave device accepts it by an ACK. The master then sends a data byte of the high byte of the first register. The slave device asserts an acknowledge ACK on the SDA line. The master then sends a data byte of the low byte of the first register. The slave device asserts an acknowledge ACK on the SDA line.

The master then sends the second register address on the bus. The slave device accepts it by an ACK. The master then sends a data byte of the high byte of the second register. The slave device asserts an acknowledge ACK on the SDA line. The master then sends a data byte of the low byte of the second register. The slave device asserts an acknowledge ACK on the SDA line.

A complete word must be written to a register for proper operation. It means that both high and low bytes must be written.

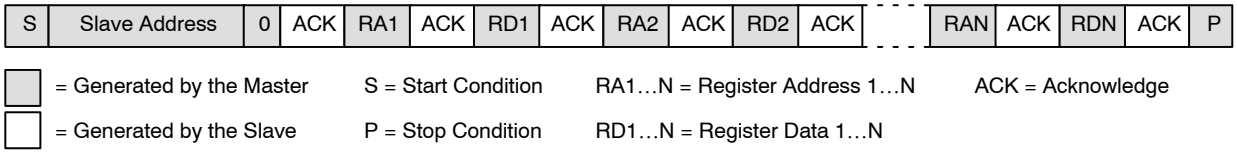


Figure 13. Multiple Register Write Operation

Table 10. REGISTER MAP

Address	R/W	Default Value	Description
0x20	R/W	0xFF	IOUT_OC_WARN_LIMIT
0x21	R	0x00	STATUS BYTE
0x22	R/W	0x00	Fault Mask
0x23	R	0x00	STATUS Fault
0x24	R	0x00	STATUS Warning
0x26	R	0x00	READ_IOUT
0x27	R	0x1A	MFR_ID
0x28	R	0x74	MFR_MODEL
0x29	R	0x04	MFR_REVISION
0x2A	R/W	0x00	Lock/Reset
0x2B	R	0x00	Soft Start Status
0x2C	N/A	0x00	Reserved
0x2D	R		Per phase OCP Status
0x2E	R/W	0x00	Per phase OCP Configuration
0x2F	R		Switching Frequency Status
0x30	R/W	0x00	Switching Frequency Configuration
0x31	N/A	0x00	Reserved
0x32	R		PSI Status
0x33	R		Phase Status
0x34	R/W	0x1F	LPC_Zone_enable
0x35	R		LPC Status
0x36	R/W	0x00	LPC Configuration
0x38	R		LL Status
0x39	R/W	0x03	LL Configuration
0x3A	RW	0x00	PHTH1 Configuration
0x3B	R		PHTH1 Status
0x3C	R/W	0x00	PHTH2 Configuration
0x3D	R		PHTH2 Status
0x3E	R/W	0x00	PHTH3 Configuration
0x3F	R		PHTH3 Status
0x40	R/W	0x00	PHTH4 Configuration
0x41	R		PHTH4 Status
0x44	R/W	0x08	Phase Shedding Hysteresis
0x45	R/W	0x14	Phase Shedding Delay
0x46	R/W	0x00	Second Function Configuration Register Latch A
0x47	R/W	0x00	Second Function Configuration Register Latch B
0x48	R		DLT_READBACK_1, Die Level Traceability
0x49	R		DLT_READBACK_2, Die Level Traceability
0x4A	R		DLT_READBACK_3, Die Level Traceability
0x4B	R		DLT_READBACK_4, Die Level Traceability
0x4C	R		DLT_READBACK_5, Die Level Traceability

IOUT_OC_WARN_LIMIT Register (0x20)

This sets the high current limit. Once the READ_IOUT register value exceeds this limit IOUT_OC_WARN_LIMIT bit is set in the Status Warning register and an ALERT is generated.

STATUS BYTE Register (0x21)

Table 11. STATUS BYTE REGISTER SETTINGS

Bits	Name	Description
7:6	Reserved	N/A
5	VOUT_OV	This bit gets set whenever the NCV81275A goes into OVP mode.
4	IOUT_OC	This bit gets set whenever the NCV81275A latches off due to an over current event.
0:3	Reserved	N/A

Fault Mask Register (0x22)

Table 12. FAULT MASK REGISTER SETTINGS

Bits	Name	Description
7:5	Reserved	
4	Clim1	When this bit is set, the Clim1 bit from the STATUS FAULT does not get set when an overcurrent event occurs.
3	Clim2	When this bit is set, the Clim2 bit from the STATUS FAULT does not get set when an overcurrent event occurs.
2	Clim_phase	When this bit is set, the Clim_phase bit from the STATUS FAULT register does not get set when an overcurrent event occurs.
1	OVP	When this bit is set, the OVP bit from the STATUS FAULT register does not get set when an overvoltage event occurs.
0	UVP	When this bit is set, the UVP bit from the STATUS FAULT register does not get set when an under voltage event occurs.

STATUS Fault Register (0x23)

Table 13. STATUS FAULT REGISTER SETTINGS

Bits	Name	Description
7:5	Reserved	N/A
4	Clim1	If not masked, this bit gets set when IOUT exceeds the ILIM value.
3	Clim2	If not masked, this bit gets set when IOUT exceeds the ILIM value.
2	Clim_phase	If not masked, this bit gets set when the phase Current (V_{CSN}–V_{CSREF}) exceeds the OCP configuration value.
1	OVP	If not masked, this bit is set when an OVP event is detected.
0	UVP	If not masked, this bit is set when an UVP event is detected.

STATUS Warning Register (0x24)

Table 14. STATUS WARNING REGISTER SETTINGS

Bits	Name	Description
7:1	Reserved	N/A
0	IOUT Overcurrent Warning Reserved	This bit gets set if IOUT exceeds its programmed high warning limit(register 0x20). This bit is only cleared when EN is toggled.

READ_IOUT Register (0x26)

Read back output current. ADC conversion 0xFF = 2 V on IOUT pin which should equate to max current.

Lock/Reset Register (0x2A)

Table 15. LOCK/RESET REGISTER SETTINGS

Bits	Name	Description
7:1	Reserved	N/A
0	Lock	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read-only and cannot be modified until the NCV81275A is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings (Lockable).

Soft Start Status Register (0x2B)

This register contains the value that sets the slew rate of the output voltage during power-up. When EN is set high, the controller reads the value of the resistor connected to the SS pin and sets the slew rate. The codes corresponding to each resistor setting are shown in Table 16. The resistor settings are updated on every rising edge of the EN signal.

Table 16. SOFT START STATUS REGISTER SETTINGS

T_{RAMP} Resistor (kΩ)	Bits	Name	Value	T_ramp (ms) REFIN =1 V	T_ramp (ms), REFIN =0.8 V
–	7:4	Reserved	N/A	N/A	N/A
10	3:0	T_Ramp	0000	0.15	0.12
14.7			0001	0.3	0.24
20			0010	0.45	0.36
26.1			0011	0.6s	0.48
33.2			0100	0.75	0.6
41.2			0101	0.9	0.72
49.9			0110	1	0.8
60.4			0111	2	1.6
71.5			1000	3	2.4
84.5			1001	4	3.2
100			1010	5	4
118.3			1011	6	4.8
136.6			1100	7	5.6
157.7			1101	8	6.4
182.1			1110	9	7.2
249			1111	10	8

NOTE: 1% tolerance.

Per Phase OCP Status Register and Configuration Register (0x2D, 0x2E)

These registers contain the values that set the per phase OCP current levels for each phase individually as well as the latch off delay time for the OCP event. When EN is set high, the controller reads the value of the resistor connected to the PWM7/OCP pin and sets the OCP threshold and latch off delay time according to Table 9. The codes corresponding to each setting are shown in Table 17. The resistor settings are updated on every rising edge of the EN signal.

The OCP configuration register (0x2E) allows the user to dynamically change the OCP threshold and latch off delay through the I^2C interface provided that the OCP bits from the second function configuration registers A and B (0x46, 0x47) are set. In addition, the OCP levels and latch off delay times can be adjusted independently when the OCP configuration register is used. The achievable switching frequency settings are listed in Table 17.

Table 17. OCP STATUS AND CONFIGURATION REGISTER SETTINGS

Bits	Name	Description
7:4	Reserved	N/A
3:2	Per Phase OCP Limit	00 = 65 mV 01 = 75 mV 10 = 100 mV 11 = 134 mV
1:0	OCP_latch Off Delay	00 = 4 ms 01 = 6 ms 10 = 8 ms 11 = 10 ms

Switching Frequency Status and Configuration Registers (0x2F, 0x30)

These registers contain the values that set the switching frequency of the controller. When EN is set high, the controller reads the value of the resistor connected to the FSW pin and sets the switching frequency according to Table 19. The codes corresponding to each setting are also shown in Table 19. The resistor settings are updated on every rising edge of the EN signal.

The switching frequency configuration register allows the user to dynamically change the switching frequency through the I^2C interface provided that the FSW bits from the second function configuration registers A and B (0x46, 0x47) are set.

PSI Status Register (0x32)

The PSI status register provides the information regarding the current status of the PSI pin though the I^2C interface as shown in Table 18.

Table 18. PSI STATUS REGISTER SETTINGS

Bits	Description
7:2	Reserved
1:0	00 = PSI MID 01 = PSI LOW 10 = PSI HIGH

Table 19. SWITCHING FREQUENCY STATUS AND CONFIGURATION REGISTER SETTINGS

FSW Pin Resistor Value (kΩ)	Bits	Value		Switching Frequency (kHz)							
		Status Register	Configuration Register	8 Phase	7 Phase	6 Phase	5 Phase	4 Phase	3 Phase	2 Phase	1 Phase
	7:5	Reserved	Reserved	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
10	4:0	0000	00000	221	253	295	355	221	293	223	232
		–	00001	244	276	330	399	244	329	243	252
14.7		0001	00010	266	309	355	425	266	358	264	272
		–	00011	293	327	387	460	293	381	294	297
20		0010	00100	307	351	412	501	307	407	317	322
		–	00101	333	384	441	542	333	450	335	340
26.1		0011	00110	351	409	480	561	351	480	352	361
		–	00111	373	431	499	615	373	510	380	385
33.2		0100	01000	394	451	528	639	394	530	399	413
		–	01001	421	481	559	676	421	562	420	435
41.2		0101	01010	449	495	593	725	449	600	436	456
		–	01011	469	525	612	746	469	614	454	478
49.9		0110	01100	479	563	639	757	479	631	483	500
		–	01101	509	570	681	799	509	663	508	509
60.4		0111	01110	518	588	697	831	518	688	526	518
		–	01111	543	617	722	874	543	722	543	540
71.5		1000	10000	581	665	779	930	581	789	583	578
		–	10001	649	718	881	1043	649	859	656	638
84.5		1001	10010	708	790	937	1129	708	930	698	698
		–	10011	751	868	1010	1211	751	1010	771	758
100		1010	10100	799	918	1073	1278	799	1095	807	818
		–	10101	866	1003	1136	1372	866	1147	860	878
118.3		1011	10110	919	1025	1220	1449	919	1233	899	938
		–	10111	964	1111	1297	1533	964	1260	950	972
136.6		1100	11000	993	1140	1339	1610	993	1341	1003	1014
		–	11001	1059	1198	1438	1687	1059	1372	1052	1067
157.7		1101	11010	1098	1262	1485	1734	1098	1450	1096	1106
		–	11011	1141	1295	1533	1821	1141	1539	1154	1155
182.1		1110	11100	1200	1338	1587	1890	1200	1619	1205	1201
		–	11101	1236	1405	1608	1954	1236	1618	1227	1245
249		1111	11110	1291	1459	1707	2012	1291	1674	1274	1280
		–	11111	1312	1493	1724	2096	1312	1724	1316	1330

NOTE: 1% tolerance.

Phase Status Register (0x33)

The Phase Status register provides the information about the status of each of the eight available phases as shown in Table 20.

Table 20. PHASE STATUS REGISTER SETTINGS

Bits	Name	Description
7	Phase 8	0 = Disabled 1 = Enabled
6	Phase 7	0 = Disabled 1 = Enabled
5	Phase 6	0 = Disabled 1 = Enabled
4	Phase 5	0 = Disabled 1 = Enabled
3	Phase 4	0 = Disabled 1 = Enabled
2	Phase 3	0 = Disabled 1 = Enabled
1	Phase 2	0 = Disabled 1 = Enabled
0	Phase 1	0 = Disabled 1 = Enabled

LPC_Zone_enable Register (0x34)

The LPC_Zone_enable register allows the user to enable or disable power zones while the controller has the PSI set low using the I^2C interface as shown in Table 21.

Table 21. LPC_ZONE_ENABLE REGISTER SETTINGS

Bits	Name	Description
7:4	Reserved	N/A
4	Zone 4	0 = Disabled 1 = Enabled
3	Zone 3	0 = Disabled 1 = Enabled
2	Zone 2	0 = Disabled 1 = Enabled
1	Zone 1	0=Disabled 1=Enabled
0	Zone 0	0 = Disabled 1 = Enabled

LPC Status and Configuration Registers (0x35, 0x36)

These registers contain the values that set the operating power zone when the PSI pin is set low. When EN is set high, the controller reads the value of the resistor connected to the PWM6/LPC1 and PWM5/LPC2 pins and sets the power zone according to Table 7. The LPC_X resistor settings are updated on every rising edge of the EN signal. LPC status register 0x35 records the status of LPC2(Bit[2:0]) and LPC1(Bit[5:3]) resistor setting during startup. The status register value won't change afterwards.

The LPC configuration register (0x36) allows the user to dynamically change the power zone (PSI = Low) through the I^2C interface provided that the LPC bits from the second function configuration registers A and B (0x46, 0x47) are set. The achievable power zone settings are listed in Table 22.

Table 22. CONFIGURATION REGISTER SETTINGS

Bits	Name	Value	Level
7:6	Reserved	N/A	N/A
5:3	LPC2 Configuration	000 (default)	0
		001	1
		010	2
		011	3
		100	4
		101 = Reserved	N/A
		110 = Reserved	N/A
		111 = Reserved	N/A
2:0	LPC1 Configuration	000 (default)	0
		001	1
		010	2
		011	3
		100	4
		101 = Reserved	N/A
		110 = Reserved	N/A
		111 = Reserved	N/A

LL Status and Configuration Registers (0x38, 0x39)

These registers contain the values that set the fraction of the externally configured load line (see Total Current Sense Amplifier section) to be used during the normal operation of the device. When EN is set high, the controller reads the value of the resistor connected to the LL/I2C_ADD pin and sets the load line according to Table 5. The codes corresponding to each setting are shown in Table 23. The load line resistor setting is updated on every rising edge of the EN signal.

The LL configuration register allows the user to dynamically change the load line settings through the I^2C interface provided that the LL bits from the second function configuration registers A and B (0x46, 0x47) are set. The achievable load line settings are listed in Table 23.

Table 23. LL STATUS AND CONFIGURATION REGISTER SETTINGS

Bits	Description
7:2	Reserved
1:0	00 = 100% of externally set load line (default) 01 = 50% of externally set load line 10 = 25 of externally set load line 11 = 0% of externally set load line

PHTH1 to PHTH4 Configuration Registers (0x3A, 0x3C, 0x3E, 0x40)

These registers contain the values that control the phase shedding thresholds and are active when the $PHTH_X$ bits from the second function configuration registers A and B (0x46 and 0x47) are set be set. These thresholds allow the user to dynamically change the thresholds through the I^2C interface. The values written to these registers should match the value of the READ_IOUT register (0x26) at the desired load current. If 0xFF is written to a register, the phase shedding threshold corresponding to that register is disabled.

PHTH1 to PHTH4 Status Registers (0x3B, 0x3D, 0x3F 0x41)

These registers contain the phase shedding threshold values set by the resistors connected to the $PHTH_X$ pins. The values of the thresholds are updated on every rising edge of the EN signal. The resistor values should be chosen to ensure that the voltage drop across them developed by the 10 μA current sourced by the NCV81275A during power-up (EN set high) matches the value of the READ_IOUT register (0x26) at the desired load current. Setting the resistors to generate a voltage above 2 V will disable the $PHTH_X$ threshold for that pin.

Phase Shedding Hysteresis Register (0x44)

This register sets the hysteresis during a transition from a high count phase to a low count phase configuration. The hysteresis is expressed in codes (LSBs) of the $PHTH_X$ threshold values, by default its value is 08H.

Phase Shedding Delay Register (0x45)

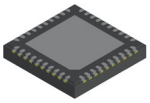
This register sets the delay during a transition from a high count phase to a low count phase configuration. The power-up default value is 200 μs (14H) and it can be dynamically changed in steps of 10 μs (1 LSB) through the I^2C interface.

Second Function Configuration Register Latch A and B Registers (0x46, 0x47)

These registers allow the user to select whether the second functions settings (LL, Soft Start, OCP, LPC and $PHTH_X$) are controlled by the external resistors or the configuration registers (see Table 24). When/EN is toggled the default control mode for the second functions is the external resistor. Switching between the two modes can be done by simply writing the appropriate byte (the same byte) to both registers (the order doesn't matter).

Table 24. SECOND CONFIGURATION LATCH REGISTER A AND B

Bits	Second Function Configuration Register	Description
7:6	Reserved	N/A
5	FSW	0 = set by external resistor (see Table 19) 1 = set by register 0x30 (see Table 19)
4	LL	0 = set by external resistor (see Table 5) 1 = set by register 0x39
3	Reserved	N/A
2	OCP	0 = set by external resistor (see Table 9) 1= set by register 0x2E
1	LPC1, LPC2	0 (default) = low power zone set by external resistor 1 = low power zone set by register 0x36
0	$PHTH_X$	0 = set by external resistors connected between $PHTH_X$ pins and GND 1 = set by registers 0x3A, 0x3C, 0x3E and 0x40



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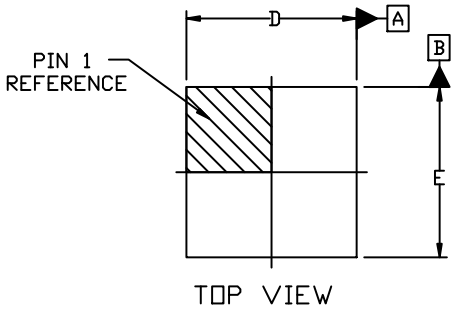
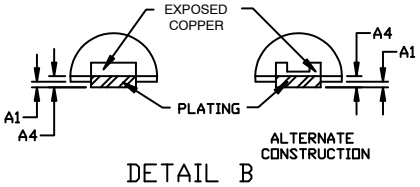
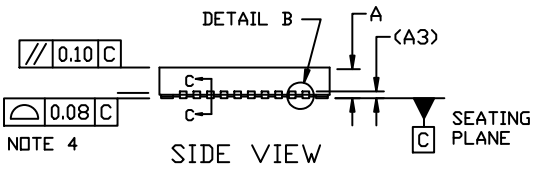


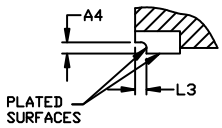
NOTES:

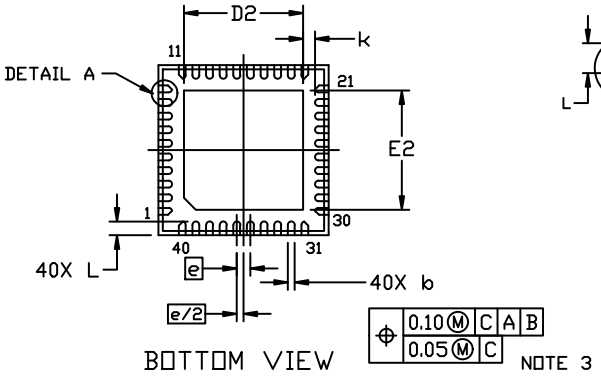
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

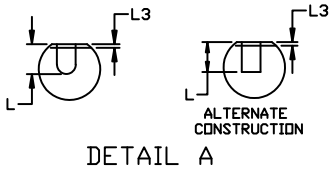


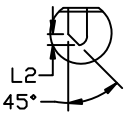
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	---	0.05
A3		0.20 REF	
A4	0.10	---	---
b	0.15	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
e		0.40 BSC	
K		0.35 REF	
L	0.30	0.40	0.50
L2		0.12 REF	
L3	---	---	0.09

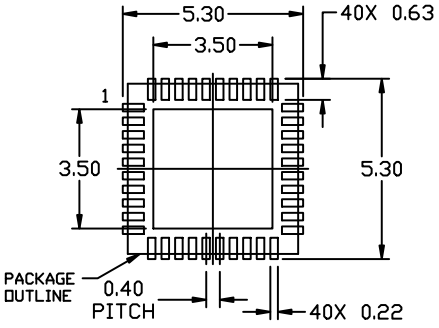






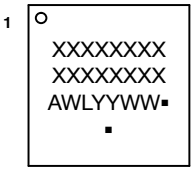






* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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