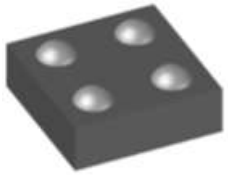
256 Kb I²C CMOS Serial EEPROM with Software Write Protect N24C256X



WLCSP4
CASE 567XG

Description

The N24C256X is a 256 Kb Serial CMOS EEPROM, internally organized as 32,768 words of 8 bits each.

It features a 64−byte page write buffer and supports the Standard (100 kHz), Fast (400 kHz) and Fast−Plus (1 MHz) I²C protocol.

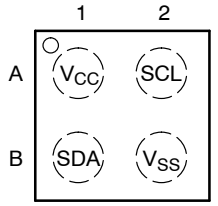
The device also features a 128−bit factory−set read−only Unique ID and Software Write Protection of the entire array. The Unique ID may be used to identify the manufacturer and the device.

Features

- Supports Standard, Fast and Fast−Plus I²C Protocol
- SCL and SDA Pins Operate at 1.2 V
- 1.7 V to 5.5 V Supply Voltage Range
- 64−Byte Page Write Buffer
- User Programmable Permanent Write Protection
- Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Temperature Range: −40°C to +125°C
- Ultra−thin 4−ball WLCSP Package
- This Device is Pb−Free, Halogen Free/BFR Free and RoHS Compliant*

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PIN CONFIGURATION

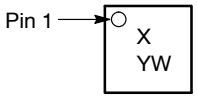


WLCSP4 1.00x1.00x0.30
(Top View)

PIN FUNCTION

Pin Name	Function
SDA	Serial Data Input/Output
SCL	Serial Clock Input
V_{CC}	Power Supply
V_{SS}	Ground

MARKING DIAGRAM



X = Specific Device Code
Y = Production Year (Last Digit)
W = Production Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

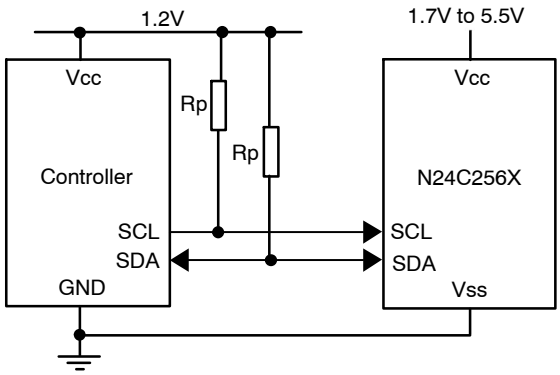


Figure 1. Functional Symbol and Typical Application

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter		Rating	Units
Storage Temperature Range		−65 to +150	°C
Operational Temperature Range		−40 to +125	°C
Voltage on Any Pin with Respect to Ground (Note 1)		−0.5 to +6.5	V
Electrostatic pulse (VESD)	HBM − Human Body Model (Note 2)	2000	V
	CDM − Charged Device Model	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. During transitions with V_{CC} = 1.7 V to 5.5 V, the voltage on any pin may undershoot to no less than −1.0 V or overshoot to no more than V_{CC} + 1.0 V, for periods of less than 20 ns.
2. Positive and negative pulses applied on different combinations of pin connections, according to AEC−Q100−002 (compliant with ANSI/ESDA/JEDEC JS−001−2012, C1 = 100 pF, R1 = 1500 Ω).

Table 2. RELIABILITY CHARACTERISTICS (Note 3)

Symbol	Parameter	Min	Units
N_{END} (Note 4)	Endurance	1,000,000	Program/Erase Cycles
T_{DR} (Note 4)	Data Retention	100	Years

3. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
4. Page Mode, V_{CC} = 5 V, T_A = 25°C

Table 3. DC AND AC OPERATING CHARACTERISTICS

Supply Voltage / Temperature Range	Operation
V_{CC} = 1.7 V to 5.5 V, T_A = −40°C to +125°C	READ / WRITE

Table 4. D.C. OPERATING CHARACTERISTICS (Vcc = 1.7 V to 5.5 V, Ta = −40 to +125°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CCR}	Read Current	Read, f_{SCL} = 400 kHz/1 MHz		1	mA
I_{CCW}	Write Current			2.5	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}		2	μA
I_L	I/O Pin Leakage	Pin at GND or V_{CC}		2	μA
V_{IL}	Input Low Voltage		−0.5	0.24	V
V_{IH}	Input High Voltage		0.96	5.5	V
V_{HYS}	Input Hysteresis Voltage		90		mV
V_{OL}	Output Low Voltage	I_{OL} = 3.0 mA		0.4	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. PIN IMPEDANCE CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Units
C_{IN} (Note 5)	SDA I/O Pin Capacitance	V_{IN} = 0 V		8	pF
C_{IN} (Note 5)	Input Capacitance (other pins)	V_{IN} = 0 V		6	pF

5. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.

Table 6. A.C. CHARACTERISTICS (Note 6)

Symbol	Parameter	Standard		Fast		Fast−Plus		Units
		Min	Max	Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400		1,000	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		0.26		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		0.50		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		0.26		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		0.26		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		50		ns
t_R (Note 7)	SDA and SCL Rise Time		1,000	20	300		100	ns
t_F (Note 7)	SDA and SCL Fall Time		300	20	300		100	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		0.25		μs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		0.5		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9		0.45	μs
t_{DH}	Data Out Hold Time	100		100		50		ns
T_i (Note 7)	Noise Pulse Filtered at SCL and SDA Inputs		50		50		50	ns
t_{WR}	Write Cycle Time		5		5		5	ms
t_{PU} (Notes 7, 8)	Power−up to Ready Mode		0.8		0.8		0.8	ms

6. Test conditions according to “A.C. Test Conditions” table.
7. Tested initially and after a design or process change that affects this parameter.
8. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

Table 7. A.C. TEST CONDITIONS

Input Levels, V	0.18, 1.02
Input Rise and Fall Times, ns	≤ 50
Input Reference Levels (V_{ILmax}, V_{IHmin}), V	0.24, 0.96
Output Reference Levels, V	0.6
Output Load	Current Source: I_{OL} = 1 mA; C_L = 100 pF

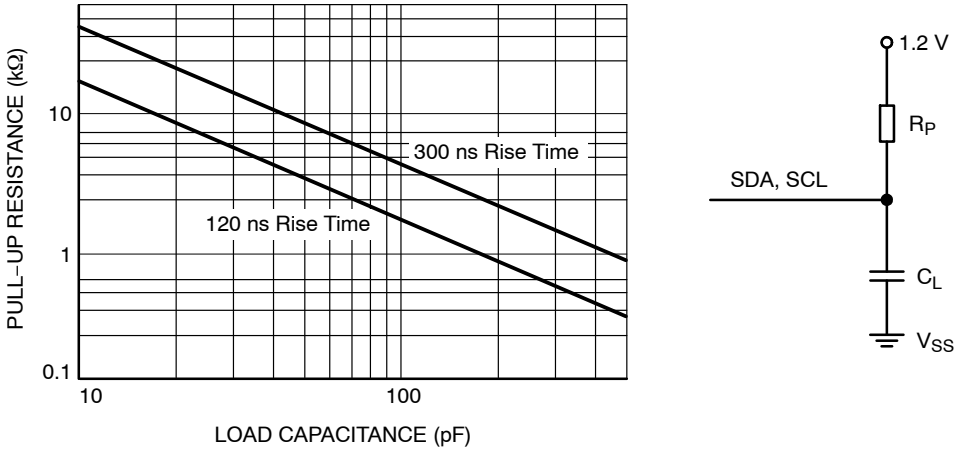


Figure 2. Maximum Pull−up Resistance vs. Load Capacitance

Power−On Reset (POR)

The N24C256X incorporates Power−On Reset (POR) circuitry which protects the device against powering up in the wrong state.

The N24C256X will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi−directional POR feature protects the device against ‘brown−out’ failure following a temporary loss of power.

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

Functional Description

The N24C256X supports the Inter−Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The N24C256X acts as a Slave device. Master and Slave alternate as either transmitter or receiver.

I^2C Bus Protocol

The I^2C bus consists of two ‘wires’, SCL and SDA. The two wires are connected to the 1.2 V supply via pull−up resistors. Master and Slave devices connect to the 2−wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to ‘transmit’ a ‘0’ and releases it to ‘transmit’ a ‘1’.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 3). The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a ‘wake−up’ call to all receivers. Absent a START, a Slave will not respond to commands. The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH.

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8−bit serial Slave address. The first 7 bits of the Slave address are set to 1010001, for normal Read/Write operations, and to 1011001 for special Read/Write operations (Figure 4). The last bit, R/$\overline{W}$, specifies whether a Read (1) or Write (0) operation is to be performed.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9^{th} clock cycle (Figure 5). The Slave will also acknowledge all address bytes and every data byte presented in Write mode if the addressed location is not write protected. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9^{th} clock cycle. As long as the Master acknowledges the data, the Slave will continue transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by issuing a STOP condition. Bus timing is illustrated in Figure 6.

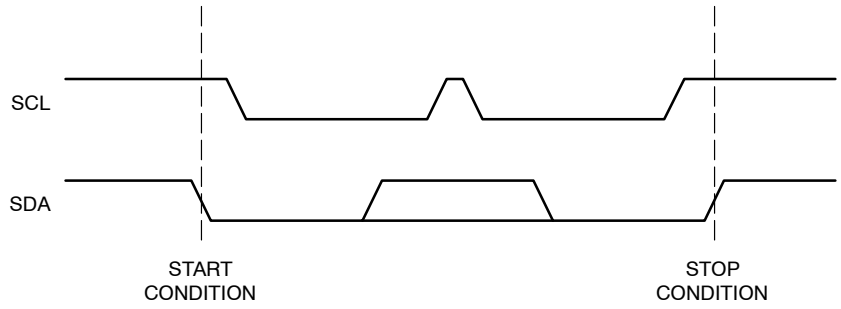


Figure 3. Start/Stop Conditions

					DEVICE ADDRESS			
Memory Array Access	1	0	1	0	0	0	1	R/W
UID, Device Config.	1	0	1	1	0	0	1	R/W

Figure 4. Slave Address Bits

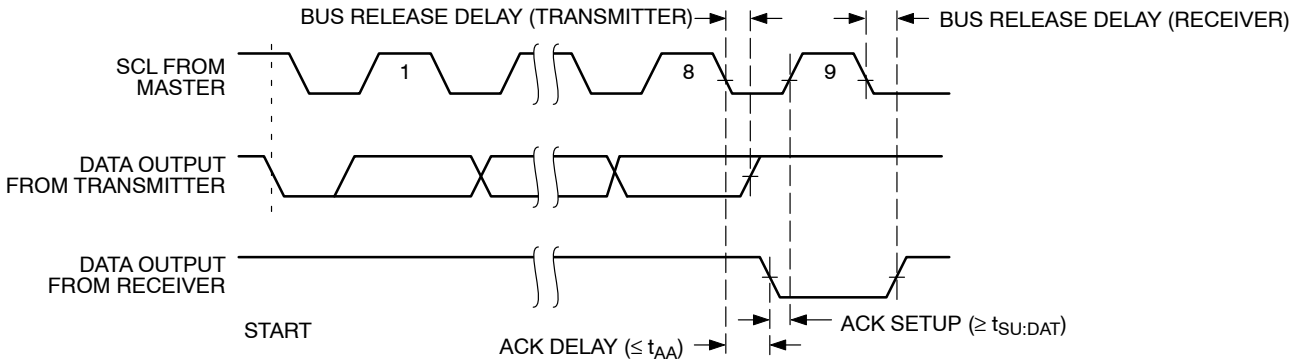


Figure 5. Acknowledge Timing

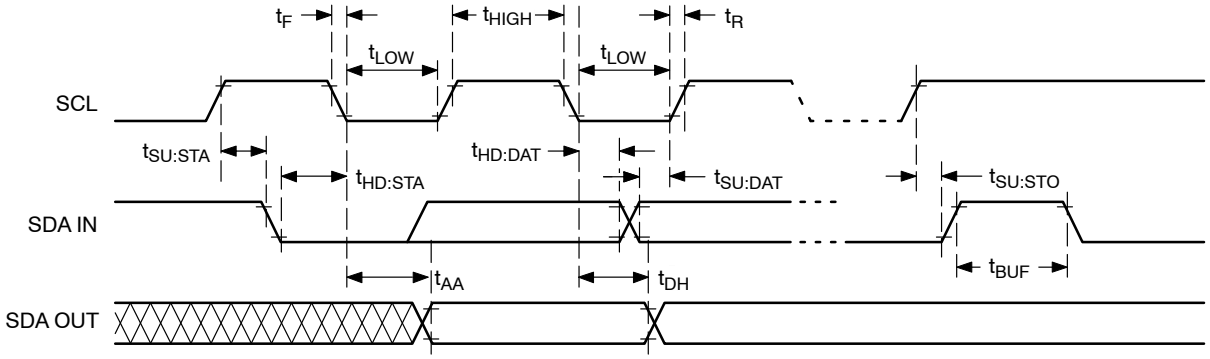


Figure 6. Bus Timing

WRITE OPERATIONS

Byte Write

In Byte Write mode the Master sends a START, followed by Slave address, two byte address (Table 8) and data to be written (Figure 7). The Slave, N24C256X acknowledges all 4 bytes, and the Master then follows up with a STOP, which in turn starts the internal Write operation (Figure 8).

During the internal Write cycle (t_{WR}), the N24C256X will not acknowledge any Read or Write request from the Master.

Page Write

The N24C256X contains 32,768 bytes of data, arranged in 512 pages of 64 bytes each. A two byte address word (Table 8), following the Slave address, points to the first byte to be written into the memory array. The most significant 9 bits from the address active bits (a14 to a6) identify the page and the last 6 bits (a5 to a0) identify the byte within the page. Up to 64 bytes can be written in one Write cycle (Figure 9). The internal byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 64 data bytes, then earlier bytes will be overwritten by later bytes in a 'wrap−around' fashion (within the selected page). The internal Write cycle starts immediately following the STOP.

Acknowledge Polling

The ready/busy status of the N24C256X can be ascertained by sending Read or Write requests immediately following the STOP condition that initiated the internal Write cycle. As long as internal Write is in progress, the N24C256X will not acknowledge the Slave address. The Device Configuration Register Write instruction does not support acknowledge polling. Following this instruction, the master must wait t_{WR} = 5 ms before sending a new instruction.

Device Configuration Register Write

The Device Configuration Register Write instruction is similar to a Byte Write instruction. The user must address the device with the header 1011b followed by the 001 bits. The second byte consists of xxxx x11x, where x is don't care. The third byte is don't care.

The SWP bit of the data byte following the address will be written into the Device Configuration Register (see Table 9 for the position of each bit.).

The SWP bit is the Software Write Protection bit. Once SWP is set to 1, the entire memory array and the Device Configuration Register are protected permanently against write operations.

Table 8. BYTE ADDRESS

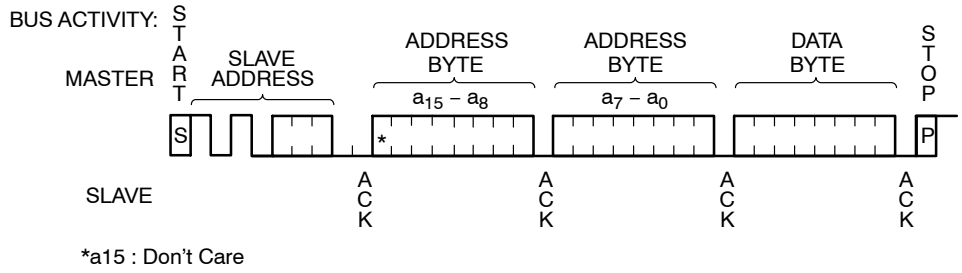
	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Memory Array	x	a14	a13	a12	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0
Unique ID Number	x	x	x	x	x	0	1	x	x	x	x	x	0	0	0	0
Device Configuration	x	x	x	x	x	1	1	x	x	x	x	x	x	x	x	x

NOTE: Command with A9=0 for header 0x0B is undefined.

9. For the write command with header 0x0B (1011b) in Figure 4, if A9=0 in Table 8, N24C256X responds with NOACK after the first data byte and enters in reset mode.
10. For the Read Command with header 0x0B (1011b) in Figure 4, if A9=0 in Table 8, N24C256X responds with NOACK after Read command byte and enters in reset mode.

Table 9. DEVICE CONFIGURATION REGISTER

b7	b6	b5	b4	b3	b2	b1	b0
0	0	1	x	x	x	SWP	x



*a15 : Don't Care

Figure 7. Byte Write Sequence

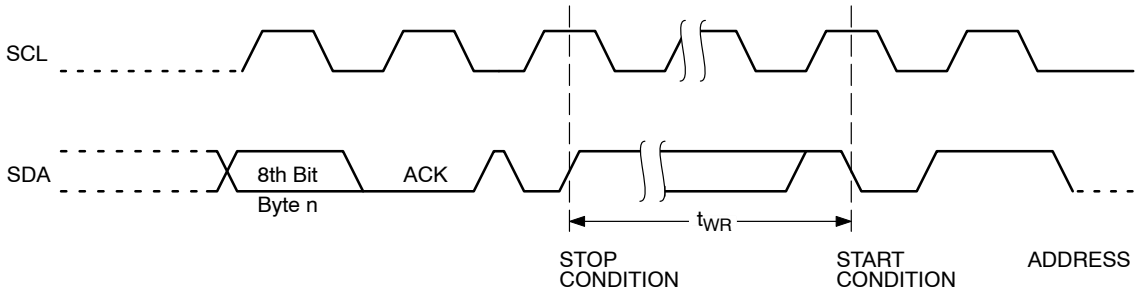
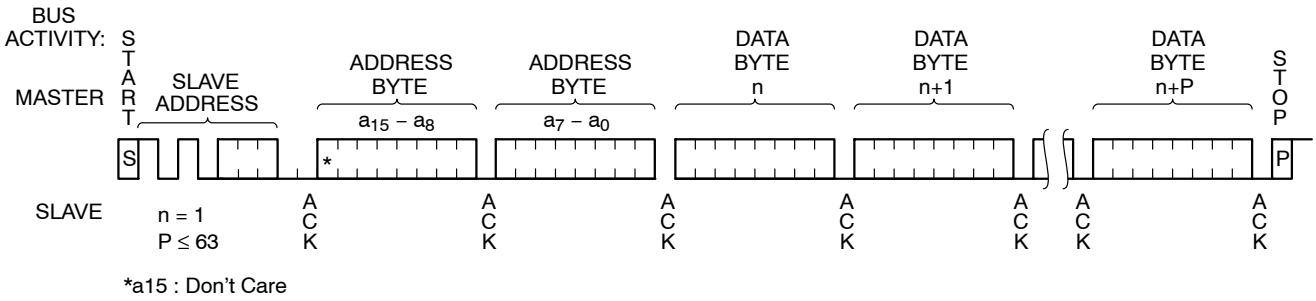


Figure 8. Write Cycle Timing



*a15 : Don't Care

Figure 9. Page Write Sequence

READ OPERATIONS

Immediate Read

Upon receiving a Slave address with the R/$\overline{W}$ bit set to '1', the N24C256X will interpret this as a request for data residing at the current byte address in memory. The N24C256X will acknowledge the Slave address, will immediately shift out the data residing at the current address, and will then wait for the Master to respond. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 10), the N24C256X returns to Standby mode.

Selective Read

To read data residing at a specific location, the internal address counter must first be initialized as described under Byte Write. If rather than following up the two address bytes with data, the Master instead follows up with an Immediate Read sequence, then the N24C256X will use the 15 active address bits to initialize the internal address counter and will shift out data residing at the corresponding location. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 11), the N24C256X returns to Standby mode.

Sequential Read

If during a Read session the Master acknowledges the 1st data byte, then the N24C256X will continue transmitting data residing at subsequent locations until the Master responds with a NoACK, followed by a STOP (Figure 12). In contrast to Page Write, during Sequential Read the address count will automatically increment to and then wrap−around at end of memory (rather than end of page).

Device Configuration Register Read

The Device Configuration Register Read instruction is similar to a Selective Read instruction. The user must send the device header and the two address bytes as for a Device Configuration Register Write instruction. This dummy write instruction is followed by an Immediate Read with the device header 1011b, and the device will shift back the content of the Device Configuration Register. Don't care bits are read as 1s.

If the master acknowledges the data byte, requesting more data, the device will continue to return the content of the Device Configuration Register until the Master responds with a NoACK.

Unique ID Number Read

The Unique ID Number Read instruction is similar to a Sequential Read instruction. The user must send the device header starting with 1011b followed by the 001 bits. As specified in Table 8, the second byte consists of xxxx x01x and the third byte if xxxx 0000, where x is don't care. This dummy write instruction is followed by an Immediate Read with the device header 1011b, and the device will shift back the Unique ID byte by byte. The Unique ID is 16 bytes (128 bits) long. The first byte contains the manufacturer ID and the second byte contains the device ID (Figure 13). After the last byte of the Unique ID has been shifted, if the master acknowledges (requesting more data), the device will wrap−around and start returning the Unique ID from the beginning.

Delivery State

The N24C256X is shipped erased, i.e., all memory array bytes are FFh and the settable Device Configuration SWP bit set to 0 (3Dh).

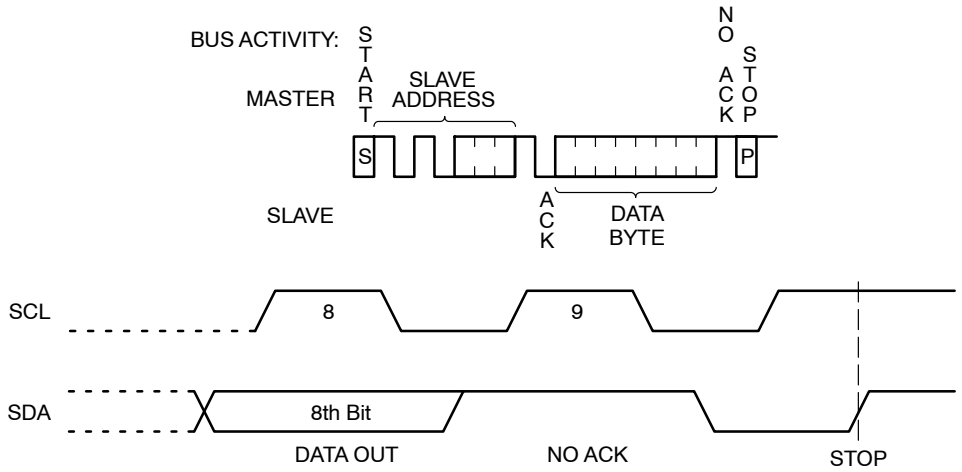


Figure 10. Immediate Read Sequence and Timing

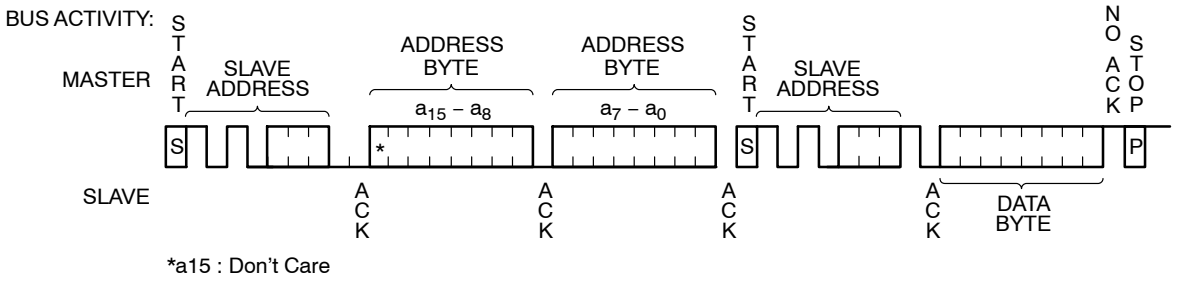


Figure 11. Selective Read Sequence

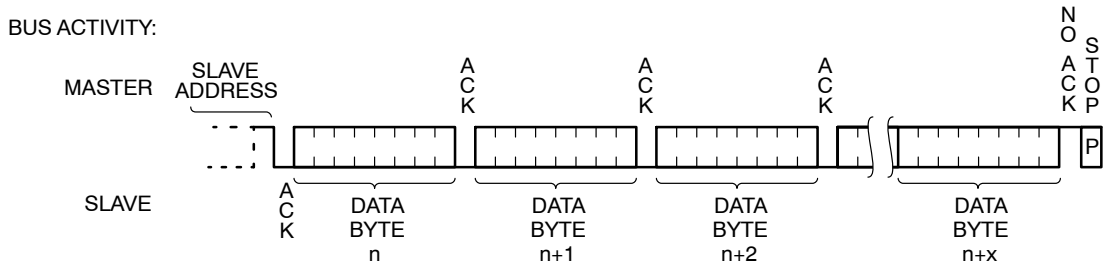


Figure 12. Sequential Read Sequence

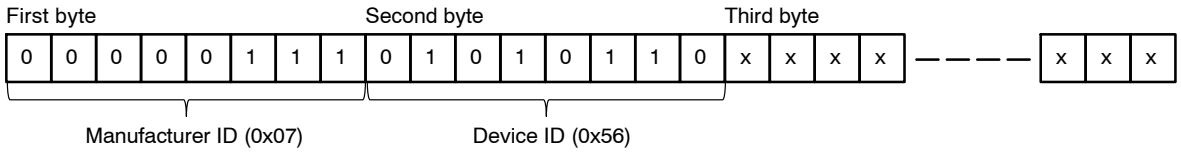


Figure 13. Unique ID Content

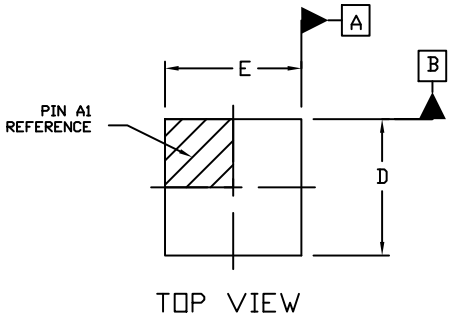
ORDERING INFORMATION (Notes 11 thru 14)

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Shipping
N24C256X−1CBT5G	J	WLCSP 4−ball	Industrial (−40°C to +125°C)	Tape & Reel, 5,000 Units / Reel

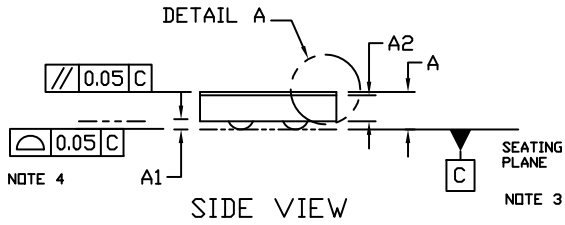
11. All packages are RoHS−compliant (Lead−free, Halogen−free).
12. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
13. For detailed information and a breakdown of device nomenclature and numbering systems, please see the **onsemi** Device Nomenclature document, TND310/D, available at www.onsemi.com
14. **Caution: The EEPROM devices delivered in WLCSP must never be exposed to ultra violet light. When exposed to ultra violet light the EEPROM cells lose their stored data.**

PACKAGE DIMENSIONS

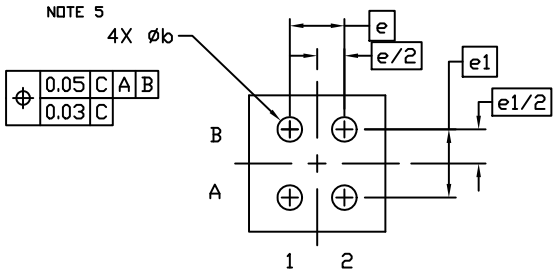
WLCSP4 1.00x1.00x0.30
CASE 567XG
ISSUE O



TOP VIEW



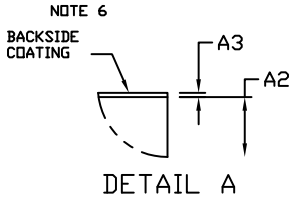
SIDE VIEW



BOTTOM VIEW

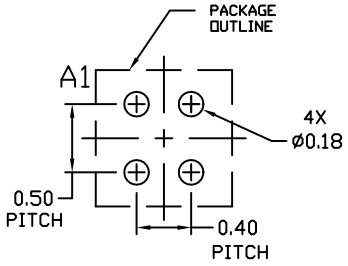
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.



DETAIL A

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	0.30
A1	0.040	0.060	0.080
A2		0.190 REF	
A3		0.025 REF	
b	0.16	0.18	0.20
D	0.98	1.00	1.02
E	0.98	1.00	1.02
e		0.40 BSC	
e1		0.50 BSC	



RECOMMENDED
MOUNTING FOOTPRINT

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales