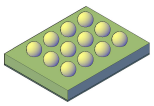
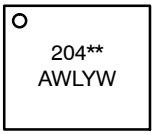
Battery Fuel Gauge LSI [Smart LiB Gauge] for 1-Cell Lithium-ion/ Polymer (Li+) with Low Power 2 μA Operation

LC709204V



WLCSP12 1.48x1.91x0.51
CASE 567XE

MARKING DIAGRAM



204**	= 20401 (LC709204VXE−01TBG)
A	= Assembly Site
WL	= Wafer Lot Number
YW	= Assembly Start Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 17 of this data sheet.

Overview

LC709204V is a Fuel Gauge for 1−Cell Lithium−ion/Polymer batteries. It is part of our ***Smart LiB Gauge*** family of Fuel Gauges which measure the battery RSOC (Relative State Of Charge) using its unique algorithm called **HG−CVR2**. The **HG−CVR2** algorithm provides accurate RSOC information even under unstable conditions (e.g. changes of battery; temperature, loading, aging and self−discharge). An accurate RSOC contributes to the operating time of portable devices. The Fuel Gauge (in other words, Gas Gauge, Battery Monitor or Battery Gauge) feature of **HG−CVR2** algorithm makes LSI highly applicable in various application. The LSI can immediately start battery measurement by setting a few parameters after battery insertion. Learning cycles that make complicated manufacturing process of applications can be avoided. The operating consumption current is very low 2 μA and it is suitable for applications such as wearables and 1series N parallel batteries.

Features

- **HG−CVR2** Algorithm Technology
  - Small Footprint: No Need for Current Sensing Resistor
  - Accurate RSOC of Aging Battery
  - Stable Gauging by Automatic Convergence of Error
  - Immediate Accurate Gauging after Battery Insertion
  - Eliminates Learning Cycle
- Low Power Consumption
  - 2 μA Operational Mode Current
- Improvement of the Battery Safety by Alarm Function RSOC / Voltage
- Two Temperature Inputs
  - Inputs to sense NTC Thermistor
  - Via I^2C
- Detection of Battery Insertion
- I^2C Interface (supported up to 400 kHz)
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Wearables / IoT Devices
- Smartphones / PDA Devices
- Digital Cameras
- Portable Game Players
- USB-related Devices

APPLICATION CIRCUIT EXAMPLE

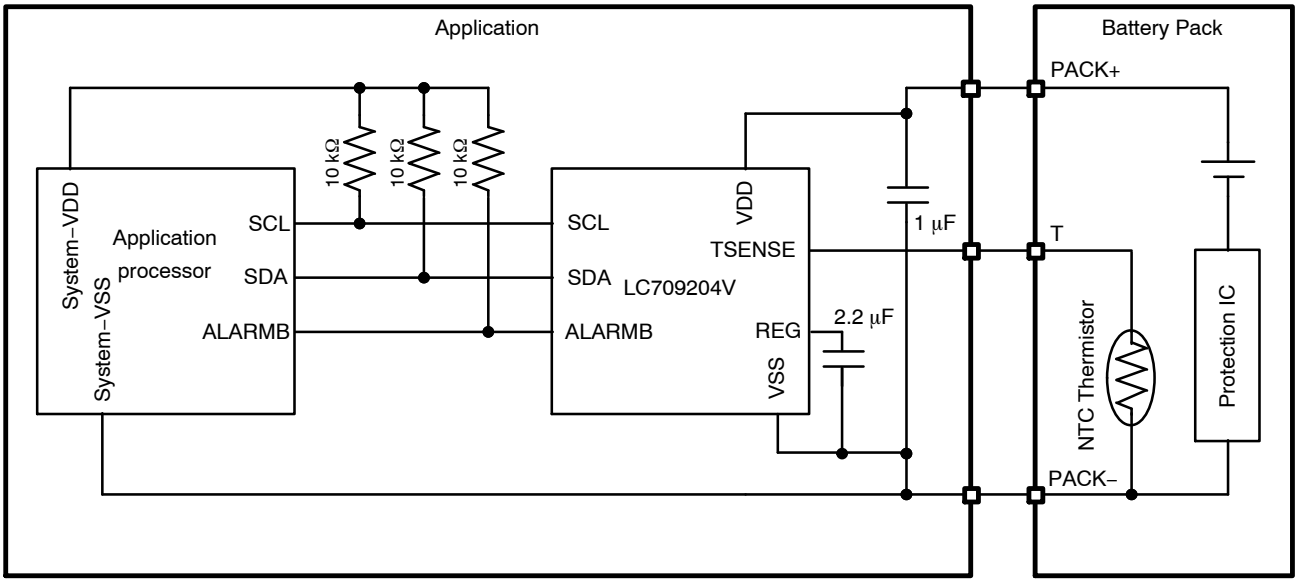


Figure 1. Example of an Application Schematic using LC709204V (The Temperature is Measured Using TSENSE Pin)

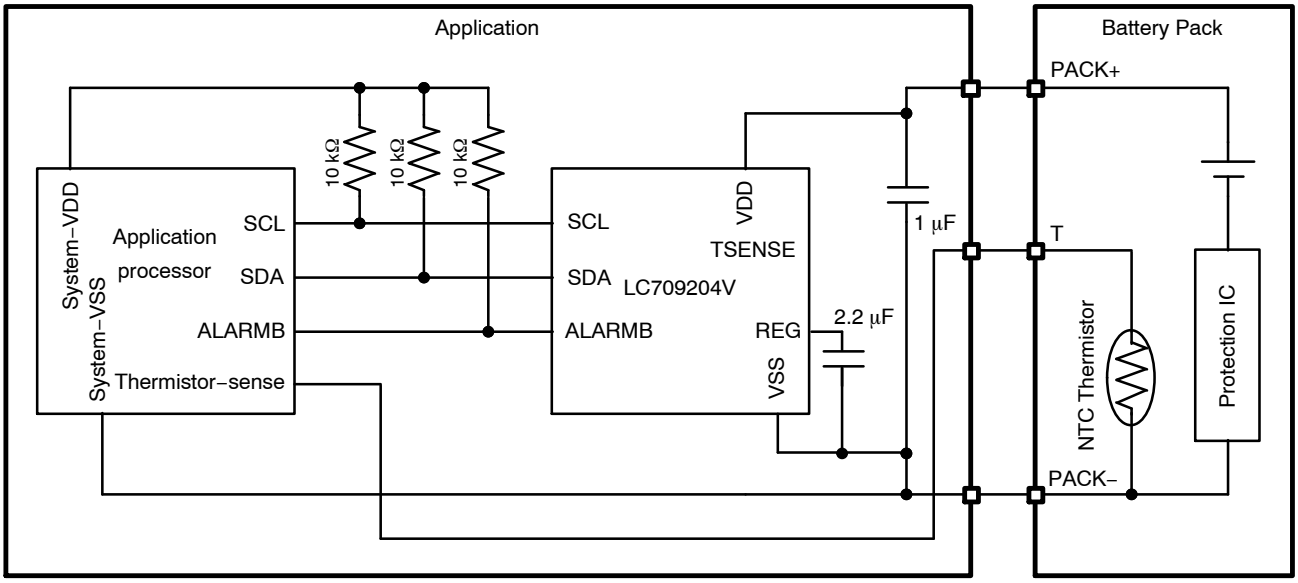


Figure 2. Example of an Application Schematic using LC709204V (The Temperature is Sent via I^2C)

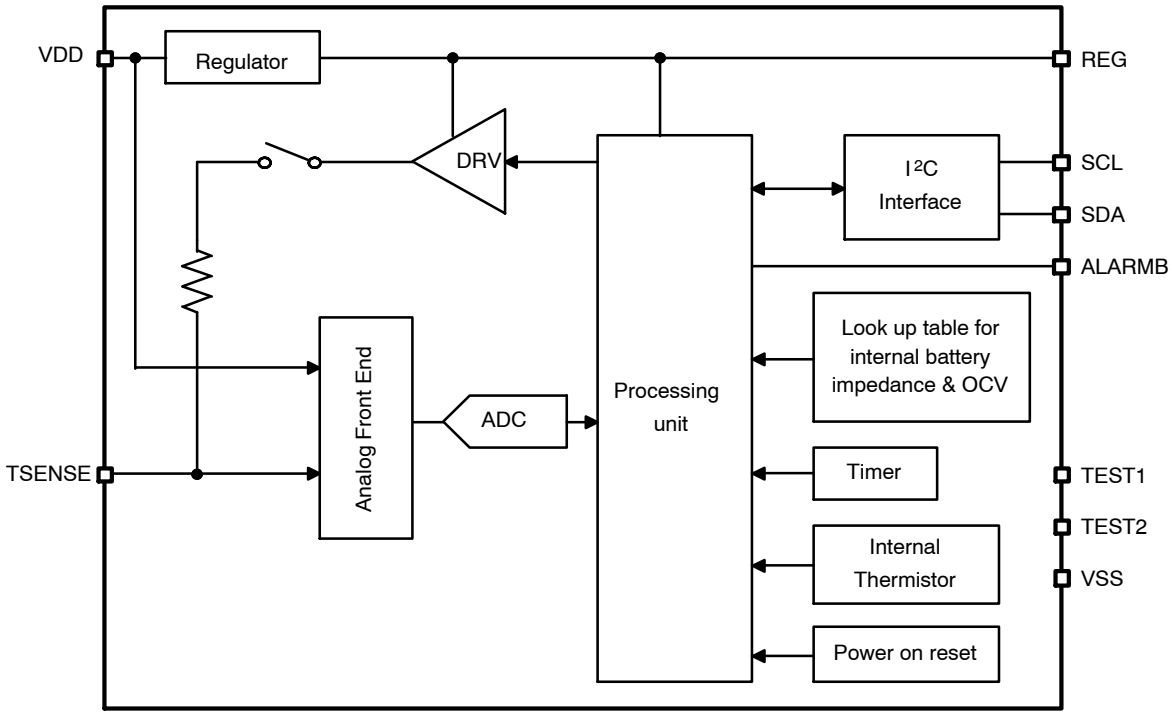
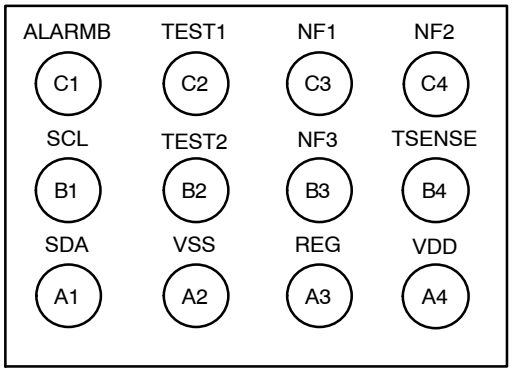


Figure 3. Block Diagram



(Bottom View)

Figure 4. Pin Assignment

Table 1. PIN FUNCTION

WLCSP12	Name	I/O	Description
A1	SDA	I/O	I²C Data pin (open drain). Pull−up must be done externally.
B1	SCL	I/O	I²C Clock pin (open drain). Pull−up must be done externally.
C1	ALARMB	O	This pin indicates alarm by low output (open drain). Pull−up must be done externally. Keep this pin OPEN when not in use.
A2	V_{SS}	−	Connect this pin to the battery's negative (−) pin.
B2	TEST2	I	Connect this pin to the battery's negative (−) pin.
C2	TEST1	I	Connect this pin to the battery's negative (−) pin.
A3	REG	O	Regulator output. Connect this pin to the capacitor.
B3	NF3	−	No function pin. Keep this pin OPEN.
C3	NF1	−	No function pin. Keep this pin OPEN.
A4	VDD	−	Connect this pin to the battery's positive (+) pin.
B4	TSENSE	I/O	Sense input and power supply for a thermistor. Connect 10 kΩ NTC thermistor to measure "Cell temperature (0x08)". Keep this pin OPEN when not in use.
C4	NF2	−	No function pin. Keep this pin OPEN.

Table 2. ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} (V)	Specification			Unit
					Min	Typ	Max	
Maximum Supply Voltage	V_{DD} max	VDD		−	−0.3	−	+6.5	V
Input Voltage	V_I (1)	ALARMB, SDA, SCL, NF1, NF2, NF3		−	−0.3	−	+6.5	
Output Voltage	V_O (1)	REG, TSENSE		−	−0.3	−	+4.6	
Allowable Power Dissipation	Pd max		T_A = −40 to +85°C	−	−	−	150	mW
Operating Ambient Temperature	Taopr			−	−40	−	+85	°C
Storage Ambient Temperature	Tstg			−	−40	−	+125	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. ALLOWABLE OPERATING CONDITIONS (T_A = −40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} (V)	Specification			Unit
					Min	Typ	Max	
Operating Supply Voltage	V_{DD} (1)	VDD		−	2.5	−	5.0	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS (T_A = −40 to +85°C, V_{SS} = 0 V, Typ: 4 V, T_A = 25°C)

Parameter	Symbol	Pin/ Remarks	Conditions	V_{DD} [V]	Specification			Unit
					Min	Typ	Max	
LDO								
LDO Output Voltage	V_{REG}	REG		2.5 to 5.0	2.3	2.7	3.0	V
CONSUMPTION CURRENT								
Operational Mode	I_{DD} (1)	VDD	Ta = −20°C to +70°C Average current with 0.01C Constant discharge.	2.5 to 5.0	−	2	−	μA
Sleep Mode	I_{DD} (2)		Ta = −20°C to +70°C	2.5 to 5.0	−	1.3	−	
INPUT / OUTPUT								
High Level Input Voltage	V_{IH}	ALARMB, SDA, SCL		2.5 to 5.0	1.4	−	5.5	V
Low Level Input Voltage	V_{IL}	ALARMB, SDA, SCL		2.5 to 5.0	−	−	0.5	
High Level Input Current	I_{IH}	ALARMB, SDA, SCL, NF1, NF2, NF3	V_{IN} = V_{DD} (including output transistor off leakage current)	2.5 to 5.0	−	−	1	μA
Low Level Input Current	I_{IL}	ALARMB, SDA, SCL, NF1, NF2, NF3	V_{IN} = V_{SS} (including output transistor off leakage current)	2.5 to 5.0	−1	−	−	
Low Level Output Voltage	V_{OL} (1)	ALARMB, SDA, SCL	I_{OL} = 3.0 mA	3.3 to 5.0	−	−	0.4	V
	V_{OL} (2)		I_{OL} = 1.3 mA	2.5 to 5.0	−	−	0.4	
Hysteresis Voltage	VHYS	ALARMB, SDA, SCL		2.5 to 5.0	−	0.2	−	
Pull−up Resistor Resistance	Rpu	TSENSE		2.5 to 5.0	−	10	−	kΩ
Pull−up Resistor Temperature Coefficient	Rpuc	TSENSE	Ta = −20°C to +70°C	2.5 to 5.0	−0.05	−	+0.05	%/°C
POWER ON RESET								
Reset Release Voltage	V_{RR}	VDD			−	−	2.4	V
Initialization Time after Reset Release	T_{INIT}			2.4 to 5.0	−	−	90	ms
TIMER								
Time Measurement Accuracy	T_{ME}		Ta = 25°C	2.5 to 5.0	−1	−	+1	%
BATTERY VOLTAGE								
Voltage Measurement Accuracy	V_{ME} (1)	VDD	Ta = +25°C	4	−7.5	−	+7.5	mV/cell
	V_{ME} (2)		Ta = −20°C to +70°C	2.5 to 5.0	−20	−	+20	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. I²C SLAVE CHARACTERISTICS (T_A = −40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} (V)	Specification		Unit
					Min	Max	
Clock Frequency	T_{SCL}	SCL		2.5 to 5.0	–	400	kHz
Bus Free Time between STOP Condition and START Condition	T_{BUF}	SCL, SDA	(See Figure 5)		1.3	–	μs
Hold Time (Repeated) START Condition. First Clock Pulse is Generated after this Interval	$T_{HD:STA}$	SCL, SDA	(See Figure 5)		0.6	–	μs
Repeated START Condition Setup Time	$T_{SU:STA}$	SCL, SDA	(See Figure 5)		0.6	–	μs
STOP Condition Setup Time	$T_{SU:STO}$	SCL, SDA	(See Figure 5)		0.6	–	μs
Data Hold Time	$T_{HD:DAT}$	SCL, SDA	(See Figure 5)		0	–	μs
Data Setup Time	$T_{SU:DAT}$	SCL, SDA	(See Figure 5)		100	–	ns
Clock Low Period	T_{LOW}	SCL	(See Figure 5)		1.3	–	μs
Clock High Period	T_{HIGH}	SCL	(See Figure 5)		0.6	–	μs
Time-out Interval (Notes 1, 2)	T_{TMO}	SCL, SDA	(See Figure 6)		12	14	s

1. This LSI resets I²C communication if the communication takes more than T_{TMO}. It initializes an internal timer to measure the interval when it detects ninth clock pulse. It can receive a new START condition after the reset.
2. This LSI may lose I²C communication at this reset operation. Then if a master can't receive a response it must restart transaction from START condition.

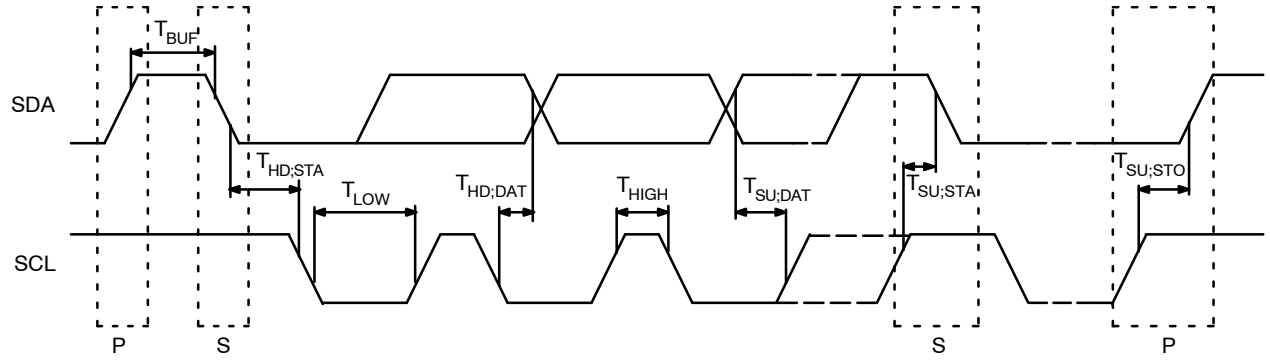


Figure 5. I²C Timing Diagram

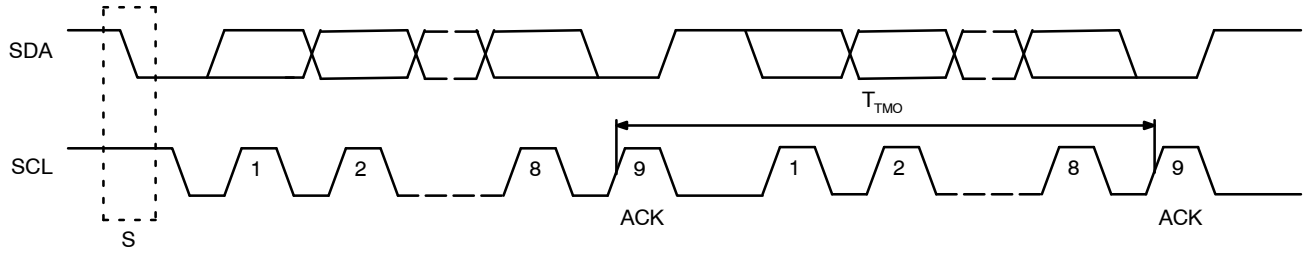


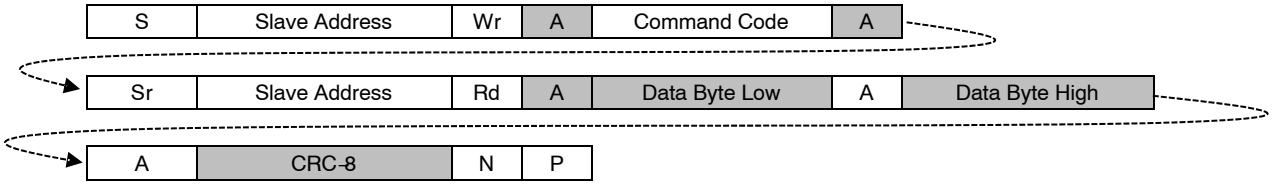
Figure 6. I²C Time-out Interval

I²C COMMUNICATION PROTOCOL

Communication protocol type: I²C
Frequency: Supported up to 400 kHz
Slave Address: 0001011 (The first 8−bits after the Strat Condition is 0x16 (WRITE) or 0x17 (READ).)
The LSI will stretch the clock.

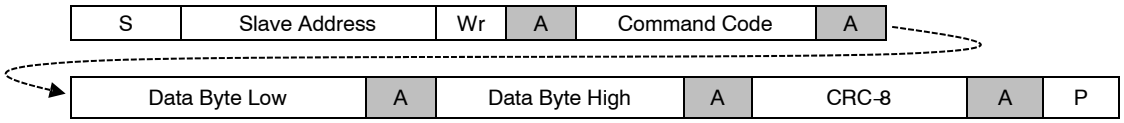
Bus Protocols

S	:	Start Condition
Sr	:	Repeated Start Condition
Rd	:	Read (bit value of 1)
Wr	:	Write (bit value of 0)
A	:	ACK (bit value of 0)
N	:	NACK (bit value of 1)
P	:	Stop Condition
CRC−8	:	Slave Address to Last Data (CRC−8−ATM : ex. 3778 mV : 0x16, 0x09, 0x17, 0xC2, 0x0E → 0x86)
	:	Master-to-Slave
	:	Slave-to-Master
...	:	Continuation of protocol



* When you do not read CRC−8, LSI data is not reliable. CRC−8−ATM ex: (5 bytes) 0x16, 0x09, 0x17, 0xC2, 0x0E → 0x86

Figure 7. Read Word Protocol



* When you do not add CRC−8, the Written data (Data byte Low/High) become invalid.
CRC−8−ATM ex: (4 bytes) 0x16, 0x09, 0x55, 0xAA → 0x3B

Figure 8. Write Word Protocol

Table 6. FUNCTION OF REGISTERS

Command Code	Register Name	R/W	Range	Unit	Description	Initial Value
BATTERY PROFILE−RELATED REGISTERS						
0x12	Change Of The Parameter	R/W	0x0000 to 0x0004		Select a battery profile.	0x0000
0x1A	Number of The Parameter	R	0x0000 to 0xFFFF		Displays Battery profile code.	−
0x0B	APA (Adjustment Pack Application)	R/W	0x0000 to 0xFFFF		Sets Adjustment parameter.	−

Table 6. FUNCTION OF REGISTERS (continued)

Command Code	Register Name	R/W	Range	Unit	Description	Initial Value
BATTERY PROFILE−RELATED REGISTERS						
0x1C	Termination current rate	R/W	0x0002 to 0x001E: Threshold (0.02C to 0.3C)	0.01C	Sets termination current rate.	0x0002
0x1D	Empty Cell Voltage	R/W	0x0000: Disable 0x09C4 to 0x1388: Threshold (2.5 V to 5 V)	mV	Sets empty cell voltage.	0x0000
0x1E	ITE Offset	R/W	0x0000 to 0x03E8 (0.0% to 100.0%)	0.1%	Sets ITE so that RSOC is 0%.	0x0000
THERMISTOR−RELATED REGISTERS						
0x16	Status Bit	R/W	0x0000: I²C mode 0x0001: Thermistor mode	Controls TSENSE thermistor.		0x0000
0x06	TSENSE Thermistor B	R/W	0x0000 to 0xFFFF	K	Sets B−constant of the TSENSE thermistor.	0x0D34 (3380 K)
0x0C	APT (Adjustment Pack Thermistor)	R/W	0x0000 to 0xFFFF	Sets a value to adjust temperature measurement delay timing.		0x001E
0x08	Cell Temperature (TSENSE)	R	0x0980 to 0x0DCC (−30°C to 80°C)	0.1 K (0.0°C = 0x0AAC)	Displays Cell Temperature.	0x0BA6 (25°C)
		W			Sets Cell Temperature in I²C mode.	
CONTROL REGISTERS						
0x15	IC Power Mode	R/W	0x0001: Operational mode 0x0002: Sleep mode	Select Power mode.		0x0002
0x0A	Current Direction	R/W	0x0000: Auto mode 0x0001: Charge mode 0xFFFF: Discharge mode	Select Auto/Charge/Discharge mode.		0x0000
0x04	Before RSOC	W	0xAA55: 1st sampling 0xAA56: 2nd sampling 0xAA57: 3rd sampling 0xAA58: 4th sampling	Optional Command, especially for obtaining the voltage with intentional timing after power on reset, see Figure 15.		–
0x07	Initial RSOC	W	0xAA55: Initialize RSOC	Initialize RSOC with current voltage when 0xAA55 is set.		–
REPORTING REGISTERS						
0x09	Cell Voltage	R	0x09C4 to 0x1388 (2.5 V to 5 V)	mV	Displays Cell Voltage.	–
0x0D	RSOC	R/W	0x0000 to 0x0064 (0% to 100%)	%	Displays RSOC value based on a 0 – 100 scale	–
0x0F	ITE (Indicator to Empty)	R	0x0000 to 0x03E8 (0.0% to 100.0%)	0.1%	Displays RSOC value based on a 0 – 1000 scale	–
ALARM THRESHOLD AND STATUS REGISTERS						
0x19	BatteryStatus	R/W	0x0000 to 0xFFFF	Displays various kinds of alarm and estimated state of the battery.		0x0080
0x14	Alarm Low Cell Voltage	R/W	0x0000: Disable 0x09C4 to 0x1388: Threshold (2.5 V to 5 V)	mV	Sets Voltage threshold to generate Low Cell Voltage Alarm signal.	0x0000
0x13	Alarm Low RSOC	R/W	0x0000: Disable 0x0001 to 0x0064: Threshold (1% to 100%)	%	Sets RSOC threshold to generate Alarm signal.	0x0000
OTHER REGISTERS						
0x11	IC Version	R	0x0000 to 0xFFFF	Displays an internal management code.		–
Except above commands	No function	–	–	Registers that the access is prohibited.		–

NOTE: 0xXXXX = Hexadecimal notation

Table 7. BATTERY PROFILE VS. REGISTER

IC Type	Battery Type	Nominal / Rated Voltage	Charging Voltage	Number of The Parameter (0x1A)	Change of The Parameter (0x12)
LC709204VXE−01TBG	01	3.7 V	4.2 V	0x1001	0x00
	04	UR18650ZY (Panasonic)			0x01
	05	ICR18650−26H (SAMSUNG)			0x02
	06	3.8 V	4.35 V		0x03
	07	3.85 V	4.4 V		0x04

BATTERY PROFILE−RELATED REGISTERS

Change of the Parameter (0x12)

The LSI contains five type battery profiles. This register can select a target battery profile from them. See Table 7. Nominal/rated voltage or charging voltage of the target battery support to determine which battery profile shall be used.

In addition to the selection this command initializes RSOC using the selected battery profile and the 1st sampled voltage during initial sequence. Refer to Before RSOC (0x04) section about the voltage.

Number of the Parameter (0x1A)

This register contains identity of installed battery profiles.

Adjustment Pack Application (0x0B)

This register contains APA values which are parameter to fit installed battery profiles in a target battery characteristics. Appropriate APA values for the target battery will improve RSOC accuracy.

Typical APA values can be taken from the design capacity of the battery in Table 8. Table 8 shows relations of typical APA value and the design capacity. Use capacity per 1−cell for the table if some batteries are connected in parallel. Calculate APA values using linear supplement if there is not a requested design capacity in the table. See following formula.

$$\text{APAvalue} = \text{Lower\_APA} + (\text{Upper\_APA} - \text{Lower\_APA}) \times \frac{\text{Capacity} - \text{Lower\_Cap.}}{\text{Upper\_Cap.} - \text{Lower\_Cap.}} \quad \text{(eq. 1)}$$

Calculation example in case 1500 mAh battery Type−01.

$$\text{APAvalue} = 45{:}0x2D + (58{:}0x3A - 45{:}0x2D) \times \frac{1500 - 1000}{2000 - 1000} = 52{:}0x34$$

The upper 8−bits and the lower 8−bits of APA register are for charging and discharging adjustment parameters each. See Table 9. Table 8 shows them as the same value. For example the set value in APA register is 0x0D0D for 0x0D APA value.

But RSOC accuracy may be improved by setting different values each depending on the target battery characteristics.

Please contact **onsemi** if you don't satisfy the RSOC accuracy. The deeper adjustment of APA value may improve the accuracy.

Table 8. TYPICAL APA VALUE FOR CHARGING AND DISCHARGING ADJUSTMENT

Design Capacity	APA[15:8],APA[7:0]		
	Type−01	Type−06	Type−07
50 mAh	0x13, 0x13	0x0C, 0x0C	0x03, 0x03
100 mAh	0x15, 0x15	0x0E, 0x0E	0x05, 0x05
200 mAh	0x18, 0x18	0x11, 0x11	0x07, 0x07
500 mAh	0x21, 0x21	0x17, 0x17	0x0D, 0x0D
1000 mAh	0x2D, 0x2D	0x1E, 0x1E	0x13, 0x13
2000 mAh	0x3A, 0x3A	0x28, 0x28	0x19, 0x19
3000 mAh	0x3F, 0x3F	0x30, 0x30	0x1C, 0x1C
4000 mAh	0x42, 0x42	0x34, 0x34	−
5000 mAh	0x44, 0x44	0x36, 0x36	−
6000 mAh	0x45, 0x45	0x37, 0x37	−

Design Capacity	APA[15:8], APA[7:0]	
	Type−04	Type−05
2600 mAh	0x10, 0x10	0x06, 0x06

Table 9. BIT CONFIGURATION OF APA REGISTER

BITS	Register Name
APA[15:8]	APA value for charging adjustment
APA[7:0]	APA value for discharging adjustment

Termination Current Rate (0x1C)

Set the termination current rate in charging when RSOC (0x0D) arrives at 100% in 0.01C. (i.e. the set value is 0x02 for 3000 mAh design capacity and 60mA termination current.) The installed battery profiles are designed so that ITE (0x0F) arrives at 0x3E8 when the battery current rate in charging decreases to 0.02C. Therefore ITE (0x0F) and RSOC (0x0D) will arrive at the maximum value at the same time when this value is 0x02 (0.02C). The arrival of RSOC to the maximum value becomes early when this value exceeds 0x02. This register produces an offset between ITE and RSOC on full charge side. See Figure 9. This offset value is calculated according to battery profile and this register value.

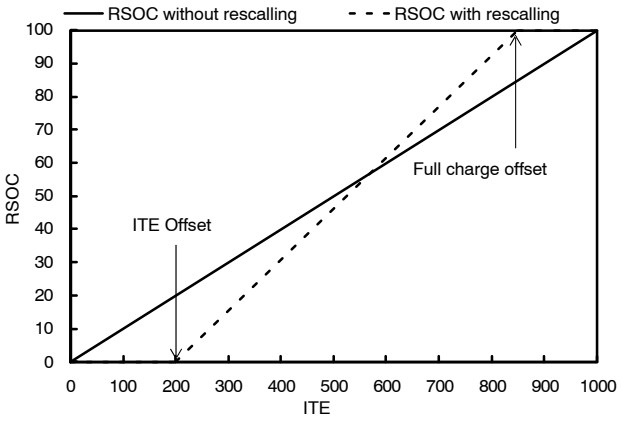


Figure 9. Rescaled RSOC by ITE Offset and Termination Current Rate

Empty Cell Voltage (0x1D)

Set the minimum battery voltage when RSOC is 0% in mV. When the LSI detects that Cell Voltage (0x09) is lower than Empty Cell Voltage (0x1D) it will set the ITE (0x0F) value of the moment to ITE Offset (0x1E) automatically. See Figure 10. RSOC (0x0D) is rescaled so that it is 0% when ITE (0x0F) is equal to ITE Offset (0x1E). Following formulas indicate the update conditions of ITE Offset (0x1E).

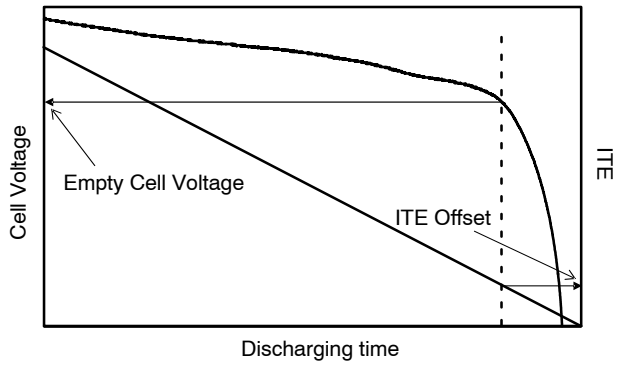


Figure 10. Empty Cell Voltage and ITE Offset in Discharging

$$\text{Cell Voltage (0x09)} < \text{Empty Cell Voltage (0x1D)} \quad \text{(eq. 2)}$$

$$\text{ITE (0x0F)} > \text{ITE Offset (0x1E)} \quad \text{(eq. 3)}$$

$$\text{Cell Temperature (0x08)} > \text{0x0AAC (0°C)} \quad \text{(eq. 4)}$$

Set this register to 0 not to update ITE Offset (0x1E) automatically.

ITE Offset (0x1E)

This register is referred to transform ITE (0x0F) to RSOC (0x0D). RSOC will be rescaled so that it is 0% when ITE (0x0F) is equal to this register. See Figure 9. There are two methods to update this register. One is to write it directly. The other is an automatic update by Empty Cell Voltage (0x1D). Refer to Empty Cell Voltage section about it.

THERMISTOR−RELATED REGISTERS

Status Bit (0x16)

This register controls temperature measurement with external thermistors as shown in Table 10.

Table 10. STATUS BIT

Status BIT	Mode	Description
0	I^2C mode	The LSI receives temperature information via I^2C.
1	Thermistor mode	The LSI measures temperature with the attached thermistor and loads the temperature into the Cell Temperature register.

TSENSE Thermistor B (0x06)

Sets B−constant of the thermistor which is connected to TSENSE. Refer to the specification sheet of the thermistor for the set value.

Adjustment Pack Thermistor (0x0C)

The LSI will power external NTC thermistors periodically to measure CELL and AMBIENT temperature. Internal pull−up resistor of TSENSE turns on for the charging. This register contains the delay time from the turn−on to the temperature measurement. The delay time is calculated by following formula.

$$\text{Delay} = 0.167\ \mu s \times (200 + \text{APT}) \quad \text{(eq. 5)}$$

See Figure 11 about the delay and waveform. The default APT (0x001E) will meet most of circuits where a capacitor as shown in Figure 12 is not placed. This will delay the measurement with this register if there is a capacitor in target battery pack.

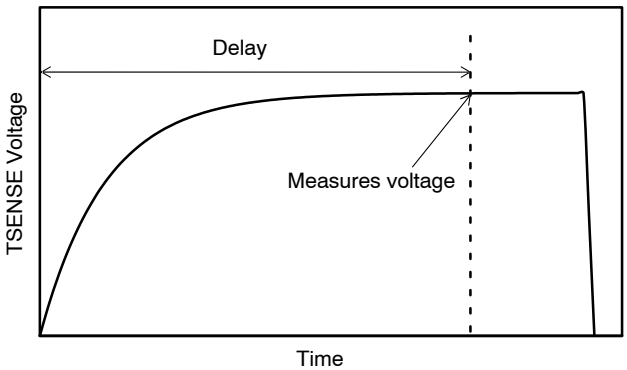


Figure 11. Example of TSENSE Voltage at Temperature Measurement

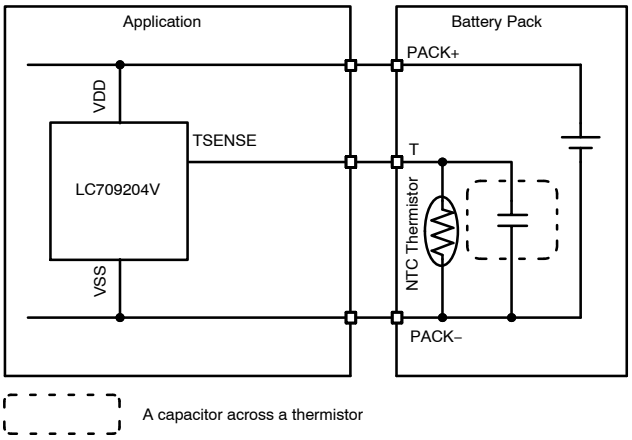


Figure 12. An Example of a Capacitor Across the Thermistor

Cell Temperature (TSENSE) (0x08)

This register contains the cell temperature from −30°C (0×0980) to +80°C (0×0DCC) measured in 0.1°C units. When Bit 0 of Status Bit (0x16) is 1 the LSI measures the attached thermistor and loads the temperature into this register. For this mode, the thermistor shall be connected to the LSI as shown in Figure 1. TSENSE pin provides power to the thermistor and senses it. Temperature measurement timing is controlled by the LSI, and the power to the thermistor is supplied only at the time.

The Cell Temperature is used for battery measurement that includes RSOC. Then when Bit 0 of Status Bit (0x16) is 0 the application processor must input temperature of the battery to this register. Update of Cell temperature is recommended if the temperature changes more than 1°C during battery charging and discharging.

CONTROL REGISTERS

IC Power Mode (0x15)

The LSI has two power modes. Operational mode (0x15 = 01) or Sleep mode (0x15 = 02). In the Operational mode all functions operate with full calculation and tracking of RSOC during charge and discharge. In the Sleep mode only I^2C communication function is enable and ALARMB pin is released from low. When it is switched from Sleep mode to Operational mode RSOC calculation is continued by using the data which was measured in the previous Operational mode.

Current Direction (0x0A)

This register is used to control the reporting of RSOC. In Auto mode the RSOC is reported as it increases or decreases. In Charge mode the RSOC is not permitted to decrease. In Discharge mode the RSOC is not permitted to increase.

With consideration of capacity influence by temperature, we recommend operating in Auto because RSOC is affected by the cell temperature. A warm cell has more capacity than a cold cell. Be sure not to charge in the Discharge mode and discharge in the Charge mode; it will create an error.

An example of RSOC reporting is shown in Figures 13 and 14.

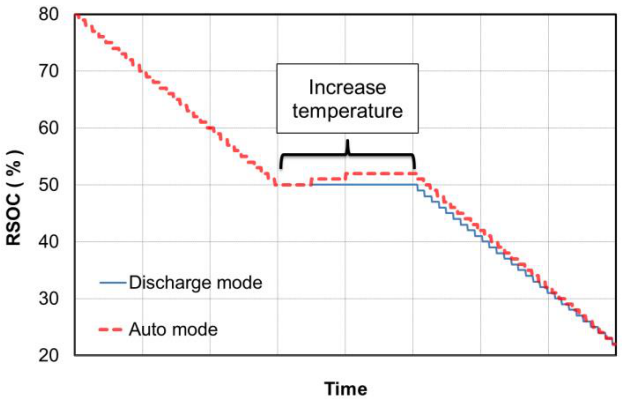


Figure 13. Discharge Mode (An Example with Increasing in Temperature. A Warm Cell has More Capacity than a Cold Cell. Therefore RSOC Increases without Charging in Auto Mode.)

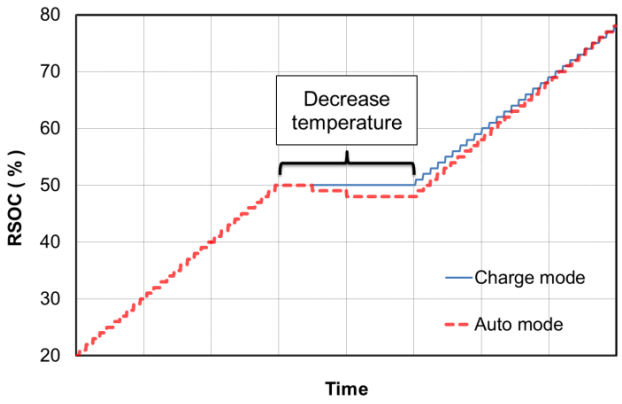


Figure 14. Charge Mode (An Example with Decreasing in Temperature. A Cold Cell has Less Capacity than a Warm Cell. Therefore RSOC Decreases without Discharging in Auto Mode.)

Before RSOC (0x04)

This command is the optional Command, used especially for obtaining the voltage with intentional timing after power on reset. Generally the LSI will get initial RSOC by Open Circuit Voltage (OCV) of a battery. It is desirable for battery current to be less than 0.025C to get expected OCV. (i.e. less than 75 mA for 3000 mAh design capacity battery.) The LSI initializes RSOC by measured battery voltage in initial sequence. But if reported RSOC after reset release is not expected value, “Before RSOC” command or “Initial RSOC” command can initialize RSOC again.

The LSI samples battery voltage four times during initial sequence. The sampling interval is around 10 ms. See Figure 15. RSOC is initialized using the 1st sampled voltage automatically with the initial sequence. The four sampled voltage are maintained until the LSI is reset. “Before RSOC” command can select a voltage for RSOC initialization from

them. See Table 11. If the battery is not charged during initial sequence the maximum voltage is suitable for more accurate initial RSOC. Try all "Before RSOC" command and read RSOC (0x0D) to search the maximum voltage. The higher RSOC after the command is caused by the higher voltage.

Table 11. BEFORE RSOC COMMAMD

Command Code	DATA	Sampling Order of Battery Voltage for RSOC Initialization
0x04	0xAA55	1st sampling
	0xAA56	2nd sampling
	0xAA57	3rd sampling
	0xAA58	4th sampling

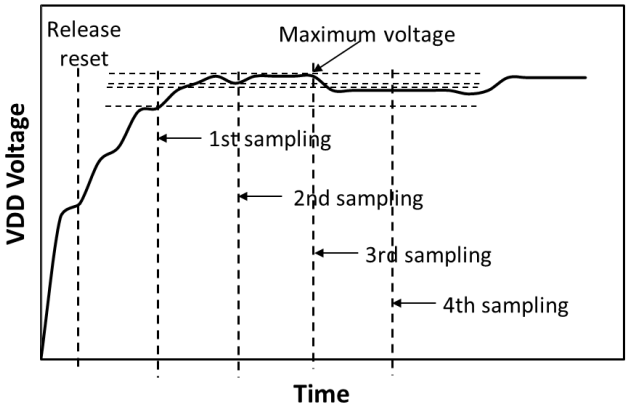


Figure 15. Sampling Order for before RSOC Command

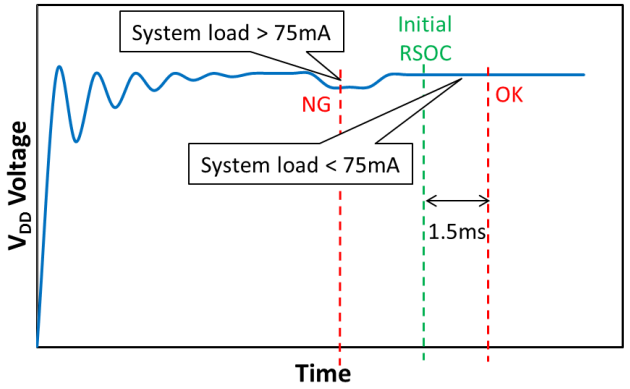


Figure 16. Initial RSOC Command

Initial RSOC (0x07)

The LSI can be forced to initialize RSOC by sending the Before RSOC Command (0×04 = AA55) or the Initial RSOC Command (0×07 = AA55).

The LSI initializes RSOC by the measured voltage at that time when the Initial RSOC command is written. (See Figure 16). The maximum time to initialize RSOC after the command is written is 1.5 ms.

REPORTING REGISTERS

Cell Voltage (0x09)

This register contains the V_{DD} voltage in mV.

RSOC (0x0D)

This register contains RSOC in 1%. When this register is written in Operational mode the data may be updated by automatic convergence function of the LSI. About the function, refer to "Automatic Convergence of the Error" section. Writing to this register is not necessary in normal operation. ITE (0x0F) will be updated with the writing too.

Indicator to Empty (0x0F)

This register contains RSOC in 0.1%.

ALARM THRESHOLD AND STATUS REGISTERS

BatteryStatus (0x19)

This register contains alarm condition. See Table 12. Each alarm bit is set to 1 when each alarm condition is satisfied. The bits which are set to 1 once will keep 1 even if the alarm conditions are resolved. Set the alarm bits to 0 after having confirmed the cause of the alarm.

Status bit 7 that is INITIALIZED helps that an application processor detects the power−on reset of the LSI by battery insertion. The bit is set to 1 after power−on reset. Then the processor can detect the power−on reset if it has set the bit to 0 after previous power−on reset.

Table 12. BatteryStatus

	BIT	Function	ALARMB Control	Initial Value
ALARM	15	Reserved	–	0
	14	Reserved	–	0
	13	Reserved	–	0
	12	Reserved	–	0
	11	Low Cell Voltage	↗	0
	10	Reserved	–	0
	9	Low RSOC	↗	0
	8	Reserved	–	0
STATUS	7	INITIALIZED	–	1
	6	Reserved	–	0
	5	Reserved	–	0
	4	Reserved	–	0
	3	Reserved	–	0
	2	Reserved	–	0
	1	Reserved	–	0
	0	Reserved	–	0

Alarm Low RSOC (0x13)

The ALARMB pin will output low level and the bit 9 of BatteryStatus register (0x19) will be set to 1 when RSOC (0x0D) falls below this value. ALARMB pin will be released from low when RSOC value rises than this value. But the bit 9 keeps 1 until it is written or Power−on reset. Set this register to 0 to disable. Figure 17.

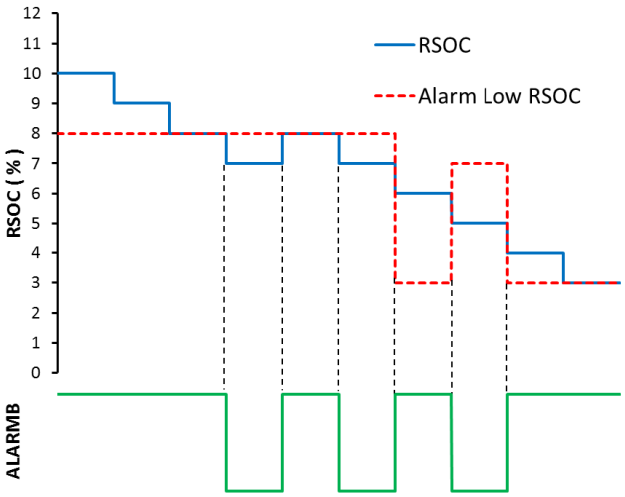


Figure 17. Alarm Low RSOC

Alarm Low Cell Voltage (0x14)

The ALARMB pin will output low level and the bit 11 of BatteryStatus register (0x19) will be set to 1 if Cell Voltage (0x09) falls below this value. ALARMB pin will be released from low if VDD rises than this value. But the bit 11 keeps 1 until it is written or Power−on reset. Set this register to 0 to disable. Figure 18.

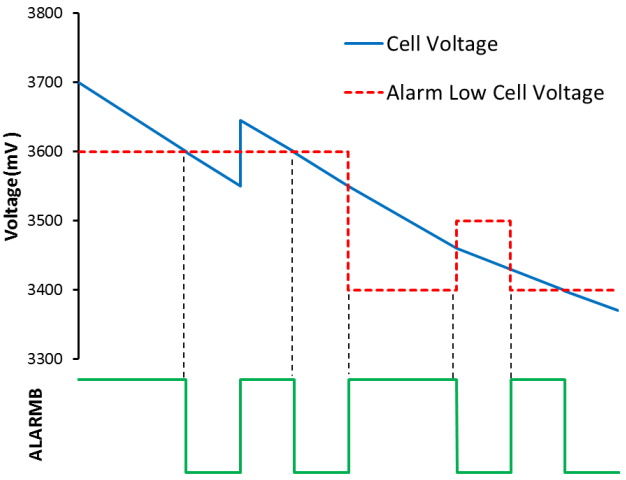


Figure 18. Alarm Low Cell Voltage

OTHER REGISTERS

IC Version (0x11)

This register contains an internal management code. The value is not published.

HG−CVR2

Hybrid Gauging by Current−Voltage Tracking with Internal Resistance

HG−CVR2 is **onsemi**'s unique method which is used to calculate accurate RSOC. **HG−CVR2** first measures battery voltage and temperature. Precise reference voltage is essential for accurate voltage measurement. LC709204V has accurate internal reference voltage circuit with little temperature dependency.

It also uses the measured battery voltage and internal impedance and Open Circuit Voltage (OCV) of a battery for the current measurement. OCV is battery voltage without load current. The measured battery voltage is separated into OCV and varied voltage by load current. The varied voltage is the product of load current and internal impedance. Then the current is determined by the following formulas.

$$V\,(VARIED) = V\,(MEASURED) - OCV \qquad \text{(eq. 6.)}$$

$$I = \frac{V\,(VARIED)}{R\,(INTERNAL)} \qquad \text{(eq. 7.)}$$

Where *V (VARIED) i*s varied voltage by load current, *V (MEASURED)* is measured voltage, *R (INTERNAL)* is internal impedance of a battery. Detailed information about the internal impedance and OCV is installed in the LSI. The internal impedance is affected by remaining capacity, load−current, temperature, and more. Then the LSI has the information as look up table. **HG−CVR2** accumulates battery coulomb using the information of the current and a steady period by a high accuracy internal timer. The remaining capacity of a battery is calculated with the accumulated coulomb.

How to Identify Aging

By repeating discharge/charge, internal impedance of a battery will gradually increase, and the Full Charge Capacity (FCC) will decrease. In coulomb counting method RSOC is generally calculated using the FCC and the Remaining Capacity (RM).

$$RSOC = \frac{RM}{FCC} \times 100\% \qquad \text{(eq. 8.)}$$

Then the decreased FCC must be preliminarily measured with learning cycle. But **HG−CVR2** can measure the RSOC of deteriorated battery without learning cycle. The internal battery impedance that **HG−CVR2** uses to calculate the current correlates highly with FCC. The correlation is based on battery chemistry. The RSOC that the LSI reports using the correlation is not affected by aging.

Automatic Convergence of the Error

A problem of coulomb counting method is the fact that the error is accumulated over time − This error must be corrected. The general gauges using coulomb counting method must find an opportunity to correct it.

The LSI with **HG−CVR2** has the feature that the error of RSOC converges autonomously, and doesn't require

calibration opportunities. The error constantly converges in the value estimated from the Open Circuit Voltage. Figure 19 shows the convergent characteristic example from the initialize error.

Also, coulomb counting method cannot detect accurate residual change because the amount of the current from self−discharge is too small but **HG−CVR2** is capable to deal with such detection by using the voltage information.

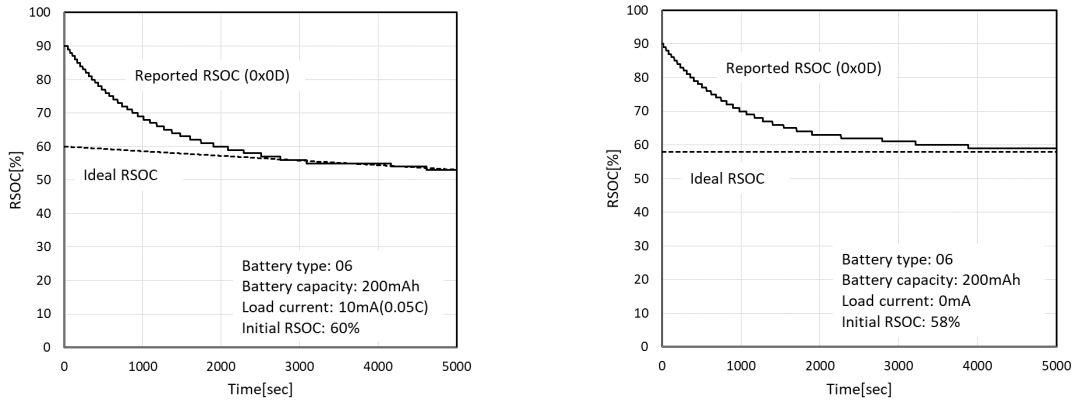
Simple and Quick Setup

In general, it is necessary to obtain multiple parameters for a fuel gauge and it takes a lot of resource and additional development time of the users. One of the unique features of LC709204V is very small number of parameters to be prepared. Such simple and quick start−up is realized by having multiple profile data in the LSI to support various types of batteries. Please contact your local sales office to learn more information on how to measure a battery that cannot use already−prepared profile data.

Low Power Consumption

Low power consumption of 2 μA is realized in the Operation mode. The LSI monitors charge/discharge condition of a battery and changes the sampling rate according to its change of current. Power consumption reduction without deteriorating its RSOC accuracy was enabled by utilizing this method.

TYPICAL CHARACTERISTICS



NOTE: This Graph is the example for starting point 90% (includes 30 − 32% error).

Figure 19. Convergent Characteristic from the Initialize Error

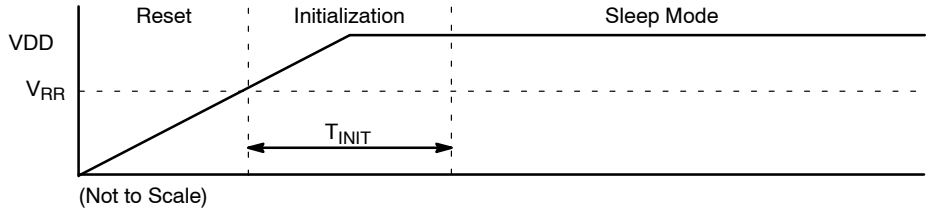


Figure 20. Power On Timing Diagram

Power−on Reset / Battery Insertion Detection

When the LSI detects battery insertion, it is reset automatically. Once the battery voltage exceeds over the V_{RR}, it will release RESET status and will complete LSI initialization within T_{INIT} to enter into Sleep mode. Then I^2C communication can be started. Figure 20. All registers are initialized after the sequence.

Measurement Starting Flow

After the initialization users can start battery measurement by writing appropriate value into the registers by following the flow shown in Figure 21 − 22. Figure 21 shows Thermistor mode that the LSI measures battery temperature with thermistors. Figure 22 shows I^2C mode that the LSI receives battery temperature from an application processor. In the figure Mandatory settings to measure RSOC are enclosed in sold line. Optional settings to use each required function are enclosed in dotted line.

Set some mandatory or optional parameters at the beginning. RSOC (0x0D) is updated to the value corresponding to a selected battery profile after Change of the Parameter command (0x12). Then set the LSI to Operational mode. At the end of starting flow set INITIALIZED bit to 0. An application processor can detect whether the LSI was reinitialized by reading the bit. (For example, for turn−off by Lib−protection IC) Repeat this starting flow again if this bit is changed to 1.

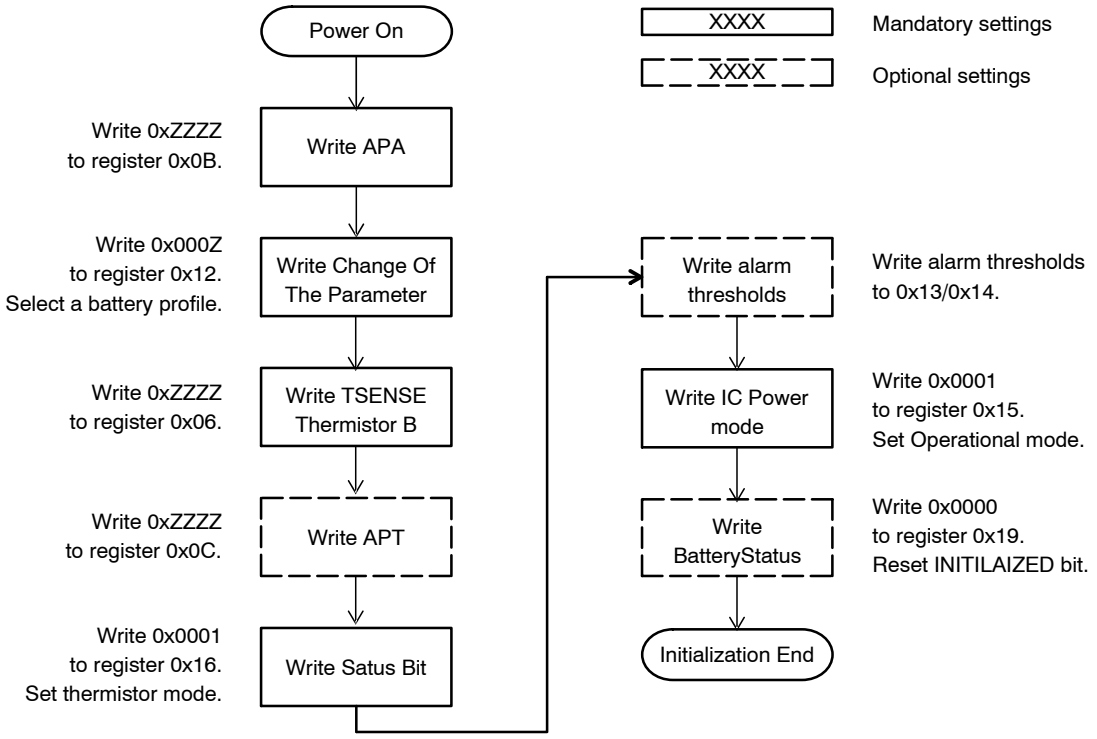


Figure 21. Starting Flow at Thermistor Mode

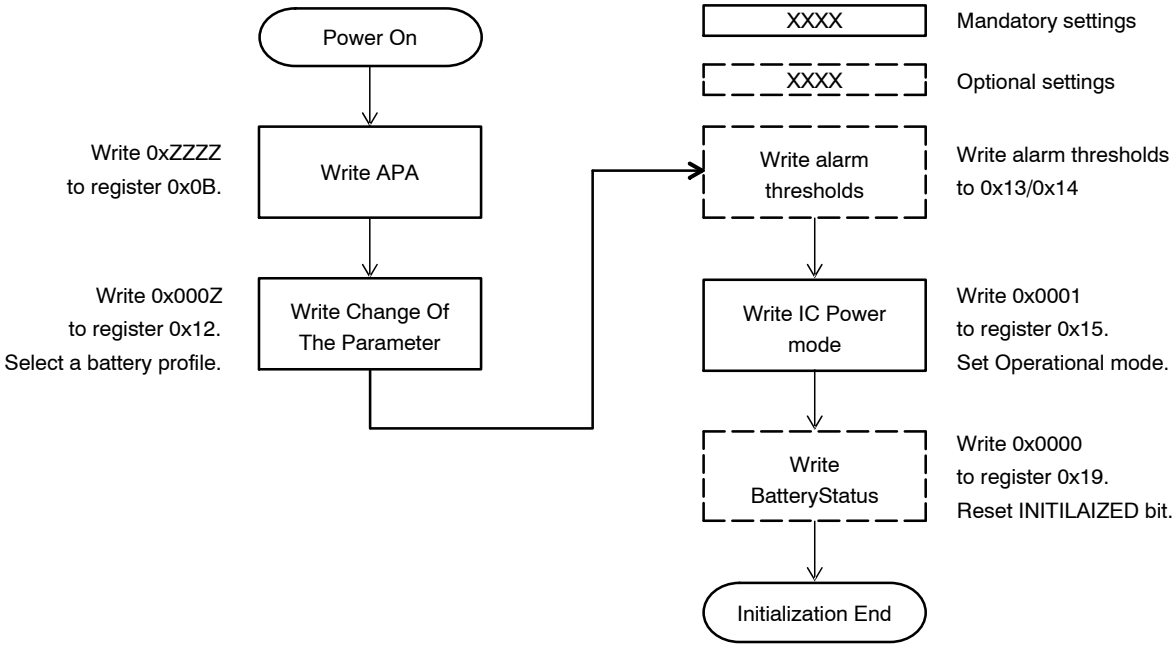


Figure 22. Starting Flow at I²C Mode

Layout guide

Figure 23 shows the recommended layout pattern around LC709204V. Place CVDD and CREG capacitor near the LSI.

Figure 24 shows the position to place the LSI on the Power paths. The resistance of the Power paths between Battery or Battery Pack and the LSI affects the gauging. Place the LSI to minimize the resistance. But the resistance of the paths which is connected to only the LSI doesn't affect it.

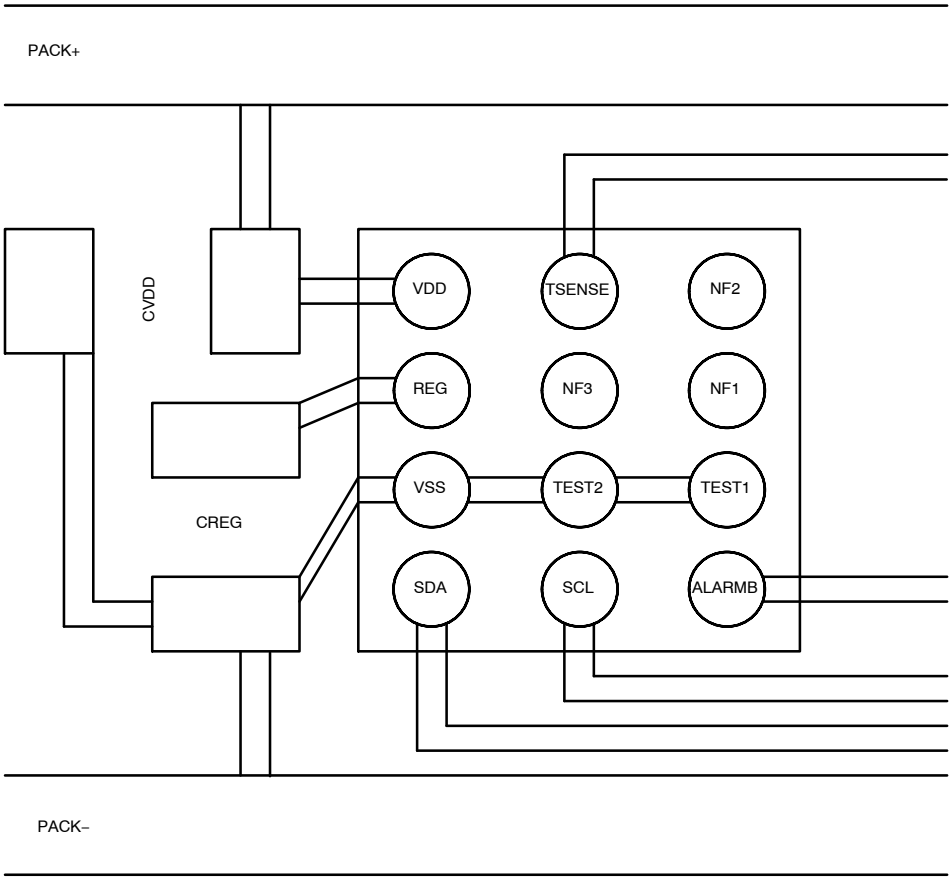


Figure 23. Layout Pattern Example Around LC709204V (Top View)

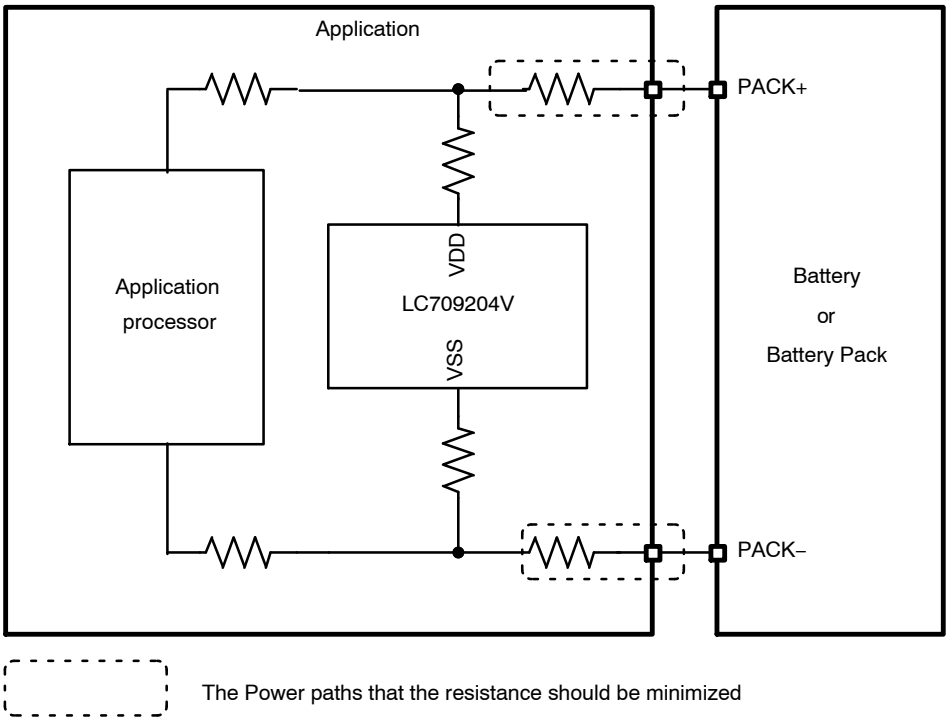


Figure 24. Position to Connect LC709204V on Power Supply Lines

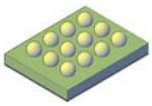
Table 13. ORDERING INFORMATION

Device	Package	Shipping†
LC709204VXE−01TBG	WLCSP12, 1.48x1.91x0.51 (Pb-Free / Halogen Free)	5,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

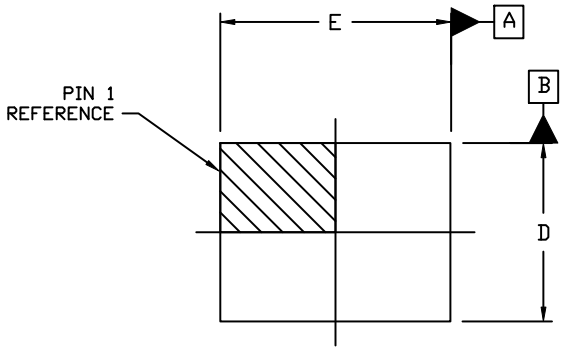
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

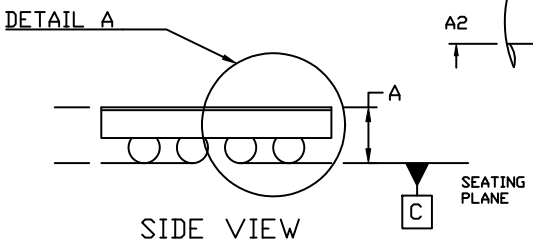


WLCSP12, 1.48x1.91x0.51
CASE 567XE
ISSUE A

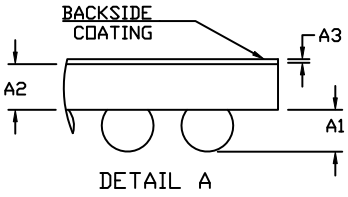
DATE 22 FEB 2019



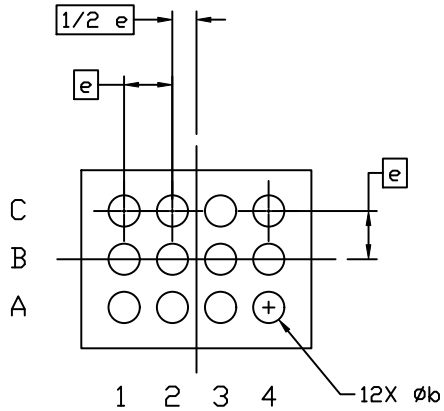
TOP VIEW



SIDE VIEW



DETAIL A

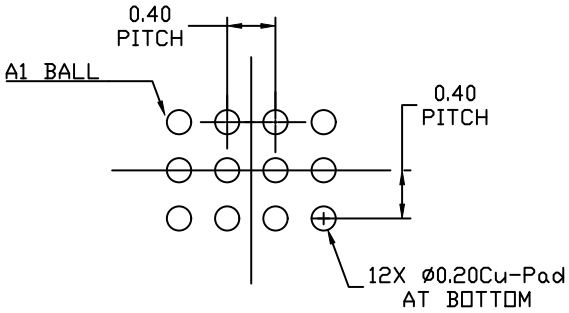


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPERICAL CROWNS OF THE CONTACT BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE CONTACT BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

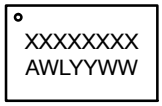
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	0.510
A1	0.18	0.21	0.24
A2	0.245 REF		
A3	0.025 REF		
b	0.21	0.26	0.31
D	1.43	1.48	1.53
E	1.86	1.91	1.96
e	0.40 BSC		



RECOMMENDED
MOUNTING FOOTPRINT*
(NSMD PAD TYPE)

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON99809G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	WLCSP12, 1.48x1.91x0.51	PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales