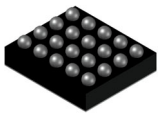
Surge and Over-Voltage Protection Switch for VBUS

FPF2188LUCX



WLCSP20
CASE 567US

Description

The FPF2188L features a surge and over voltage protection switch for power path in USB type C/PD applications. The FPF2188L has Single Input Single Output (SISO) power path. Power path (V_{BUS} to V_{OUT}) is an active−low, 28 V / 6 A rated, power MOSFET switch with an internal clamp supporting surge protection, selectable OVP by GPIO.

BUS_DET is paired with always ON LDO to power downstream devices when VBUS is greater than 3.1 V, regardless of OVLO and ENB State. This provides system power supply without battery. The FPF2188L features OTG_DET pin to supply the device when OTG device is inserted. It will support to turn on the power MOSFET even when VBUS voltage is low.

The FPF2188L has active discharge path at VBUS which can meet USB type C w/ PD compliance. The FPF2188L is available in a 20−bump, Wafer−Level Chip−Scale Package (WL−CSP) with 0.4 mm pitch.

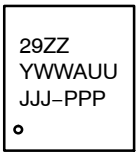
Features

- SISO (Single Input Single Output) Surge and Over−Voltage Protection Switch
- 200 V Surge Protection at VBUS under IEC 61000−4−5
- Hot Plug Max = 28 V
- VBUS Voltage Range: 2.7 V ~ 21.0 V
- Max Continuous Current Capability: 6 A
- Low ON−Resistance: Typical 9 mΩ at 5 V / 25°C
- Selectable OVP Trip Level by GPIO
- Ultra−fast OV Response Time: Typ 50 ns
- Always ON LDO Output, BUS_DET
- OTG_DET for OTG Start−up Power Supply
- Active Discharge Path at VBUS
- Open Drain OVP FLAGB
- Over−Temperature Protection (OTP)

Applications

- Mobile Handsets and Tablets

MARKING DIAGRAM



29 = Specific Device Code
ZZ = Assembly Lot Code
YWW = Year / Work Week
A = Assembly Location
UU = Wafer Number
JJJ−PPP = X/Y Coordinates

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

Application Diagram

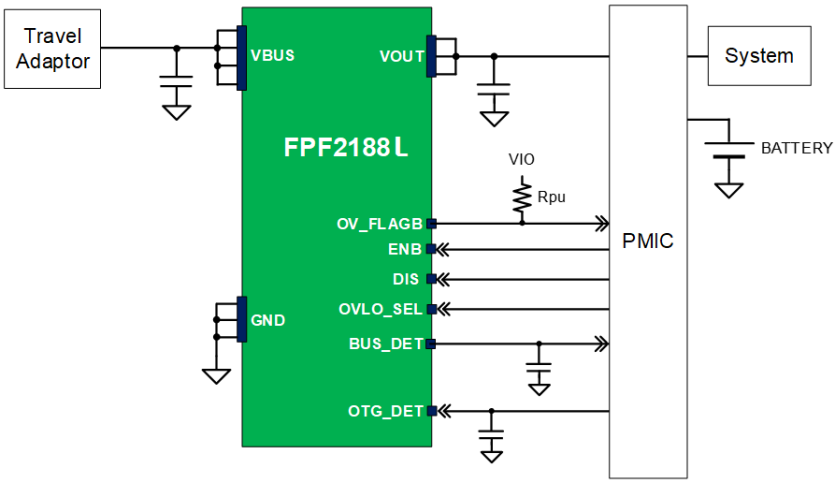


Figure 1. Typical Application

Block Diagram

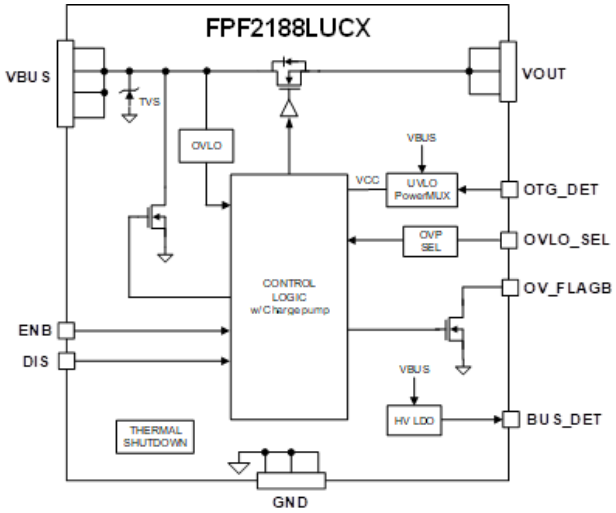


Figure 2. Functional Block Diagram

Pin Configuration

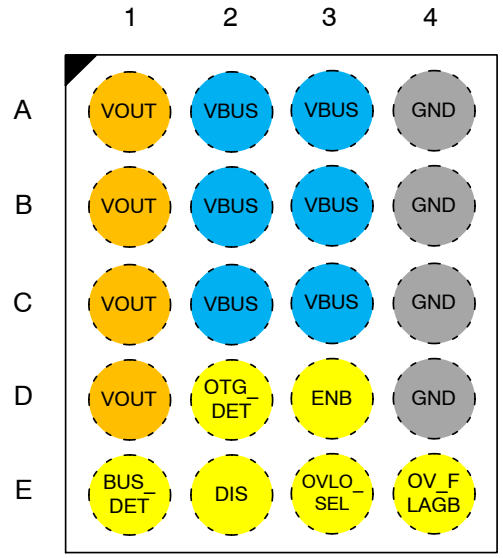


Figure 3. Pin Configuration (Top View)

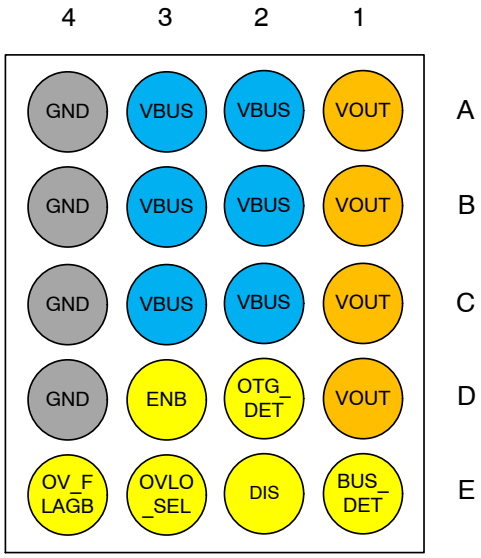


Figure 4. Pin Configuration (Bottom View)

PIN FUNCTION DESCRIPTION

Pin #	Pin Name	Type	Description
VBUS	A2,A3,B2,B3, C2,C3	Input/Supply	Switch Input/Output and Power Paths Block Power Supply
VOUT	A1,B1,C1,D1	Output/Supply	Switch Output/Input to Load
OTG_DET	D2	AI	Power supply for charge pump circuit during startup in OTG mode
BUS_DET	E1	Output	Regulated output according to VBUS
ENB	D3	Input	Active LOW for Power Path. Internal pull−down resistor of 1 MΩ is included.
DIS	E2	Input	Active HIGH for discharge path at VBUS node. Internal pull−down resistor of 1 MΩ is included.
OVLO_SEL	E3	Input	Over−Voltage Lockout Selection for VOUT path. Internal pull−down resistor of 1 MΩ is included. When OVLO_SEL = LOW then 12.4 V (typ.) (Default)/ 13.7 V (typ.) (OTP Option) When OVLO_SEL = HIGH then OVLO is set typ 21.9 V.
OV_FLAGB	E4	Output	Open drain output for OV state. External pull−up resistor with bias voltage are required. If not used, leaves the pin floating.
GND	A4,B4,C4,D4	GND	Ground

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
VBUS	VBUS to GND & VBUS to VOUT = GND or Float		−0.3	28	V
VOUT	VOUT to GND		−0.3	28	V
BUS_DET	BUS_DET to GND		−0.3	6	V
VENB_OTG_-DET_DIS_OV_FLAGB	ENB, OTG_DET, DIS, OVLO_SEL or OV_FLAGB to GND		−0.3	6	V
IIN_VBUS_VO-UT	Continuous VBUS to VOUT Current			6	A
	Peak VBUS to VOUT Current (5ms)			12	A
IIN_BUS_DET	Continuous BUS_DET Current		10		mA
tPD	Total Power Dissipation at T_A = 25°C			1.66	W
ΔPD/ΔT	Derating factor of PD over temperature			−16	mW/°C
TSTG	Storage Junction Temperature		−65	+150	°C
TJ	Operating Junction Temperature			+150	°C
TL	Lead Temperature (Soldering, 10 Seconds)			+260	°C
TJA	Thermal Resistance, Junction−to−Ambient (1in.^{2} pad of 2 oz. copper)			63.3 (Note1)	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, ANSI/ESDA/JEDEC JS−001	±2		kV
		Charged Device Model, JESD22−C101	±1		
	IEC61000−4−2 System Level	Air Discharge at VBUS	±15		
		Contact Discharge at VBUS	±8		
Surge	IEC61000−4−5	VBUS	−200	+200	V
Hot plug	IVBUS = 5 A; Vbus rising up from 0 V with slew rate > 6 V/μS			28	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured using 2S2P JEDEC std. PCB.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
VBUS	VBUS Operating Voltage	2.7	21.0	V
VOTG_DET	OTG_DET Operating Voltage	3.1	4.85	V
VOUT_OTG	VOUT Operating Voltage in OTG operation	5.0	5.4	V
CIN (Note 2)	Input Capacitance for VBUS. Minimum rating 50 V. (Note 3)	1		μF
COUT (Note 2)	Output Capacitance for VOUT. Minimum rating 25 V. (Note 3)	1		μF
COTG_DET (Note 2)	Capacitance for OTG_DET. Minimum rating 10 V. (Note 3)	1		μF
CBUS_DET (Note 2)	Capacitance for BUS_DET. Minimum rating 10 V. (Note 3)	1		μF
TA	Ambient Operating Temperature, TA	−40	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Bypass capacitor should be placed to the device as close as possible in order to reduce the parasitic inductance.
3. Each capacitor's DC rating is depending on Samsung's internal guidance.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, VBUS = 2.7 to 21.0 V, TA = −40 to 85°C; Typical values are at VBUS = 5 V, IIN ≤ 12 A, ENB=DIS=LOW, OVLO_SEL=GND, BUS_DET=Floating, CIN = 1 μF and TA = 25°C.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
BASIC OPERATION						
IQ_PWR	Power Input Quiescent Current enable	VBUS = 5 V, ENB = LOW			140	μA
	Power Input Quiescent Current disable	VBUS = 5 V, ENB = HIGH			140	
IIN_OVLO	OVLO Supply Current	VBUS = 15 V, VOUT = 0 V, ENB=LOW, OVLO_SEL = GND			160	μA
		VBUS = 23 V, VOUT = 0 V, ENB=LOW, OVLO_SEL = HIGH			180	
VUVLO	Under−Voltage Trip Level	VBUS Rising, TA= −40 to 85 °C	2.35	2.5	2.65	V
		VBUS Falling, TA= −40 to 85 °C	2.2	2.35	2.5	V
RPD	VBUS Discharge Resistance	VBUS = 5 V, DIS = 1.8 V		550		Ω
tDIS_ON	VBUS Discharge ON Delay Time	VOUT = 5 V. Time from DIS = HIGH to Discharge path ON		0.5	3	μs
tDIS_OFF	VBUS Discharge OFF Delay Time	VOUT = 5 V. Time from DIS = LOW to Discharge path OFF		1	3	μs
t_{DIS}	VBUS Discharge Time	VOUT = 5 V, CBUS = 1 μF, COUT=1Uf DIS = ENB = LOW → HIGH and VOUT source is removed at the same time, Time from VBUS = 5 V to 0.5 V		1.5	5	ms
T_{SDN}	Thermal Shutdown (Note 4)			145		°C
T_{SDN_HYS}	Thermal Shutdown Hysteresis (Note 4)			20		°C
INTEGRATED BI−DIRECTIONAL TVS						
VRW_P	Positive Reverse Working Voltage				28	V
VBR_P	Positive Breakdown Voltage	IIN = 1 mA	30	32	34	V
VCL_P	Positive Clamping Voltage (Note 4)	+200 V Surge (IEC61000−4−5 TA = −40°C to 85°C)			40	V
IIN_PK_P	Positive Peak Current During Surge test	+200 V Surge (IEC61000−4−5 TA = −40°C to 85°C)			100	A
VOUT_MAX	Maximum VOUT During Positive Surge	VBUS=11 V+200 V Surge (IEC61000−4−5), OVLO_SEL=LOW, ENB=LOW, RL=Open, no COUT, TA = −40°C to 85°C			15	V
		VBUS=21 V+200 V Surge (IEC61000−4−5), OVLO_SEL=HIGH, ENB=LOW, RL=Open, no COUT, TA = −40°C to 85°C			23	V
VRW_N	Negative Reverse Working Voltage		−0.2			V
VF_TVS	Forward Voltage of TVS	IIN = −10 mA	−0.8	−0.6	−0.2	V
VCL_N	Negative Clamping Voltage	−200 V Surge (IEC61000−4−5)	−6			V
IIN_PK_N	Negative Peak Current During Surge test	−200 V Surge (IEC61000−4−5), T_A = −40°C to 85°C	−100			A

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, VBUS = 2.7 to 21.0 V, TA = −40 to 85°C; Typical values are at VBUS = 5 V, IIN ≤ 12 A, ENB=DIS=LOW, OVLO_SEL=GND, BUS_DET=Floating, CIN = 1 μF and TA = 25°C.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VBUS TO VOUT SWITCH						
V_{OVLO}	Over−Voltage Trip Level	VBUS Rising, OVLO_SEL=GND TA= −40 to 85°C	12.1	12.4	12.7	V
		VBUS Falling, OVLO_SEL=GND TA= −40 to 85°C		12.1		V
		VBUS Rising, OVLO_SEL=GND TA= −40 to 85°C(OTP Option)	13.4	13.7	14.0	V
		VBUS Falling, OVLO_SEL=GND TA= −40 to 85°C(OTP Option)		13.4		V
		VBUS Rising, OVLO_SEL = HIGH TA = −40°C to 85°C	21.5	21.9	22.3	V
		VBUS Falling, OVLO_SEL = HIGH TA = −40°C to 85°C		21.5		V
RON_VOUT	On−Resistance (Note 5)	VBUS = 5 V, IOUT = 200 mA, TA = 25°C		9	12	mΩ
		VBUS = 12 V, IOUT = 200 mA, TA = 25°C		9	12	
		VBUS = 21 V, IOUT = 200 mA, TA = 25°C		9	12	
tDEB_VOUT	Debounce Time	Time from VUVLO < VBUS < VOVLO to VOUT = 0.1 × VBUS		15	20	ms
tON_VOUT	Switch Turn−On Time	RL = 100 Ω, CL = 1 μF, VOUT from 0.1 × VBUS to 0.9 × VBUS		1	3	ms
tOFF_OVP	Switch Turn−Off Time (Note 4)	RL=100 Ω, COUT=1 μF, OVLO_SEL = LOW, Time from VBUS = VBUS_OVLO to VOUT stop rising. Measured when VBUS rises from 0 V to 15 V at 14 V/1 μs Slew Rate under IEC61000−4−5 spec		50		ns
		RL = 100 Ω, COUT = 1 μF, OVLO_SEL = HIGH, Time from VBUS = VBUS_OVLO to VOUT stop rising. Measured when VBUS rises from 0 V to 25 V at 14 V/1 μs Slew Rate under IEC61000−4−5 spec		50		ns
tOFF_ENB	Switch Turn−Off Time by control	RL = 100 Ω, COUT = 1μF, VENB > VIH to VOUT = 0.9 × VBUS		12	18	μs
VOUT TO VBUS SWITCH (OTG Mode)						
RON_OTG	On−Resistance	VOUT = 5 V, IBUS = 200 mA, TA = 25°C		9	12	mΩ
VUVLO_OTG	OTG_DET Under−Voltage Lockout Level	OTG_DET Rising, TA= −40 to 85°C	2.80	2.95	3.10	V
		OTG_DET Falling, TA= −40 to 85°C		2.80		V
tDON_OTG	OTG Start−up Delay Time	Time from OTG_DET > UVLO_OTG to VBUS FET Fully ON			1	ms
IOTG_DET	Current at OTG_DET	OTG_DET = 2.5 V, VOUT = 0 V, ENB = LOW, VBUS = Open, TA = −40°C to 85°C		55	70	μA
		OTG_DET = 5 V, VOUT = 0 V, ENB = LOW, VBUS = Open, TA = −40°C to 85°C		66	120	
		OTG_DET = 4.5V, VOUT = 5V, ENB = LOW, VBUS open, TA = −40°C to 85°C			1	
		OTG_DET = 0V, VOUT = 5V, ENB = LOW, VBUS open, TA = −40°C to 85°C			1	

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, VBUS = 2.7 to 21.0 V, TA = −40 to 85°C; Typical values are at VBUS = 5 V, IIN ≤ 12 A, ENB=DIS=LOW, OVLO_SEL=GND, BUS_DET=Floating, CIN = 1 μF and TA = 25°C.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ALWAYS ON LDO, BUS_DET						
VBUS_DET	BUS_DET Output Voltage	VBUS = 5 V, IBUS_DET = 0 mA, TA = 25°C	3.8	4.0	4.2	V
		VBUS = 21 V, IBUS_DET = 0 mA, TA = 25°C	3.8	4.0	4.2	
		VBUS = 5 V, IBUS_DET = 10 mA, TA = 25°C	3.8	4.0	4.2	
		VBUS = 21 V, IBUS_DET = 10 mA, TA = 25°C	3.8	4.0	4.2	
tSTART_BUS_DET	BUS_DET Output Startup de−bounce time	Time from VBUS > VUVLO to BUS_DET = 0.1 × VBUS_DET		30		ms
tR_BUS_DET	BUS_DET Output Rising time	Time from BUS_DET = 0.1 × VBUS_DET to BUS_DET = 0.9 × VBUS_DET, CBUS_DET = 1μF, RL = 10kΩ		0.1		ms
DIGITAL SIGNALS						
VFLAGB_OL	OV_FLAGB Output LOW Voltage	VIO (Pull up voltage)=1.2 V/1.8 V, Rpu = 100 kΩ			0.36	V
$T_{FLAGB\_PWR\_DELAY}$	OV_FLAGB Assertion delay Time	ENB=Low, Time from VBUS ≥ VBUS_OVLO to OV_FLAGB assertion			3	μs
		ENB=High, Time from VBUS ≥ VBUS_OVLO to OV_FLAGB assertion			3	μs
tFLAGB_REC_EN	OV_FLAGB Recovery de−bounce Time when enabled	ENB=Low, Time from VBUS ≤ VBUS_OLVO to OV_FLAGB de−assertion	16			ms
tFLAGB_REC_DIS	OV_FLAGB Recovery de−bounce Time when disabled	ENB=High, Time from VBUS ≤ VBUS_OLVO to OV_FLAGB de−assertion	100	200		μs
TOV_FLAGB_REC	OV_FLAGB Recovery de−bounce Time when the device in thermal shutdown status	Time from VBUS < VOVLO to OV_FLAGB de−assertion, device in thermal shutdown mode		3		ms
RPD_ENB_DIS_OVSEL	Internal Pull−Down Resistor at ENB, DIS and OVLO_SEL pin			1		MΩ
VIH_ENB_DIS_OVSEL	Logic Enable HIGH Voltage	VBUS operating range	0.84			V
VIL_ENB_DIS_OVSEL	Logic Enable LOW Voltage	VBUS operating range			0.54	V
IBUS_DET_LEAK	BUS_DET Leakage Current	VBUS_DET = 5 V, VBUS= 0 V			1	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Guaranteed by characterization and design.
5. Self−heating is not included

Timing Diagrams

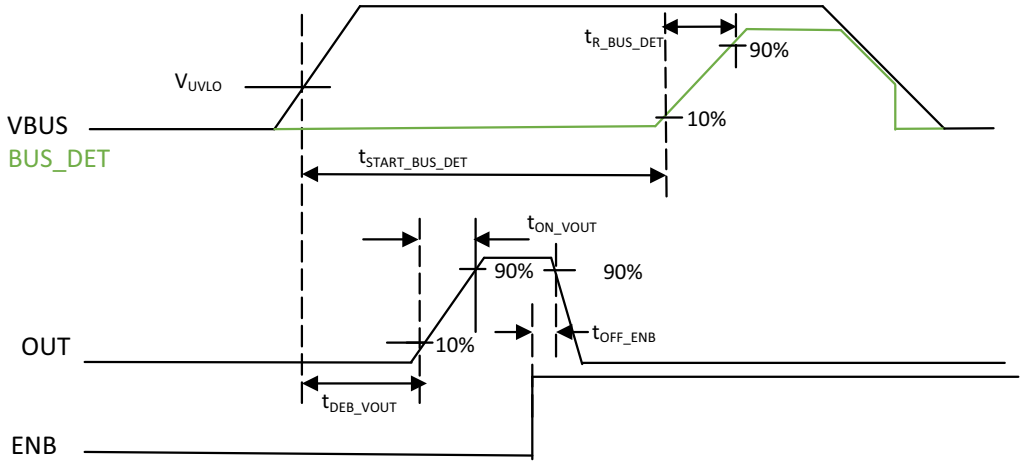


Figure 5. VBUS to VOUT Power Up/Down and Normal Operation

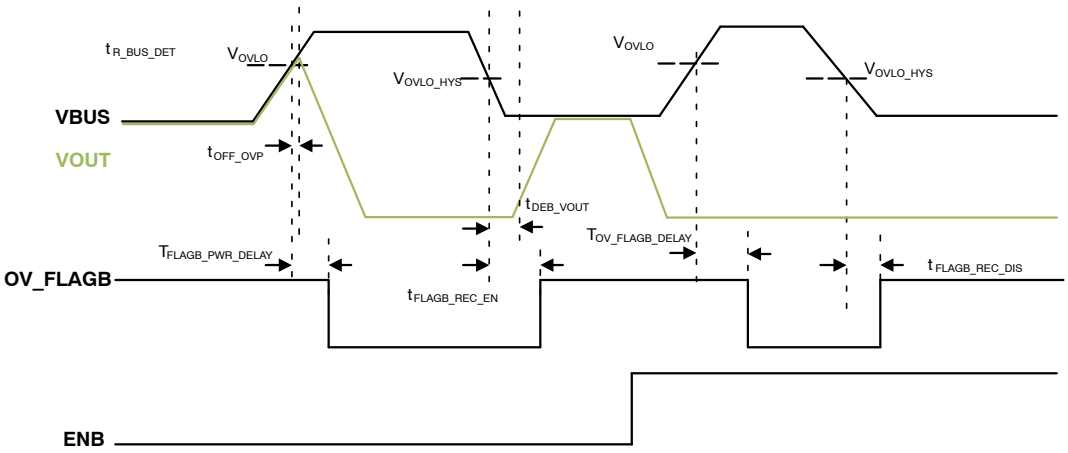


Figure 6. VBUS to VOUT OVLO Operation

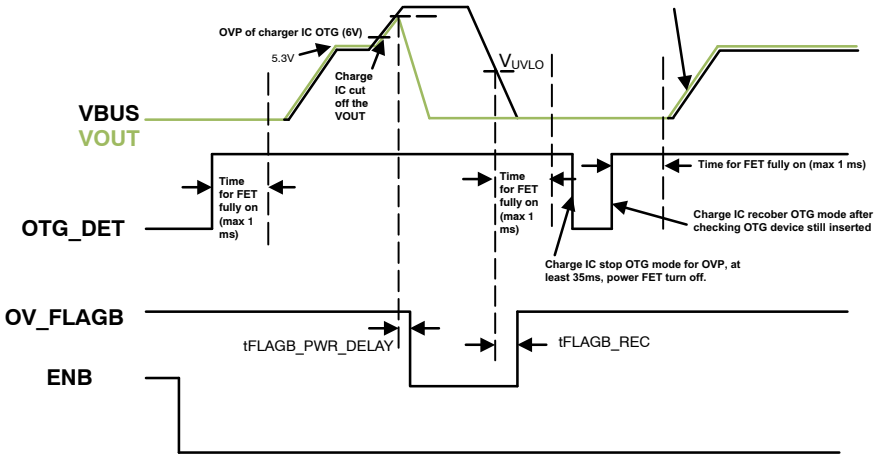


Figure 7. OVP in OTG Mode Operation (with Charger IC internal OVP 6V)

Timing Diagrams

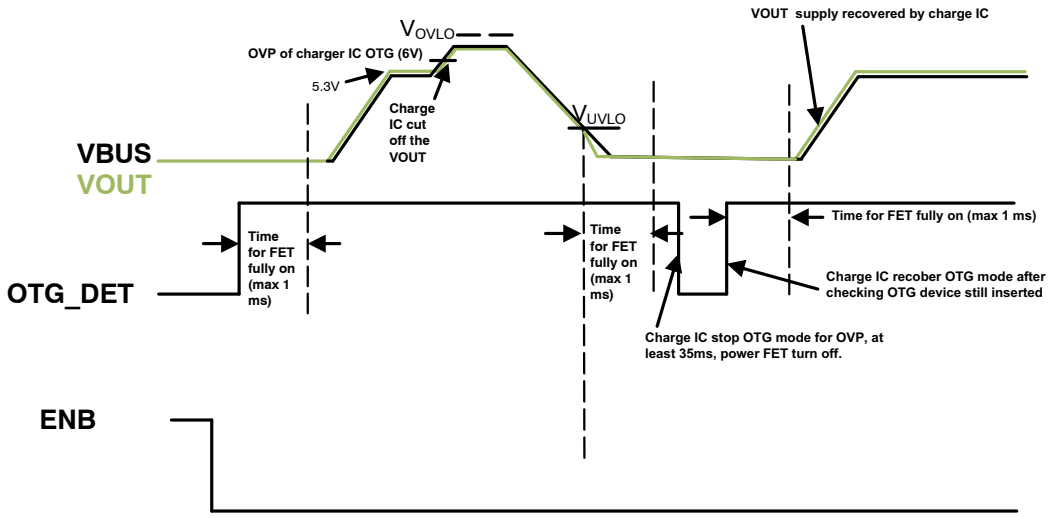


Figure 8. HV event without OVLO in OTG Mode Operation (with Charger IC internal OVP 6V)

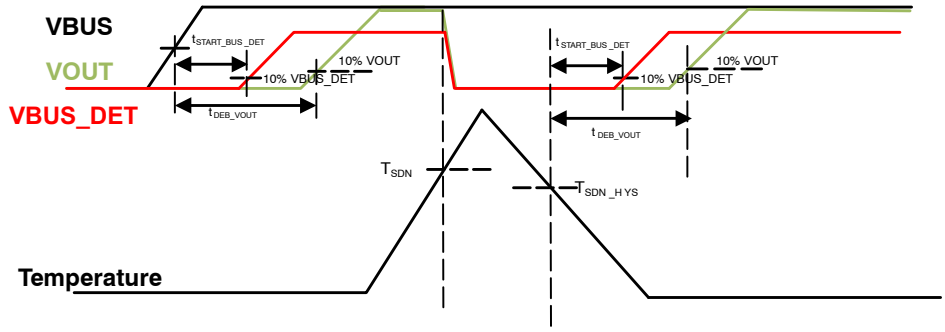


Figure 9. Thermal Shutdown Operation

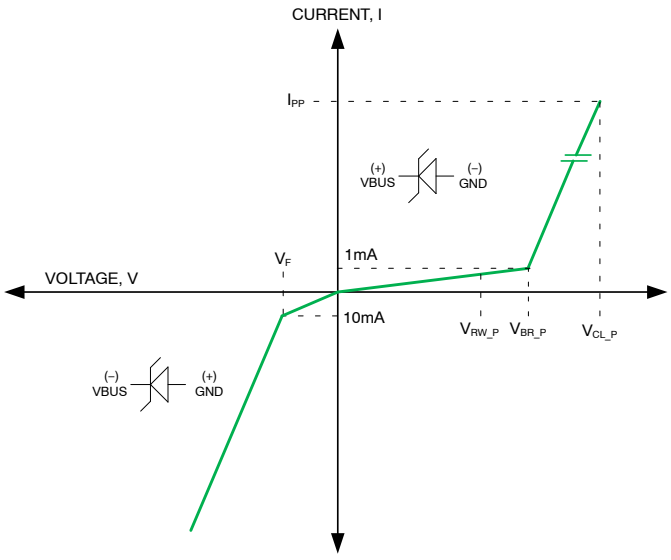


Figure 10. Integrated TVS IV Curve at VBUS

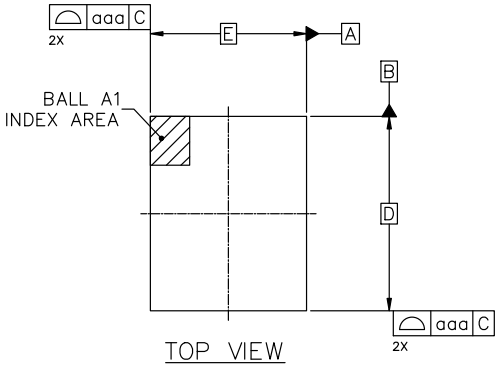
ORDERING INFORMATION

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method†
FPF2188LUCX	−40°C to +85°C	29	20−Ball, 0.4 mm Pitch WLCSP	Tape & Reel

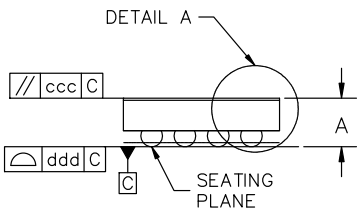
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

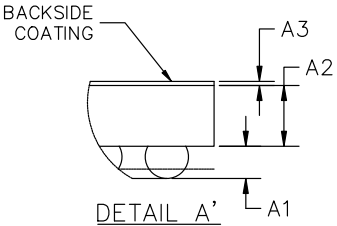
WLCSP20 1.88x2.34x0.32, 0.40P
CASE 567US
ISSUE B



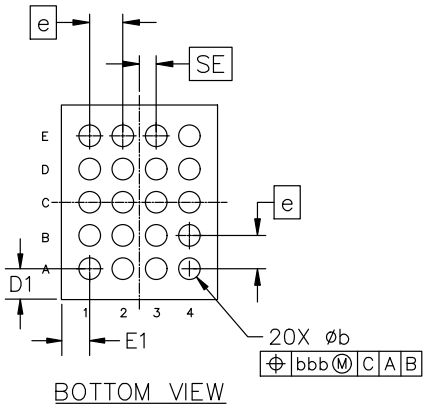
TOP VIEW



SIDE VIEW



DETAIL A'
SCALE 2:1

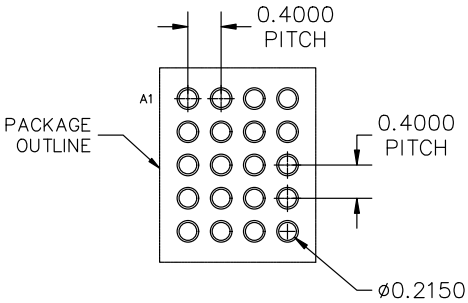


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.482	0.515	0.548
A1	0.185	0.200	0.215
A2	0.275	0.290	0.305
A3	0.022	0.025	0.028
b	0.255	0.270	0.285
D	2.340 BSC		
D1	0.350	0.365	0.380
E	1.880 BSC		
E1	0.320	0.335	0.350
e	0.400 BSC		
TOLERANCES OF FORM AND POSITION			
aaa	0.030		
bbb	0.005		
ccc	0.060		
ddd	0.050		



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales